Renesas Electronics America Inc - UPD78F0483GK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0483gk-gak-ax

1.3 Ordering Information

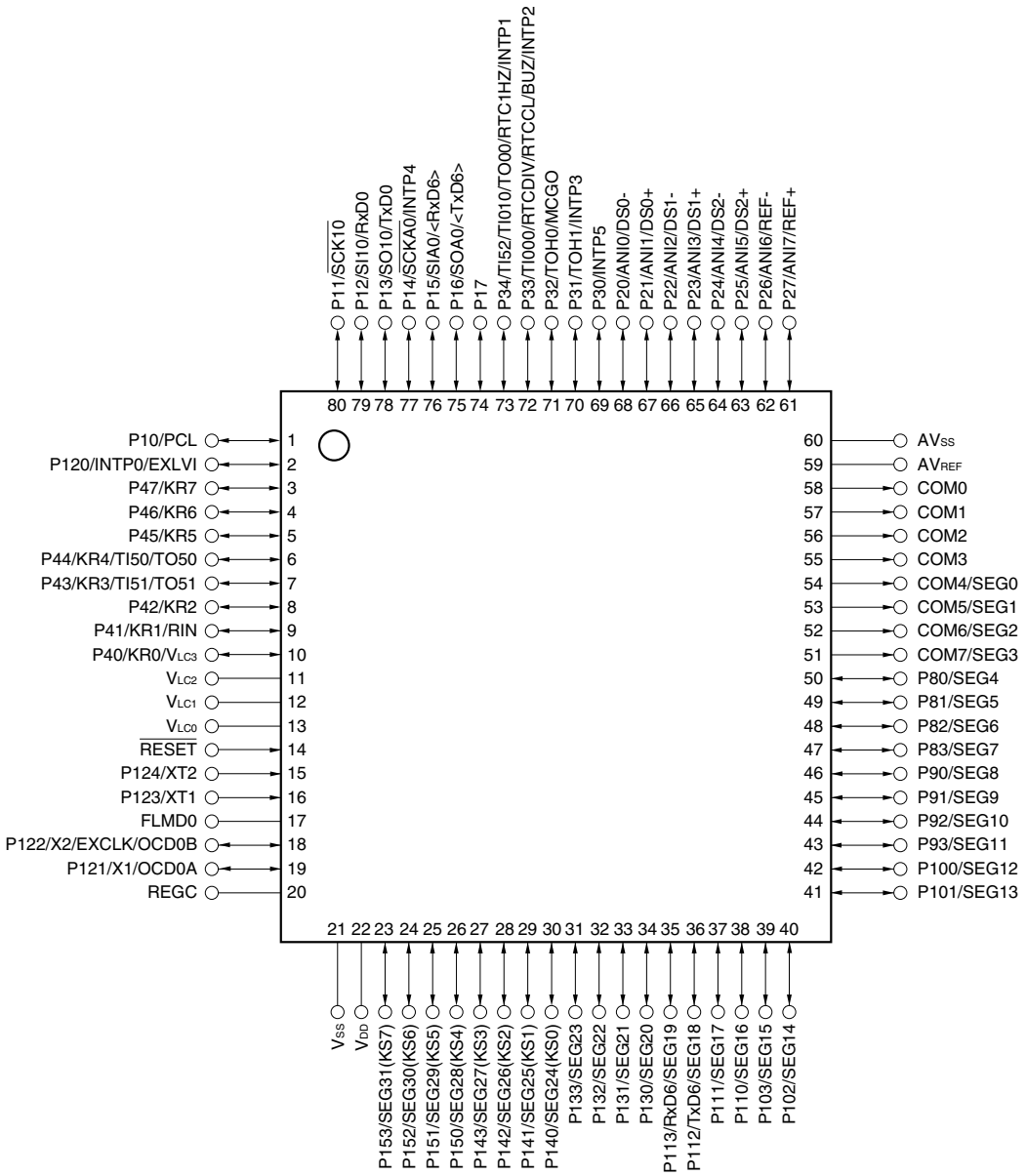
- **Flash memory version (Lead-free products)**

Part Number	Package
μPD78F0471GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0472GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0473GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0474GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0475GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0471GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0472GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0473GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0474GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0475GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0481GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0482GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0483GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0484GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0485GC-GAD-AX	80-pin plastic LQFP (14 × 14)
μPD78F0481GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0482GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0483GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0484GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0485GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0491GC-GAD-AX[Note]	80-pin plastic LQFP (14 × 14)
μPD78F0492GC-GAD-AX[Note]	80-pin plastic LQFP (14 × 14)
μPD78F0493GC-GAD-AX[Note]	80-pin plastic LQFP (14 × 14)
μPD78F0494GC-GAD-AX[Note]	80-pin plastic LQFP (14 × 14)
μPD78F0495GC-GAD-AX[Note]	80-pin plastic LQFP (14 × 14)
μPD78F0491GK-GAK-AX[Note]	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0492GK-GAK-AX[Note]	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0493GK-GAK-AX[Note]	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0494GK-GAK-AX[Note]	80-pin plastic LQFP (fine pitch) (12 × 12)
μPD78F0495GK-GAK-AX[Note]	80-pin plastic LQFP (fine pitch) (12 × 12)

Note Under development

(3) μPD78F0491, 78F0492, 78F0493, 78F0494, 78F0495

- 80-pin plastic LQFP (14 × 14)
- 80-pin plastic LQFP (fine pitch) (12 × 12)



Cautions 1. Connect the AVSS pin to VSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF: recommended).

3. ANI0/P20 to ANI7/P27 are set in the analog input mode after release of reset.

4. Only the bottom side pins (pin numbers 35 and 36) correspond to the UART6 pins (RxD6 and TxD6) when writing by a flash memory programmer. Writing cannot be performed by the top side pins (pin numbers 76 and 75).

Remarks 1. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

<R> **2.** The functions within parentheses can be used by setting the LCD mode register (LCDMD).

(2/2)

Item		μPD78F0491	μPD78F0492	μPD78F0493	μPD78F0494	μPD78F0495
10-bit successive approximation type A/D converter		10-bit resolution × 8 channels (AV_{REF} = 2.3 to 5.5 V)				
16-bit ΔΣ type[Note 1] A/D converter		16-bit resolution × 3 channels (AV_{REF} = 2.7 to 5.5 V)				
Serial interface		• UART supporting LIN-bus[Note 2]: 1 channel • 3-wire serial I/O/UART[Note 3]: 1 channel • Automatic transmit/receive 3-wire CSI: 1 channel				
LCD controller/driver		• External resistance division and internal resistance division are switchable. • Segment signal outputs: 32 (28) [28 (24)][Note 4, 5] • Common signal outputs: 4 (8)[Note 4]				
Remote controller receiver		Provided				
Manchester code generator		Provided				
Vectored interrupt sources	Internal	22				
	External	7				
<R> Segment key source signal output		Segment key source signal outputs: 8 (SEG24(KS0)-SEG31(KS7))				
Key interrupt		Key interrupt (INTKR) occurs by detecting falling edge of key input pins (KR0 to KR7).				
Reset		• Reset using $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 1.8 to 5.5 V				
Operating ambient temperature		T_A = −40 to +85°C				
Package		• 80-pin plastic LQFP (14 × 14) • 80-pin plastic LQFP (fine pitch) (12 × 12)				

Notes 1. The specifications of the 16-bit ΔΣ A/D converter may have been changed.
For details of the specifications, contact an NEC Electronics sales representative or authorized dealer.

2. The LIN-bus supporting UART pins can be changed to the automatic transmit/receive 3-wire CSI pins (pin numbers 75 and 76).

3. Select either of the functions of these alternate-function pins.

4. The values in parentheses are the number of signal outputs when 8com is used.

<R> **5.** The values in square brackets are the number of signal outputs when using the UART6 pins (RxD6, TxD6) on the bottom side.

3.1.2 Internal data memory space

78K0/LF3 products incorporate the following RAMs.

(1) Internal high-speed RAM

Table 3-5. Internal High-Speed RAM Capacity

Part Number	Internal High-Speed RAM
μPD78F0471, 78F0481, 78F0491	768 × 8 bits (FC00H to FEFFH)
μPD78F0472, 78F0482, 78F0492	1024 × 8 bits (FB00H to FEFFH)
μPD78F0473, 78F0483, 78F0493	
μPD78F0474, 78F0484, 78F0494	
μPD78F0475, 78F0485, 78F0495	

This area cannot be used as a program area in which instructions are written and executed.

The internal high-speed RAM can also be used as a stack memory.

(2) Internal expansion RAM

Table 3-6. Internal Expansion RAM Capacity

Part Number	Internal Expansion RAM
μPD78F0471, 78F0481, 78F0491	–
μPD78F0472, 78F0482, 78F0492	
μPD78F0473, 78F0483, 78F0493	
μPD78F0474, 78F0484, 78F0494	1024 × 8 bits (F400H to F7FFH)
μPD78F0475, 78F0485, 78F0495	

The internal expansion RAM can also be used as a normal data area similar to the internal high-speed RAM, as well as a program area in which instructions can be written and executed.

The internal expansion RAM cannot be used as a stack memory.

(3) LCD display RAM

LCD display RAM is incorporated in the LCD controller/driver (see Figure 18-5 LCD Display RAM).

Table 3-7. LCD Display RAM Capacity

Part Number	Internal Expansion RAM
μPD78F047x, 78F048x	40 × 8 bits (FA40H to FA67H)
μPD78F049x	32 × 8 bits (FA40H to FA5FH)

3.1.3 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FF00H to FFFFH (see **Table 3-8 Special Function Register List** in **3.2.3 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.4.7 Based addressing

[Function]

8-bit immediate data is added as offset data to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all of the memory spaces.

[Operand format]

Identifier	Description
–	[HL + byte]

[Description example]

MOV A, [HL + 10H]; when setting byte to 10H

Operation code

1	0	1	0	1	1	1	0

0	0	0	1	0	0	0	0

[Illustration]

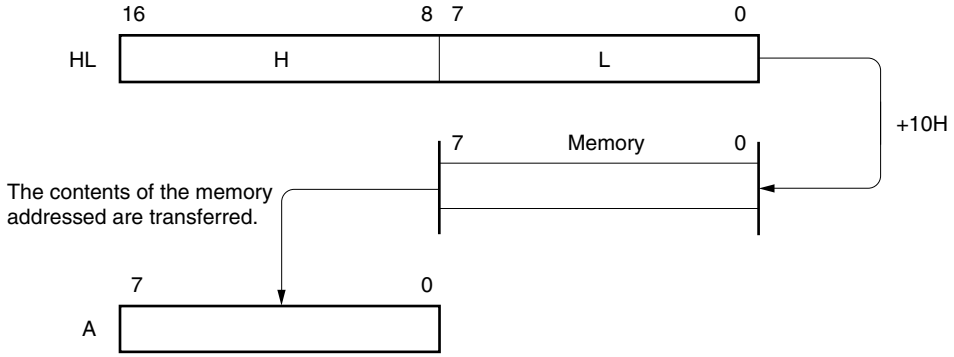
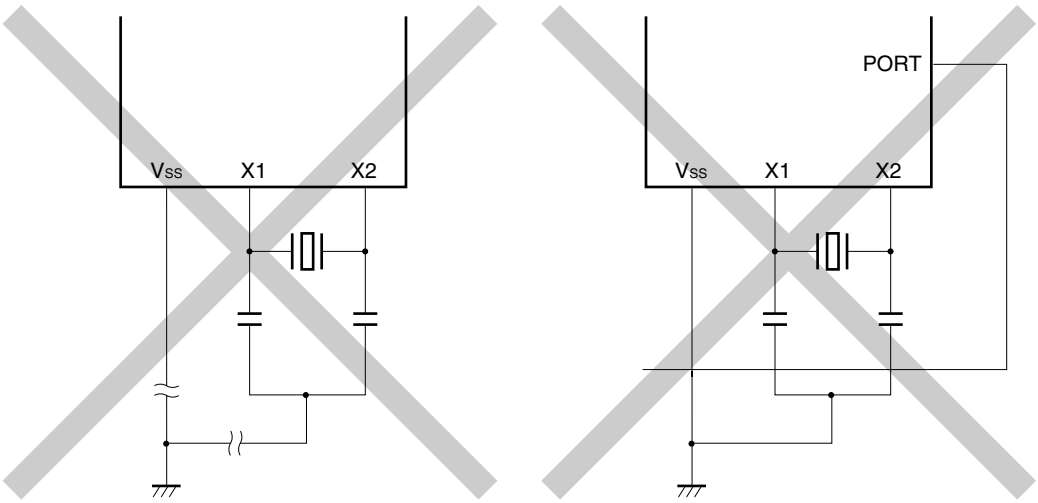


Figure 5-12 shows examples of incorrect resonator connection.

Figure 5-12. Examples of Incorrect Resonator Connection (1/2)

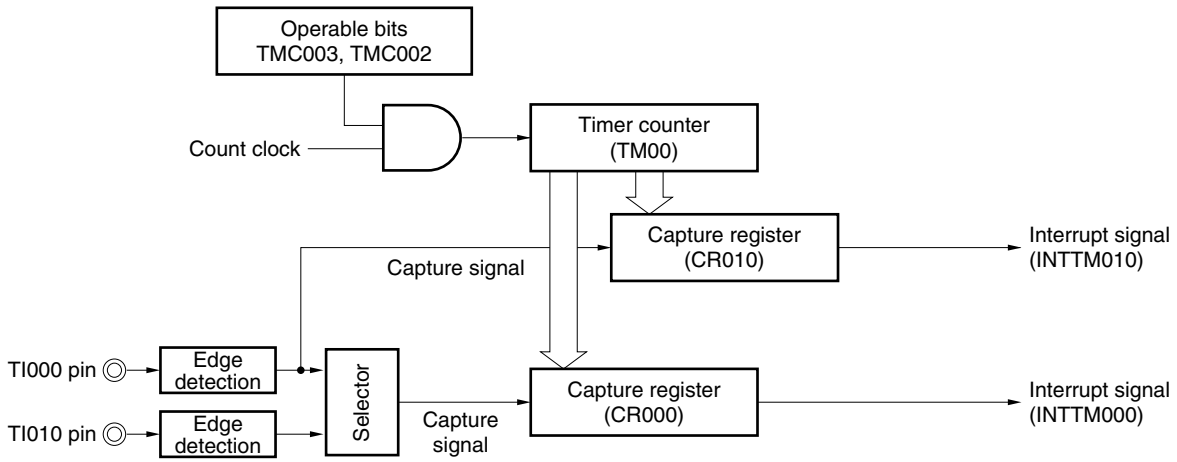
(a) Too long wiring **(b) Crossed signal line**



Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

(3) Free-running timer mode operation
(CR000: capture register, CR010: capture register)

Figure 6-37. Block Diagram of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register)

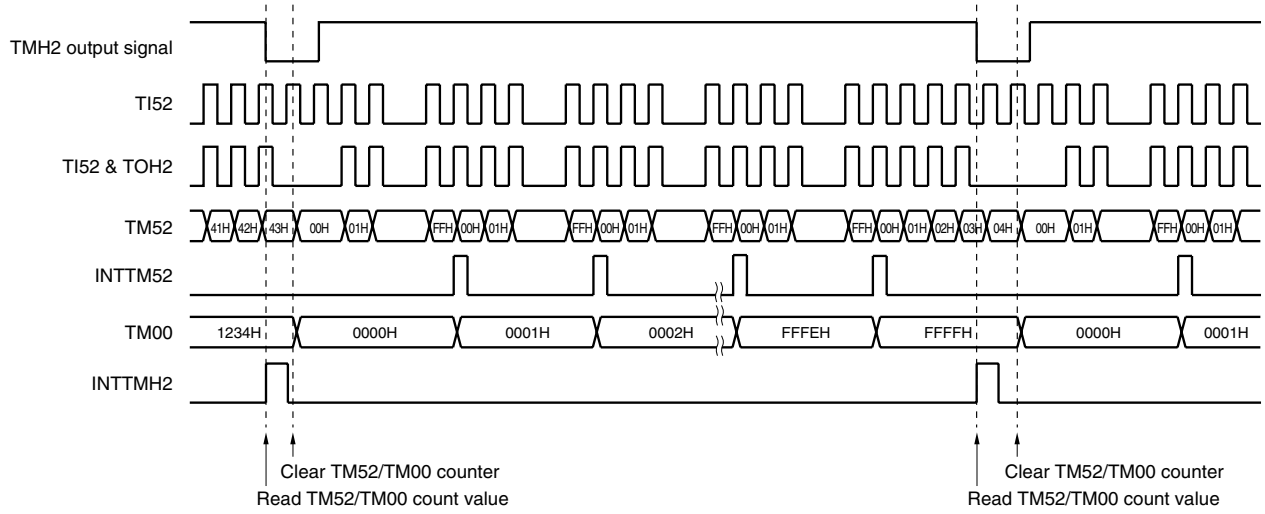


Remark If both CR000 and CR010 are used as capture registers in the free-running timer mode, the TO00 output level is not inverted.
However, it can be inverted each time the valid edge of the TI000 pin is detected if bit 1 (TMC001) of 16-bit timer mode control register 00 (TMC00) is set to 1.

<3> When the TM52 and CR52 (= FFH) values match, TM52 is cleared to 00, and the match signal causes TM000 to start counting up. Then, when the TM000 and CR000 values match, TM00 is cleared to 0000H, and a match interrupt signal (INTTM000) is generated.

If input enable for the TI52 pin is controlled, external event count values within the input enable periods for the TI52 pin can be measured, by reading TM52, the TM00 count value, and TMIF52 via interrupt servicing by the TMH2 interrupt request signal (INTTMH2).

Figure 6-55. Operation Timing of External 24-bit Event Counter



12.2 Configuration of 10-Bit Successive Approximation Type A/D Converter

The 10-bit successive approximation type A/D converter includes the following hardware.

(1) ANI0 to ANI7 pins

These are the 8-channel analog input pins of the 10-bit successive approximation type A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins or segment output pins (μPD78F048x only).

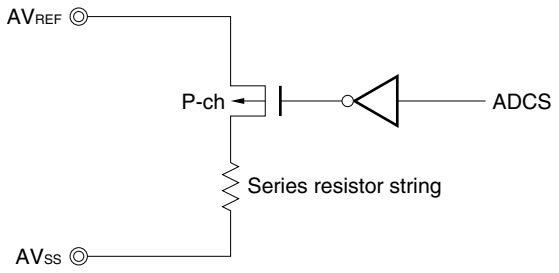
(2) Sample & hold circuit

The sample & hold circuit samples the input voltage of the analog input pin selected by the selector when A/D conversion is started, and holds the sampled voltage value during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AV_{REF} and AV_{SS}, and generates a voltage to be compared with the sampled voltage value.

Figure 12-2. Circuit Configuration of Series Resistor String



(4) Voltage comparator

The voltage comparator compares the sampled voltage value and the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register converts the result of comparison by the voltage comparator, starting from the most significant bit (MSB).

When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(6) 10-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its higher 10 bits (the lower 6 bits are fixed to 0).

Figure 13-2. Format of 16-bit ΔΣ type A/D Converter Control Register 0 (ADDCTL0)

Address: FF7CH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
ADDCTL0	ADPON	ADDCE	HAC	AINMCD	0	0	ADDS1	ADDS0

ADDPON	16-bit ΔΣ type A/D circuit power supply control
0	Power supply OFF
1	Power supply ON

ADDCE	16-bit ΔΣ type A/D conversion operation control
0	Stops conversion operation
1	Starts conversion operation

HAC	Setting 16-bit ΔΣ type A/D conversion high-accuracy mode
0	High-accuracy mode OFF
1	High-accuracy mode ON

AINMOD	16-bit ΔΣ type A/D conversion input mode control
0	Single input
1	Differential input

ADDS1	ADDS0	16-bit ΔΣ type analog input specification
0	0	DS0+/DS0-
0	1	DS1+/DS1-
1	0	DS2+/DS2-
1	1	Setting prohibited

Cautions 1. Do not set the ADDPON and ADDCE bits to 1 at the same time. ADDCE must be set to 1, at least 1.2 μs after ADDPON has been set to 1.

2. Setting the ΔΣ analog input channel to be set by ADDS1 and ADDS0 to a pin which has been selected to be used in the analog input mode by the ADPC0 register is prohibited.

3. Operating 16-bit ΔΣ type A/D conversion and 10-bit successive approximation type A/D conversions at the same time (ADDCE = 1 and ADCS = 1) is prohibited.

4. If ADDCTL0 is rewritten (including identical data), A/D conversion operation is resumed after it has been initialized.

5. Set the input voltage in accordance with Table 13-4 Input Voltage Range.

6. When executing a STOP instruction, power to the 16-bit ΔΣ type A/D converter must be turned off (ADDPON = 0).

Remark LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol intended to aid the cost reduction of an automotive network.

LIN communication is single-master communication, and up to 15 slaves can be connected to one master.

The LIN slaves are used to control the switches, actuators, and sensors, and these are connected to the LIN master via the LIN network.

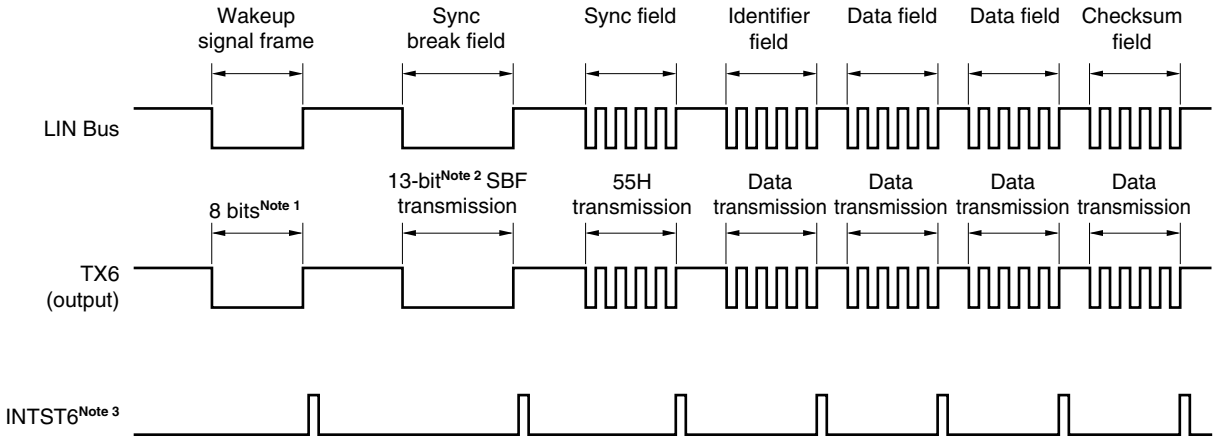
Normally, the LIN master is connected to a network such as CAN (Controller Area Network).

In addition, the LIN bus uses a single-wire method and is connected to the nodes via a transceiver that complies with ISO9141.

In the LIN protocol, the master transmits a frame with baud rate information and the slave receives it and corrects the baud rate error. Therefore, communication is possible when the baud rate error in the slave is ±15% or less.

Figures 15-1 and 15-2 outline the transmission and reception operations of LIN.

Figure 15-1. LIN Transmission Operation



Notes 1. The wakeup signal frame is substituted by 80H transmission in the 8-bit mode.

2. The sync break field is output by hardware. The output width is the bit length set by bits 4 to 2 (SBL62 to SBL60) of asynchronous serial interface control register 6 (ASICL6) (see **15.4.2 (2) (h) SBF transmission**).

3. INTST6 is output on completion of each transmission. It is also output when SBF is transmitted.

Remark The interval between each field is controlled by software.

(e) Normal reception

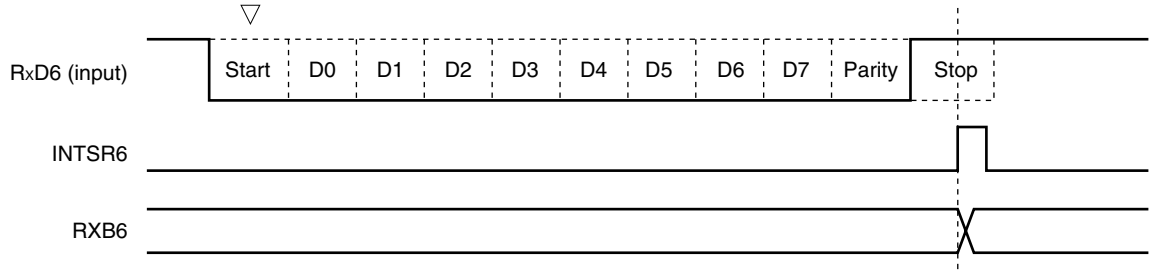
Reception is enabled and the RxD6 pin input is sampled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1.

The 8-bit counter of the baud rate generator starts counting when the falling edge of the RxD6 pin input is detected. When the set value of baud rate generator control register 6 (BRGC6) has been counted, the RxD6 pin input is sampled again (▽ in Figure 15-21). If the RxD6 pin is low level at this time, it is recognized as a start bit.

When the start bit is detected, reception is started, and serial data is sequentially stored in the receive shift register (RXS6) at the set baud rate. When the stop bit has been received, the reception completion interrupt (INTSR6) is generated and the data of RXS6 is written to receive buffer register 6 (RXB6). If an overrun error (OVE6) occurs, however, the receive data is not written to RXB6.

Even if a parity error (PE6) occurs while reception is in progress, reception continues to the reception position of the stop bit, and a reception error interrupt (INTSR6/INTSRE6) is generated on completion of reception.

Figure 15-21. Reception Completion Interrupt Request Timing



Cautions 1. If a reception error occurs, read ASIS6 and then RXB6 to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.

2. Reception is always performed with the "number of stop bits = 1". The second stop bit is ignored.

3. Be sure to read asynchronous serial interface reception error status register 6 (ASIS6) before reading RXB6.

(2) Serial status register 0 (CSIS0)

This is an 8-bit register used to select the base clock, control the communication operation, and indicate the status of serial interface CSIA0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction. However, rewriting CSIS0 is prohibited when bit 0 (TSF0) is 1.

Reset signal generation clears this register to 00H.

Figure 17-3. Format of Serial Status Register 0 (CSIS0)

Address: FF91H After reset: 00H R/W[Note 1]

Symbol	7	6	5	4	3	2	1	0
CSIS0	0	CKS00	0	0	0	0	0	TSF0

CKS00	Base clock (f_W) selection[Note 2]				
		f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	f_{PRS}[Note 3]	2 MHz	5 MHz	8 MHz	10 MHz
1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz

TSF0	Transfer status detection flag
0	• Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 • At reset input • At the end of the specified transfer • When transfer is stopped by setting bit 1 (ATSTP0) of serial trigger register 0 (CSIT0) to 1
1	From the transfer start to the end of the specified transfer

Notes 1. Bit 0 is read-only.

2. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

3. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of CKS00 = 0 (base clock: f_{PRS}) is prohibited.

Cautions 1. Be sure to clear bits 7 and 5 to 1.

2. During transfer (TSF0 = 1), rewriting serial operation mode specification register 0 (CSIMA0), serial status register 0 (CSIS0), divisor selection register 0 (BRGCA0), automatic data transfer address point specification register 0 (ADTP0), automatic data transfer interval specification register 0 (ADTI0), and serial I/O shift register 0 (SIOA0) are prohibited. However, these registers can be read and re-written to the same value. In addition, the buffer RAM can be rewritten during transfer.

Remark f_{PRS}: Peripheral hardware clock frequency

18.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

Table 18-2. Configuration of LCD Controller/Driver

Item	Configuration
Display outputs	μPD78F047x: 40 segment signals[Note 1] (SEG0-SEG39), 8 common signals[Note 1] (COM0 to COM7) μPD78F048x: 40 segment signals[Note 1] (SEG0-SEG39), 8 common signals[Note 1] (COM0 to COM7) μPD78F049x: 32 segment signals[Note 1] (SEG0-SEG31), 8 common signals[Note 1] (COM0 to COM7)
Segment key source output	Segment key source signal: 8 (SEG24 (KS0)-SEG31 (KS7))
Control registers	LCD mode register (LCDMD) LCD display mode register (LCDM) LCD clock control register (LCDC0) Port function register 2 (PF2)[Note 2] Port function register ALL (PFALL) Key return mode register (KRM) Port mode register 4 (PM4) Pull-up resistor option register4 (PU4) Port register 14 (P14) Port register 15 (P15)

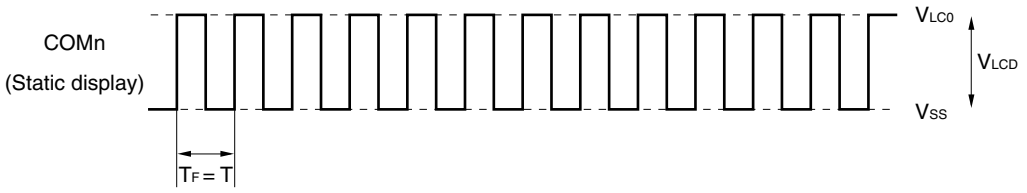
Notes 1. The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register.

2. μPD78F047x and 78F048x only.

Figure 18-13 shows the common signal waveforms, and Figure 18-14 shows the voltages and phases of the common and segment signals.

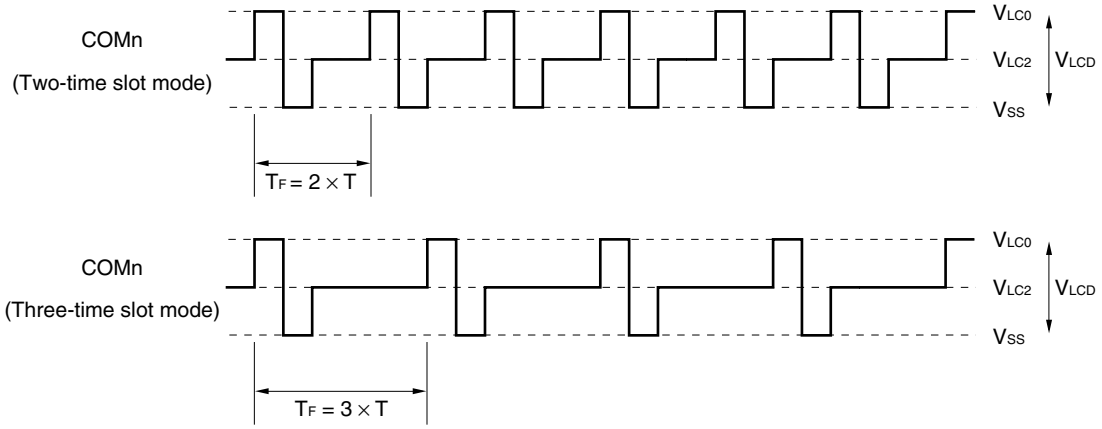
Figure 18-13. Common Signal Waveforms

(a) Static display mode



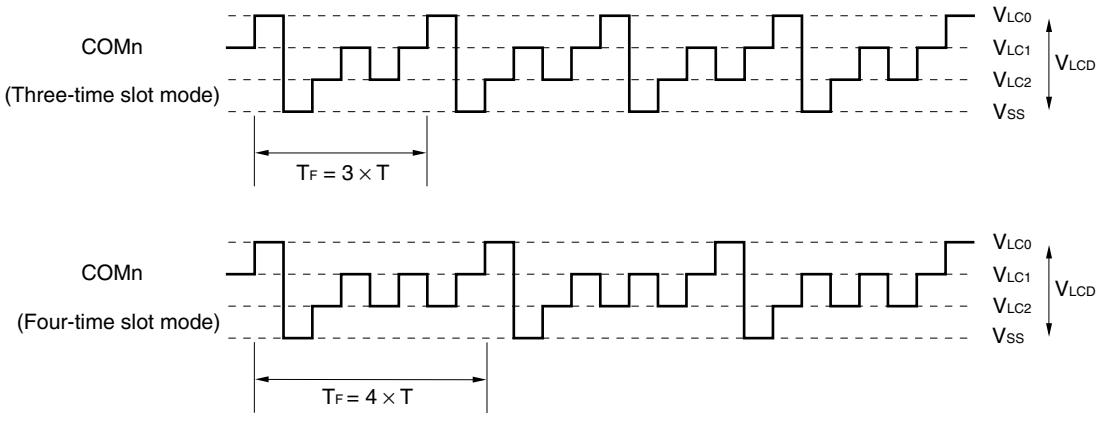
T: One LCD clock period T_F: Frame frequency

(b) 1/2 bias method



T: One LCD clock period T_F: Frame frequency

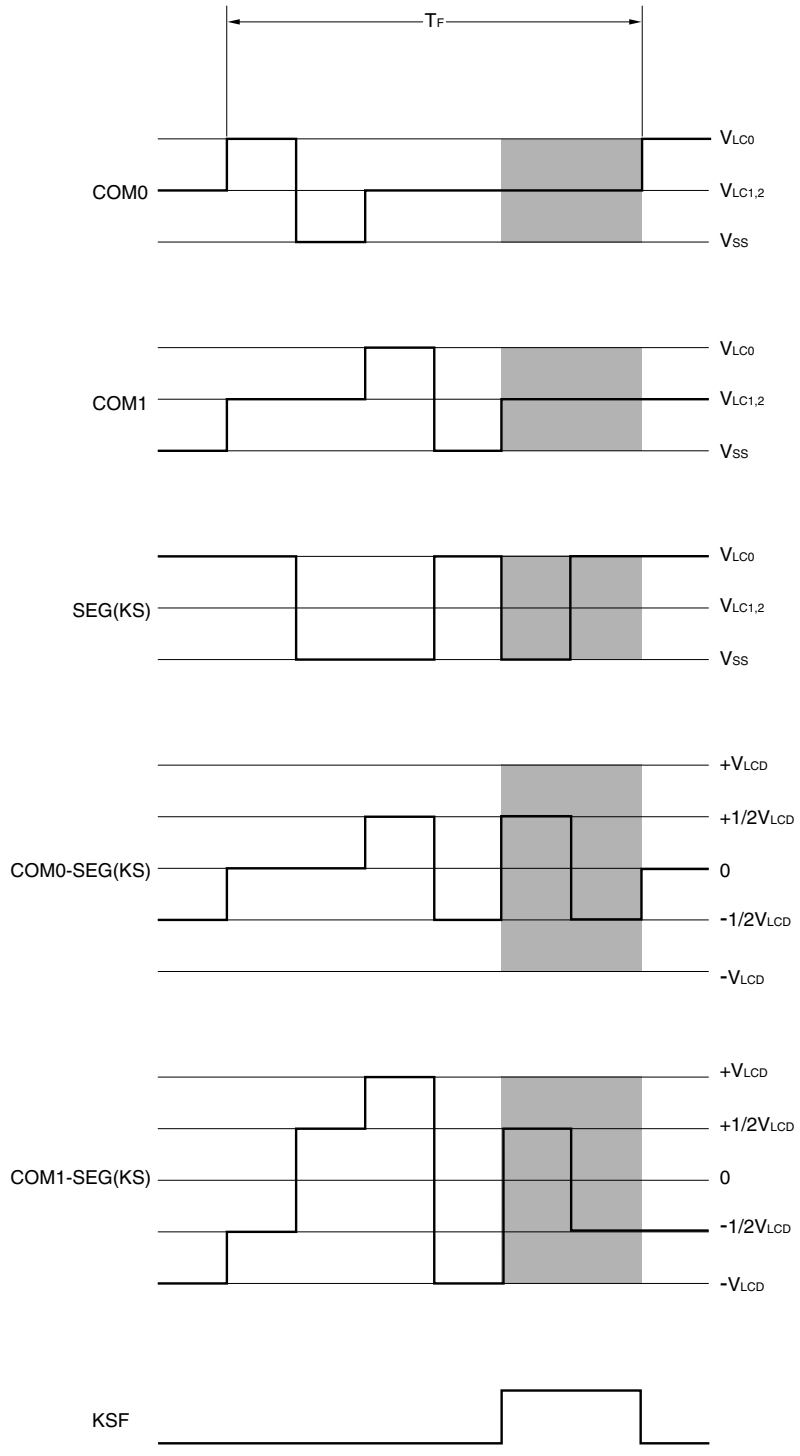
(c) 1/3 bias method



T: One LCD clock period T_F: Frame frequency

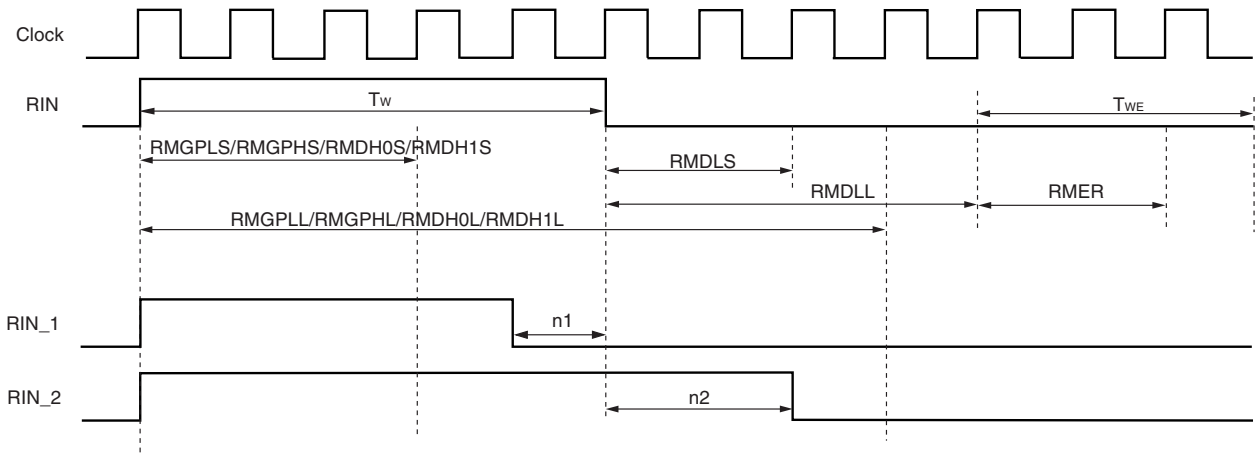
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

Figure 20-12. Setting Example (Where n1 = 1, n2 = 2)



(1) Formula for RMGPLS, RMGPHS, RMDLS, RMDH0S, and RMDH1S

$$\left[\frac{T_W \times (1 - a/100)}{1/f_{REMPRS}}\right]_{INT} - 2 - n1$$

(2) Formula for RMGPLL, RMGPHL, RMDLL, RMDH0L, and RMDH1L

$$\left[\frac{T_W \times (1 + a/100)}{1/f_{REMPRS}}\right]_{INT} + 1 + n2$$

(3) Formula for RMER

$$\left[\frac{T_{WE} \times (1 - a/100)}{1/f_{REMPRS}}\right]_{INT} - 1$$

T_W: Width of RIN input waveform

$1/f_{REMPRS}$: Width of internal operation clock cycle after division control by PRSEN

a: Tolerance (%)

$[\ ]_{INT}$: Round down the fractional portion of the value produced by the formula in the brackets.

n1, n2: Variables of waveform change caused by noise[Note1]

T_{WE}: End width of RIN input[Note2]

Notes 1. Set the values of n1 and n2 as required to meet the user's system specification.

2. This end width is counted after RMDLL.
The low-level width actually required after the last data has been received is as follows:
(RMDLL + 1 + RMER + 1) × (width of internal operation clock cycle after division control by PRSEN)

Table 23-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

23.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

26.4.2 When used as interrupt

(1) When detecting level of supply voltage (V_{DD})

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Clear bit 2 (LVISEL) of the low-voltage detection register (LVIM) to 0 (detects level of supply voltage (V_{DD})) (default value).
  - <3> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <4> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <5> Use software to wait for an operation stabilization time (10 μs (MAX.)).
  - <6> Confirm that "supply voltage (V_{DD}) $\geq$ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of LVIM.
  - <7> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <8> Release the interrupt mask flag of LVI (LVIMK).
  - <9> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <10> Execute the EI instruction (when vector interrupts are used).

  Figure 26-7 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <9> above.

- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVION to 0.

(2/3)

Edition	Description	Applied to:
2nd edition	Change of **Figure 14-1 Block Diagram of Serial Interface UART0**	**CHAPTER 14 SERIAL INTERFACE UART0**
	Addition of **Note 1** to **Figure 14-4 Format of Baud Rate Generator Control Register 0 (BRGC0)**	
	Change of **14.3 (5) Port mode register 1 (PM1)**	
	Change of **Table 14-2. Relationship Between Register Settings and Pins**	
	Addition of **Notes 1** and **2** to **Table 14-4 Set Value of TPS01 and TPS00**	
	Change of explanation in **15.1 Functions of Serial Interface UART6**	**CHAPTER 15 SERIAL INTERFACE UART6**
	Change of **Figure 15-4 Block Diagram of Serial Interface UART6**	
	Addition of **Notes 1** and **2** to **Figure 15-8 Format of Clock Selection Register 6 (CKSR6)**	
	Change of **15.3 (9) Port mode register 1 (PM1)**	
	Change of **(a)** in **Table 15-2. Relationship Between Register Settings and Pins**	
	Addition of **Notes 1**, **2**, and **3** to **Table 15-4 Set Value of TPS63 to TPS60**	
	Change of **Figure 16-1. Block Diagram of Serial Interface CSI10**	**CHAPTER 16 SERIAL INTERFACE CSI10**
	Addition of **Notes 1** and **2** to **Figure 16-3 Format of Serial Clock Selection Register 10 (CSIC10)**	
	Change of **Figure 17-1. Block Diagram of Serial Interface CSIA0**	**CHAPTER 17 SERIAL INTERFACE CSIA0**
	Addition of **Notes 2** and **3** to **Figure 17-3. Format of Serial Status Register 0 (CSIS0)**	
	Change of **Note 2** in **18.3 (2) LCD display mode register (LCDM)**	**CHAPTER 18 LCD CONTROLLER/DRIVER**
	Change of **Note** in **18.4 Setting LCD Controller/Driver**	
	Addition of **Notes 1** and **2** to **Figure 19-5. Format of MCG Control Register 1 (MC0CTL1)**	**CHAPTER 19 MANCHESTER CODE GENERATOR**
	Addition of **Notes 1** and **2** to **19.4.2 (b) MCG control register 1 (MC0CTL1)**	
	Change of **Note 4** in **Table 21-1. Interrupt Source List**	**CHAPTER 21 INTERRUPT FUNCTIONS**
	Change of **Note 2** in and addition of **Notes 4**, **5**, and **6** to **Table 21-2 Flags Corresponding to Interrupt Request Sources**	
	Change of **Caution 1** in **Figure 22-2 Format of Key Return Mode Register (KRM)**	**CHAPTER 22 KEY INTERRUPT FUNCTION**
	Addition of explanation to **Caution 3** in **23.1.1 Standby function**	**CHAPTER 23 STANDBY FUNCTION**
	Change of explanation in **26.3 (1) Low-voltage detection register (LVIM)**	**CHAPTER 26 LOW-VOLTAGE DETECTOR**
	Addition of **Notes 1** and **4** and **Cautions 3** and **4** to **Figure 26-2 Format of Low-Voltage Detection Register (LVIM)**	
	Change of explanation in **26.3 (2) Low-voltage detection level selection register (LVIS)**	
	Addition of **Note** and **Caution 4** to **Figure 26-3 Format of Low-Voltage Detection Level Selection Register (LVIS)**	
	Addition of **Note 3** to **Figure 26-7 Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD}))**	
	Addition of **Note 3** to **Figure 26-8 Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))**	
	Change of **Figure 26-9 Example of Software Processing After Reset Release**	