Renesas Electronics America Inc - UPD78F0484GC-GAD-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0484gc-gad-ax

An outline of the timer is shown below.

		16-Bit Timer/ Event Counters 00	8-Bit Timer/ Event Counters 50, 51, and 52			8-Bit Timers H0, H1, and H2			Real-time Counter	Watchdog Timer
		TM00	TM50	TM51	TM52	TMH0	TMH1	TMH2		
Function	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel Note 1	–
	External event counter	1 channel Note 2	1 channel	1 channel	1 channel Note 2	–	–	– Note 2	–	–
	PPG output	1 output	–	–	–	–	–	–	–	–
	PWM output	–	1 output	1 output	–	1 output	1 output	–	–	–
	Pulse width measurement	2 inputs	–	–	–	–	–	–	–	–
	Square-wave output	1 output	1 output	1 output	–	1 output	1 output	–	–	–
	Carrier generator	–	–	– Note 3	–	–	1 output Note 3	–	–	–
	Calendar function	–	–	–	–	–	–	–	1 channel Note 1	
	RTC output	–	–	–	–	–	–	–	2 outputs Note 4	–
	Watchdog timer	–	–	–	–	–	–	–	–	1 channel
Interrupt source		2	1	1	1	1	1	1	1	–

Notes 1. In the real-time counter, the Interval timer function and calendar function can be used simultaneously.

2. TM52 and TM00 can be connected in cascade to be used as a 24-bit counter. Also, the external event input of TM52 can be input enable-controlled via TMH2.

3. TM51 and TMH1 can be used in combination as a carrier generator mode.

4. A 1 Hz output can be used as one output and a 512 Hz, 16.384 kHz, or 32.768 kHz output can be used as one output.

(a) INTP1 to INTP3 and INTP5

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TO00, TOH0, TOH1

These are timer output pin.

(c) TI000

This is a pin for inputting an external count clock to 16-bit timer/event counters 00 and is also for inputting a capture trigger signal to the capture registers (CR000 or CR010) of 16-bit timer/event counters 00.

(d) TI010

This is a pin for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counters 00.

(e) TI52

This is the pin for inputting an external count clock to 8-bit timer/event counter 52.

(f) BUZ

This is a buzzer output pin.

(g) RTCDIV

This is a real-time counter clock (32 kHz, divided) output pin.

(h) RTCCL

This is a real-time counter clock (32 kHz, original oscillation) output pin.

(i) RTC1HZ

This is a real-time counter correction clock (1 Hz) output pin.

(j) MCGO

This is a Manchester code output pin.

2.2.4 P40 to P47 (port 4)

P40 to P47 function as an 8-bit I/O port. These pins also function as pins for key interrupt input, segment key scan input, timer I/O, remote control receive data input, and power supply voltage for driving the LCD.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P47 function as an 8-bit I/O port. P40 and P47 can be set to input port or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

(2) Control mode

P40 and P47 function as key interrupt input, segment key scan input, timer I/O, remote control receive data input, and power supply voltage for driving the LCD.

CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

Each products in the 78K0/LF3 can access a 64 KB memory space. Figures 3-1 to 3-10 show the memory maps.

Caution Regardless of the internal memory capacity, the initial values of the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS) of all products in the 78K0/LF3 are fixed (IMS = CFH, IXS = 0CH). Therefore, set the value corresponding to each product as indicated below.

Table 3-1. Set Values of Internal Memory Size Switching Register (IMS) and Internal Expansion RAM Size Switching Register (IXS)

Flash Memory Version (78K0/LF3)	IMS	IXS	ROM Capacity	Internal High-Speed RAM Capacity	Internal Expansion RAM Capacity
μPD78F0471, 78F0481, 78F0491	04H	0CH	16 KB	768 bytes	–
μPD78F0472, 78F0482, 78F0492	C6H		24 KB	1 KB	
μPD78F0473, 78F0483, 78F0493	C8H		32 KB		
μPD78F0474, 78F0484, 78F0494	CCH	0AH	48 KB		1 KB
μPD78F0475, 78F0485, 78F0495	CFH		60 KB		

3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and return instructions are executed or the register is saved/reset upon generation of an interrupt request.

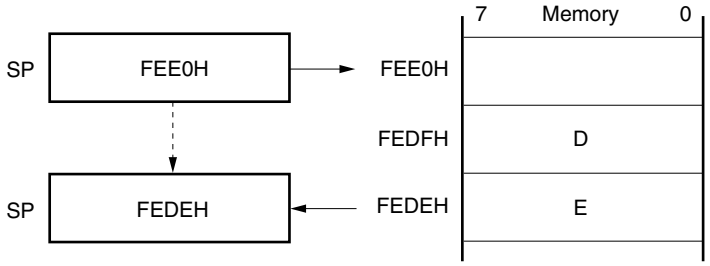
With stack addressing, only the internal high-speed RAM area can be accessed.

[Description example]

PUSH DE; when saving DE register

Operation code	1	0	1	1	0	1	0	1

[Illustration]



CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are two types of pin I/O buffer power supplies: AV_{REF}[Note] and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 4-1. Pin I/O Buffer Power Supplies

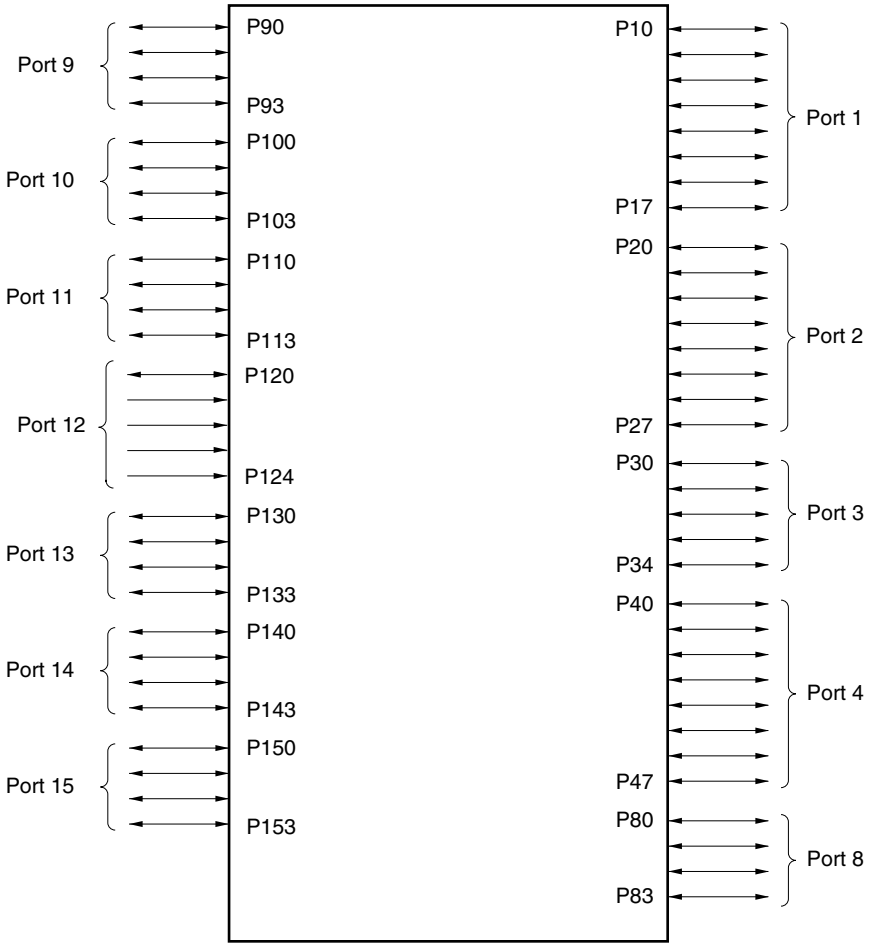
Power Supply	Corresponding Pins
AV_{REF}[Note]	P20 to P27
V_{DD}	Port pins other than P20 to P27

Note μPD78F048x and 78F049x only. The power supply is V_{DD} with μPD78F047x.

78K0/LF3 products are provided with the ports shown in Figure 4-1, which enable variety of control operations. The functions of each port are shown in Table 4-2.

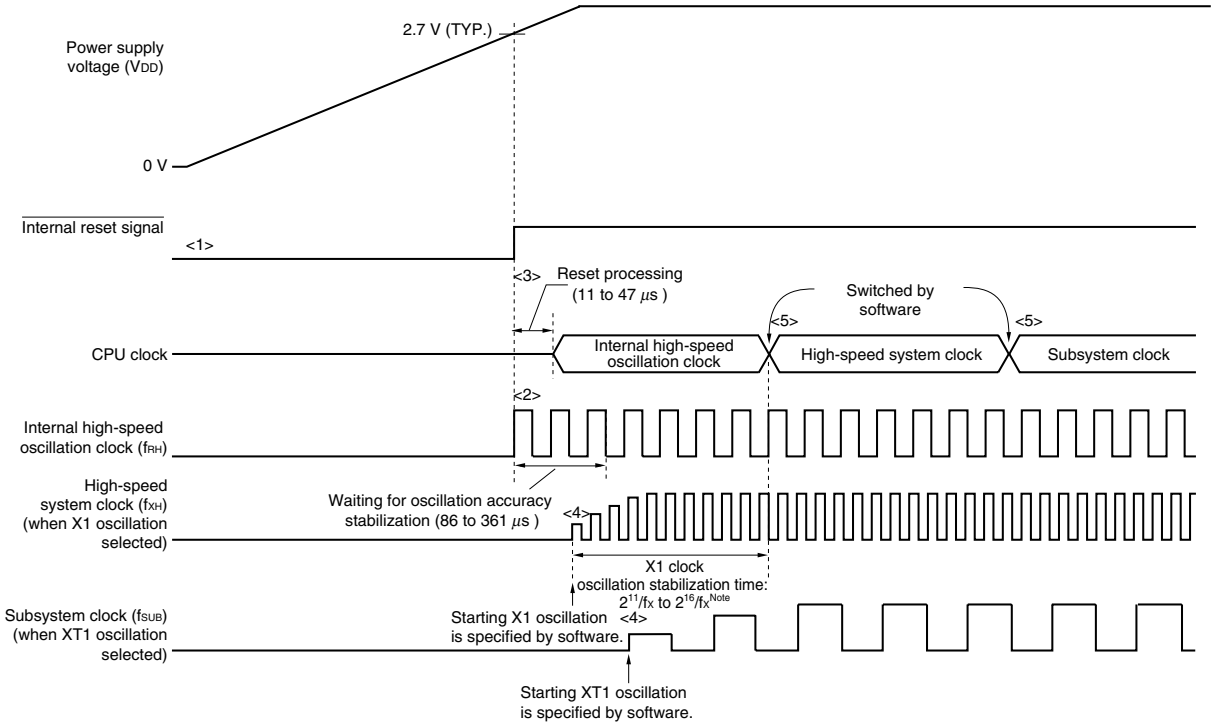
In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-1. Port Types



Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (see **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**, and **(4)** in **5.6.3 Example of controlling subsystem clock**).

Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On (When 2.7 V/1.59 V POC Mode Is Set (Option Byte: POCMODE = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 2.7 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Note When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

<R> **Cautions 1. A voltage oscillation stabilization time of 1.93 to 5.39 ms is required after the supply voltage reaches 1.59 V (TYP.). If the time the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) is within 1.93 to 5.39 ms, a power supply stabilization wait time of 0 to 5.39 ms occurs automatically before reset processing, and the reset processing time becomes 19 to 80 μs.**

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

6.4.2 Square wave output operation

When 16-bit timer/event counter 00 operates as an interval timer (see **6.4.1**), a square wave can be output from the TO00 pin by setting the 16-bit timer output control register 00 (TOC00) to 03H.

When TMC003 and TMC002 are set to 11 (count clear & start mode entered upon a match between TM00 and CR000), the counting operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H, an interrupt signal (INTTM000) is generated, and TO00 output is inverted. This TO00 output that is inverted at fixed intervals enables TO00 to output a square wave.

Remarks 1. For the setting of I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 6-16. Block Diagram of Square Wave Output Operation

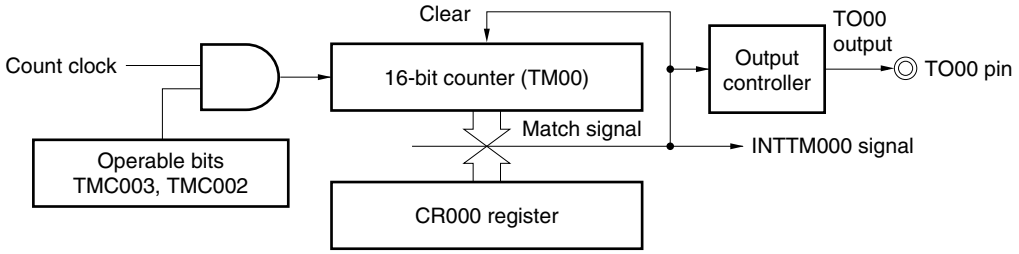


Figure 6-17. Basic Timing Example of Square Wave Output Operation

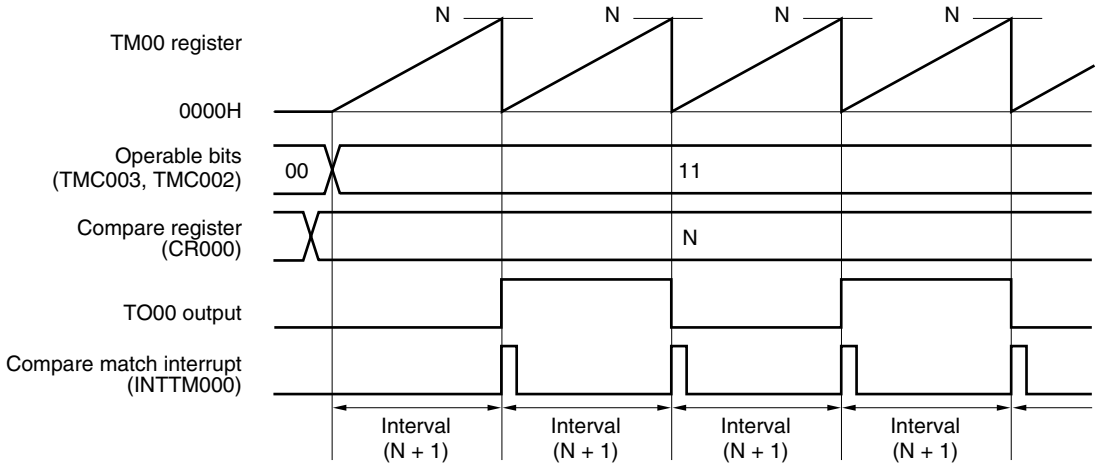
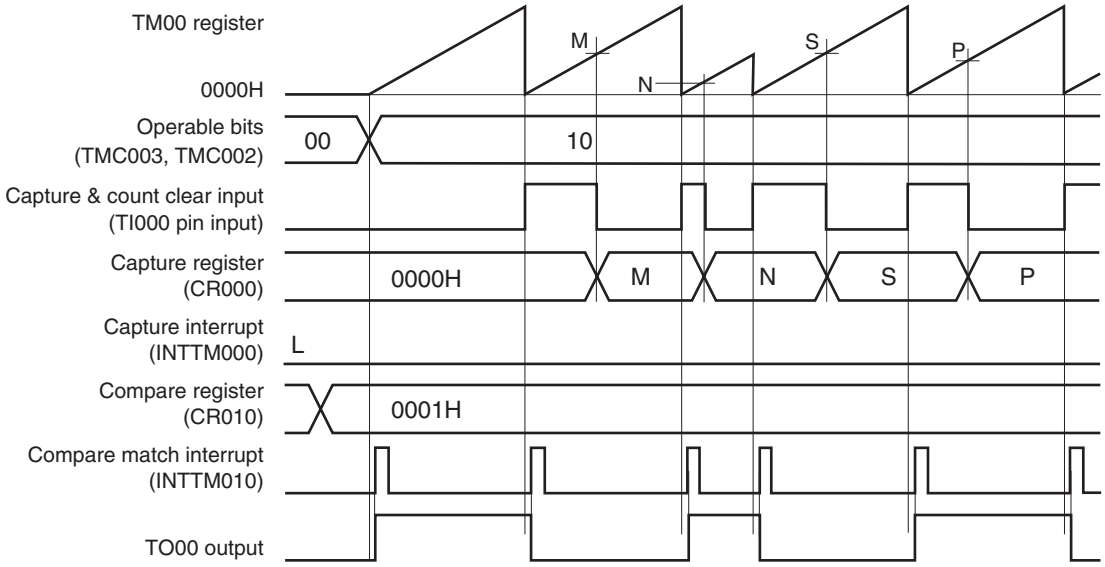


Figure 6-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00, = 03H, TMC00 = 08H, CR010 = 0001H



This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

(2) Cautions for input enable control for TI52 pin

The input enable control signal (TMH2 output signal) for the TI52 pin is synchronized by the TI52 pin input clock, as described in **Figure 6-54 Configuration Diagram of External 24-bit Event Counter** and **Figure 6-55 Operation Timing of External 24-bit Event Counter**. Thus, when the counter is operated as an external event counter, an error up to one count may be caused.

(3) Cautions for 16-bit timer/event counter 00 count up during external 24-bit event counter operation

16-bit timer/event counter 00 has an internal synchronization circuit to eliminate noise when starting operation, and the first clock immediately after operation start is not counted.

When using the counter as a 24-bit counter, by setting 16-bit timer/event counter 00 and 8-bit timer/event counter 52 as the higher and lower timer and connecting them in cascade, the interrupt request flag of 8-bit timer/event counter 52 which is the lower timer must be checked as described below, in order to accurately read the 24-bit count values.

- If TMIF52 = 1 when TM52 and TM00 are read:

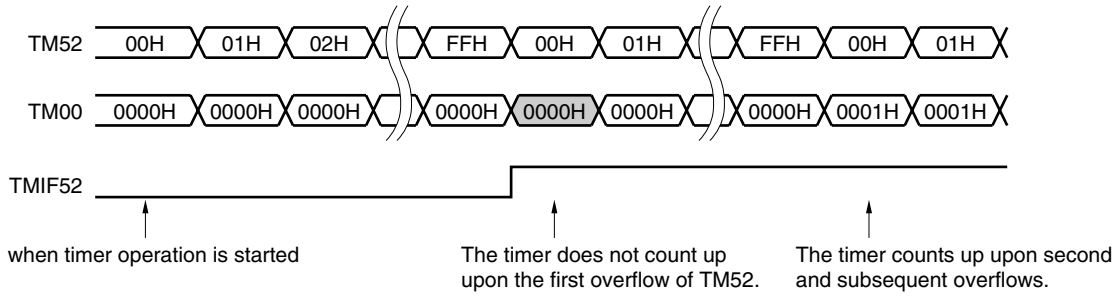
  The actual TM00 count value is “read value of TM00 + 1”.

- If TMIF52 = 0 when TM52 and TM00 are read:

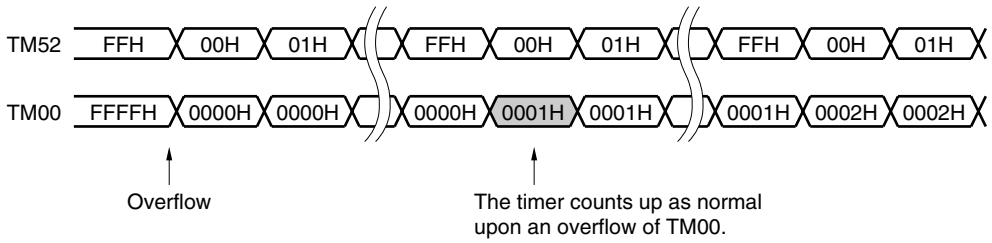
  The read value is the correct value.

This phenomenon of 16-bit timer/event counter 00 occurs only when operation is started. A count delay will not occur when 16-bit timer/event counter 00 overflows and the count is restarted from 0000H, since synchronization has already been implemented.

<When starting operation>



<Overflow of higher timer>



6.5 Special Use of TM00

6.5.1 Rewriting CR010 during TM00 operation

In principle, rewriting CR000 and CR010 of the 78K0/LF3 when they are used as compare registers is prohibited while TM00 is operating (TMC003 and TMC002 = other than 00).

However, the value of CR010 can be changed, even while TM00 is operating, using the following procedure if CR010 is used for PPG output and the duty factor is changed (when setting CR010 to a smaller or larger value than the current value, rewrite the CR010 value immediately after a match between CR010 and TM00 or between CR000 and TM00. When CR010 is rewritten immediately before a match between CR010 and TM00 or between CR000 and TM00, an unexpected operation may be performed).

Procedure for changing value of CR010

<1> Disable interrupt INTTM010 (TMMK010 = 1).
<2> Disable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 0).
<3> Change the value of CR010.
<4> Wait for one cycle of the count clock of TM00.
<5> Enable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 1).
<6> Clear the interrupt flag of INTTM010 (TMIF010 = 0) to 0.
<7> Enable interrupt INTTM010 (TMMK010 = 0).

Remark For TMIF010 and TMMK010, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

6.5.2 Setting LVS00 and LVR00

(1) Usage of LVS00 and LVR00

LVS00 and LVR00 are used to set the default value of the TO00 output and to invert the timer output without enabling the timer operation (TMC003 and TMC002 = 00). Clear LVS00 and LVR00 to 00 (default value: low-level output) when software control is unnecessary.

LVS00	LVR00	Timer Output Status
0	0	Not changed (low-level output)
0	1	Cleared (low-level output)
1	0	Set (high-level output)
1	1	Setting prohibited

CHAPTER 9 REAL-TIME COUNTER

9.1 Functions of Real-Time Counter

The real-time counter has the following features.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 1 month to 0.5 seconds)
- Alarm interrupt function (alarm: week, hour, minute)
- Interval interrupt function
- Pin output function of 1 Hz
- Pin output function of 512 Hz or 16.384 kHz or 32.768 kHz

9.2 Configuration of Real-Time Counter

The real-time counter includes the following hardware.

Table 9-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter clock selection register (RTCCL)
	Real-time counter control register 0 (RTCC0)
	Real-time counter control register 1 (RTCC1)
	Real-time counter control register 2 (RTCC2)
	Sub-count register (RSUBC)
	Second count register (SEC)
	Minute count register (MIN)
	Hour count register (HOUR)
	Day count register (DAY)
	Week count register (WEEK)
	Month count register (MONTH)
	Year count register (YEAR)
	Watch error correction register (SUBCUD)
	Alarm minute register (ALARMWM)
	Alarm hour register (ALARMWH)
	Alarm week register (ALARMWW)

14.3 Registers Controlling Serial Interface UART0

Serial interface UART0 is controlled by the following six registers.

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)

(1) Asynchronous serial interface operation mode register 0 (ASIM0)

This 8-bit register controls the serial communication operations of serial interface UART0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Figure 14-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (1/2)

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock.

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission.

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception.

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

15.3 Registers Controlling Serial Interface UART6

Serial interface UART6 is controlled by the following twelve registers.

- Asynchronous serial interface operation mode register 6 (ASIM6)
- Asynchronous serial interface reception error status register 6 (ASIS6)
- Asynchronous serial interface transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Asynchronous serial interface control register 6 (ASICL6)
- Input switch control register (ISC)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)
- Port mode register 11 (PM11)
- Port register 11 (P11)

(1) Asynchronous serial interface operation mode register 6 (ASIM6)

This 8-bit register controls the serial communication operations of serial interface UART6.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Remark ASIM6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 15-5. Format of Asynchronous Serial Interface Operation Mode Register 6 (ASIM6) (1/2)

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock

TXE6	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission

RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception

Notes 1. The output of the TxD6 pin goes high level and the input from the RxD6 pin is fixed to the high level when POWER6 = 0 during transmission.

2. Asynchronous serial interface reception error status register 6 (ASIS6), asynchronous serial interface transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6), and receive buffer register 6 (RXB6) are reset.

(10) Port mode register 11 (PM11)

This register sets port 11 input/output in 1-bit units.

When using the P112/SEG18/TxD6 pin for serial interface data output, clear PM112 to 0 and set the output latch of P112 to 1.

When using the P113/SEG19/RxD6 pin for serial interface data input, set PM113 to 1. The output latch of P113 at this time may be 0 or 1.

PM11 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

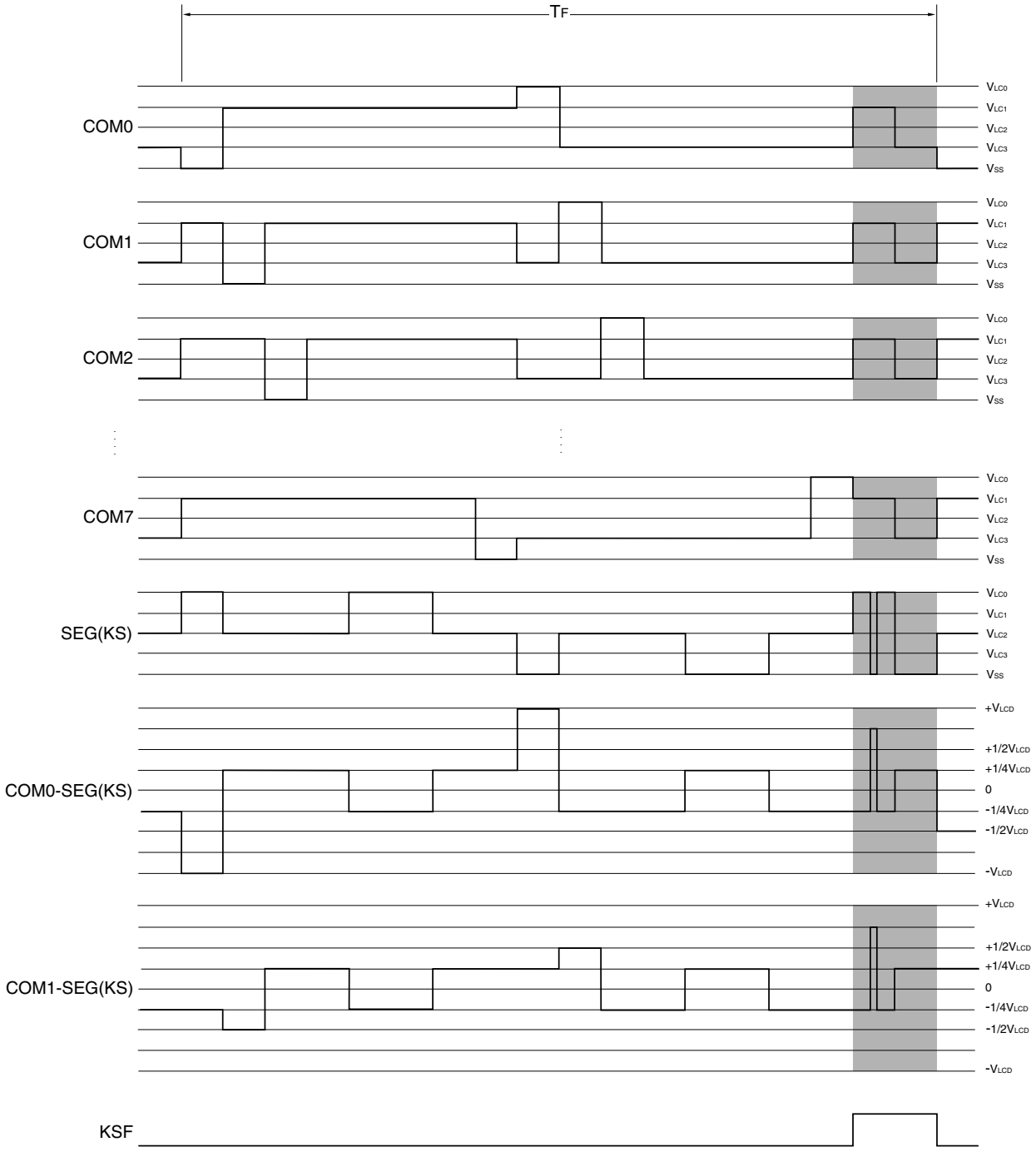
Figure 15-14. Format of Port Mode Register 11 (PM11)

Address: FF2BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM11	1	1	1	1	PM113	PM112	PM111	PM110

PM11n	P11n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

<Key identification>



Shaded sections: Segment key scan output period

Remark During key identification, the residual charge of the LCD panel can be eliminated by outputting a signal with an inverted relationship between its first half and latter half.

20.4.8 Compare register setting

This remote controller receiver has the following 11 types of compare registers.

- Remote controller receive GPLS compare register (RMGPLS)
- Remote controller receive GPLL compare register (RMGPLL)
- Remote controller receive GPHS compare register (RMGPHS)
- Remote controller receive GPHL compare register (RMGPHL)
- Remote controller receive DLS compare register (RMDLS)
- Remote controller receive DLL compare register (RMDLL)
- Remote controller receive DH0S compare register (RMDH0S)
- Remote controller receive DH0L compare register (RMDH0L)
- Remote controller receive DH1S compare register (RMDH1S)
- Remote controller receive DH1L compare register (RMDH1L)
- Remote controller receive end width select register (RMER)

Use formulas (1) to (3) below to set the value of each compare register.

Making allowances for tolerance enables a normal reception operation, even if the RIN input waveform is RIN_1 or RIN_2 shown in Figure 20-12 due to the effect of noise.

Cautions 1. Always set each compare register while remote controller reception is disabled (RMEN = 0).

2. Set the set values so that they satisfy all the following four conditions.

- **RMGPLS < RMGPLL**
- **RMGPHS < RMGPHL**
- **RMDLS < RMDLL**
- **RMDH0S < RMDH0L ≤ RMDH1S < RMDH1L**

Figure 26-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFBEH After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from external input pin (EXLVI)

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when operation is disabled • LVISEL = 1: Input voltage from external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. This bit is cleared to 00H upon a reset other than an LVI reset.

2. Bit 0 is read-only.

3. LVION, LVIMD, and LVISEL are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

4. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 μs (MAX.)) from when LVION is set to 1 until operation is stabilized. After operation has stabilized, 200 μs (MIN.) are required from when a state below LVI detection voltage has been entered, until LVIF is set (1).

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. Input voltage from external input pin (EXLVI) must be EXLVI < V_{DD}.

(e) AUTOCSI (Master mode, $\overline{SCKA0}$... internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKA0}$ cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
		1.8 V ≤ V_{DD} < 2.7 V		1800			ns
$\overline{SCKA0}$ high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2 - 50$			ns
		2.7 V ≤ V_{DD} < 4.0 V		$t_{KCY3}/2 - 100$			ns
		1.8 V ≤ V_{DD} < 2.7 V		$t_{KCY3}/2 - 200$			ns
SIA0 setup time (to $\overline{SCKA0}$↑)	t_{SIK3}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		200			ns
SIA0 hold time (from $\overline{SCKA0}$↑)	t_{KSI3}			300			ns
Delay time from $\overline{SCKA0}$↓ to SOA0 output	t_{KSO3}	C = 100 pF Note	4.0 V ≤ V_{DD} ≤ 5.5 V			200	ns
			2.7 V ≤ V_{DD} < 4.0 V			300	ns
			1.8 V ≤ V_{DD} < 2.7 V			400	ns

Note C is the load capacitance of the $\overline{SCKA0}$ and SOA0 output lines.

(f) AUTOCSI (Slave mode, $\overline{SCKA0}$... external clock input)

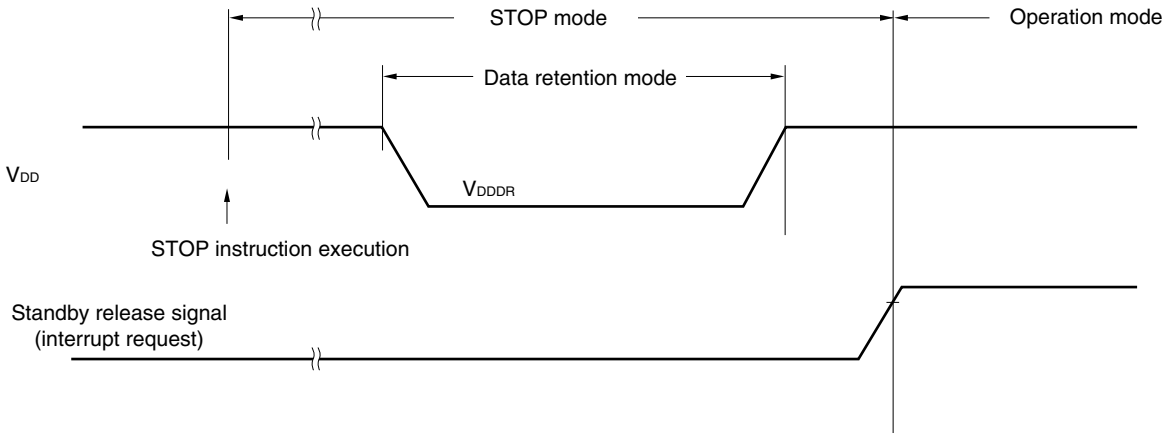
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKA0}$ cycle time	t_{KCY4}	4.0 V ≤ V_{DD} ≤ 5.5 V		600			ns
		2.7 V ≤ V_{DD} < 4.0 V		1200			ns
		1.8 V ≤ V_{DD} < 2.7 V		1800			ns
$\overline{SCKA0}$ high-/low-level width	t_{KH4}, t_{KL4}	4.0 V ≤ V_{DD} ≤ 5.5 V		300			ns
		2.7 V ≤ V_{DD} < 4.0 V		600			ns
		1.8 V ≤ V_{DD} < 2.7 V		900			ns
SIA0 setup time (to $\overline{SCKA0}$↑)	t_{SIK4}	4.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
SIA0 hold time (from $\overline{SCKA0}$↑)	t_{KSI4}			2/f_W+100			ns
Delay time from $\overline{SCKA0}$↓ to SOA0 output	t_{KSO4}	C = 100 pF Note	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_W+100	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_W+200	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_W+300	ns
$\overline{SCKA0}$ rise/fall time	t_{R4}, t_{F4}					1000	ns

Note C is the load capacitance of the SOA0 output line.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

• Basic characteristics

Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}					4.5	11.0	mA
Erase time[Note 1, 2]	All block	T_{eraca}					20	200	ms
	Block unit	T_{erasa}					20	200	ms
Write time (in 8-bit units)[Note 1]		T_{wrwa}					10	100	μs
<R> Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite[Note 3]	When a flash memory programmer is used, and the libraries provided by NEC Electronics are used	Retention: 15 years	1000			Times
				When the EEPROM emulation libraries provided by NEC Electronics are used, and the rewritable ROM size is 4 KB	Retention: 3 years[Note 4]	10000			Times

<R> **Notes 1.** Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP5, is used and the rewrite time during self programming, see **Tables 28-12** and **28-13**.

2. The prewrite time before erasure and the erase verify time (writeback time) are not included.

3. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

<R> **4.** Data retention is guaranteed for three years after data has been written. If rewriting has been performed, data retention is guaranteed for another three years thereafter.

Remark f_{XP}: Main system clock oscillation frequency

(2/3)

Edition	Description	Applied to:
2nd edition	Change of **Figure 14-1 Block Diagram of Serial Interface UART0**	**CHAPTER 14 SERIAL INTERFACE UART0**
	Addition of **Note 1** to **Figure 14-4 Format of Baud Rate Generator Control Register 0 (BRGC0)**	
	Change of **14.3 (5) Port mode register 1 (PM1)**	
	Change of **Table 14-2. Relationship Between Register Settings and Pins**	
	Addition of **Notes 1** and **2** to **Table 14-4 Set Value of TPS01 and TPS00**	
	Change of explanation in **15.1 Functions of Serial Interface UART6**	**CHAPTER 15 SERIAL INTERFACE UART6**
	Change of **Figure 15-4 Block Diagram of Serial Interface UART6**	
	Addition of **Notes 1** and **2** to **Figure 15-8 Format of Clock Selection Register 6 (CKSR6)**	
	Change of **15.3 (9) Port mode register 1 (PM1)**	
	Change of **(a)** in **Table 15-2. Relationship Between Register Settings and Pins**	
	Addition of **Notes 1**, **2**, and **3** to **Table 15-4 Set Value of TPS63 to TPS60**	
	Change of **Figure 16-1. Block Diagram of Serial Interface CSI10**	**CHAPTER 16 SERIAL INTERFACE CSI10**
	Addition of **Notes 1** and **2** to **Figure 16-3 Format of Serial Clock Selection Register 10 (CSIC10)**	
	Change of **Figure 17-1. Block Diagram of Serial Interface CSIA0**	**CHAPTER 17 SERIAL INTERFACE CSIA0**
	Addition of **Notes 2** and **3** to **Figure 17-3. Format of Serial Status Register 0 (CSIS0)**	
	Change of **Note 2** in **18.3 (2) LCD display mode register (LCDM)**	**CHAPTER 18 LCD CONTROLLER/DRIVER**
	Change of **Note** in **18.4 Setting LCD Controller/Driver**	
	Addition of **Notes 1** and **2** to **Figure 19-5. Format of MCG Control Register 1 (MC0CTL1)**	**CHAPTER 19 MANCHESTER CODE GENERATOR**
	Addition of **Notes 1** and **2** to **19.4.2 (b) MCG control register 1 (MC0CTL1)**	
	Change of **Note 4** in **Table 21-1. Interrupt Source List**	**CHAPTER 21 INTERRUPT FUNCTIONS**
	Change of **Note 2** in and addition of **Notes 4**, **5**, and **6** to **Table 21-2 Flags Corresponding to Interrupt Request Sources**	
	Change of **Caution 1** in **Figure 22-2 Format of Key Return Mode Register (KRM)**	**CHAPTER 22 KEY INTERRUPT FUNCTION**
	Addition of explanation to **Caution 3** in **23.1.1 Standby function**	**CHAPTER 23 STANDBY FUNCTION**
	Change of explanation in **26.3 (1) Low-voltage detection register (LVIM)**	**CHAPTER 26 LOW-VOLTAGE DETECTOR**
	Addition of **Notes 1** and **4** and **Cautions 3** and **4** to **Figure 26-2 Format of Low-Voltage Detection Register (LVIM)**	
	Change of explanation in **26.3 (2) Low-voltage detection level selection register (LVIS)**	
	Addition of **Note** and **Caution 4** to **Figure 26-3 Format of Low-Voltage Detection Level Selection Register (LVIS)**	
	Addition of **Note 3** to **Figure 26-7 Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Supply Voltage (V_{DD}))**	
	Addition of **Note 3** to **Figure 26-8 Timing of Low-Voltage Detector Interrupt Signal Generation (Detects Level of Input Voltage from External Input Pin (EXLVI))**	
	Change of **Figure 26-9 Example of Software Processing After Reset Release**	