Renesas Electronics America Inc - UPD78F0485GC-GAD-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0485gc-gad-ax

(2) Control mode

P140 to P143 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

<R> **(a) SEG24 (KS0) to SEG27 (KS3)**

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.12 P150 to P153 (port 15)

P150 to P153 function as a 4-bit I/O port. These pins also function as pins for segment signal output and simultaneous output of segment key source signal for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

(1) Port mode

P150 to P153 function as a 4-bit I/O port. P150 to P153 can be set to input or output port in 1-bit units using port mode register 15 (PM15). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 15 (PU15).

(2) Control mode

P150 to P153 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

<R> **(a) SEG28 (KS4) to SEG31 (KS7)**

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.13 AV_{REF} (μPD78F048x and 78F049x only)

This is the 10-bit successive approximation type A/D converter reference voltage input pin and the positive power supply pin of port 2 and 16-bit $\Delta\Sigma$ type A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note When one or more of the pins of port 2 is used as the digital port pins or for segment output, make AV_{REF} the same potential as V_{DD}.

2.2.14 AV_{SS} (μPD78F048x and 78F049x only)

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

2.2.15 COM0 to COM7

These pins are the common signal output pins for the LCD controller/driver.

2.2.16 V_{LC0} to V_{LC3}

These pins are the power supply voltage pins for driving the LCD.

2.2.17 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

4.2.1 Port 1

Port 1 is an 8-bit I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

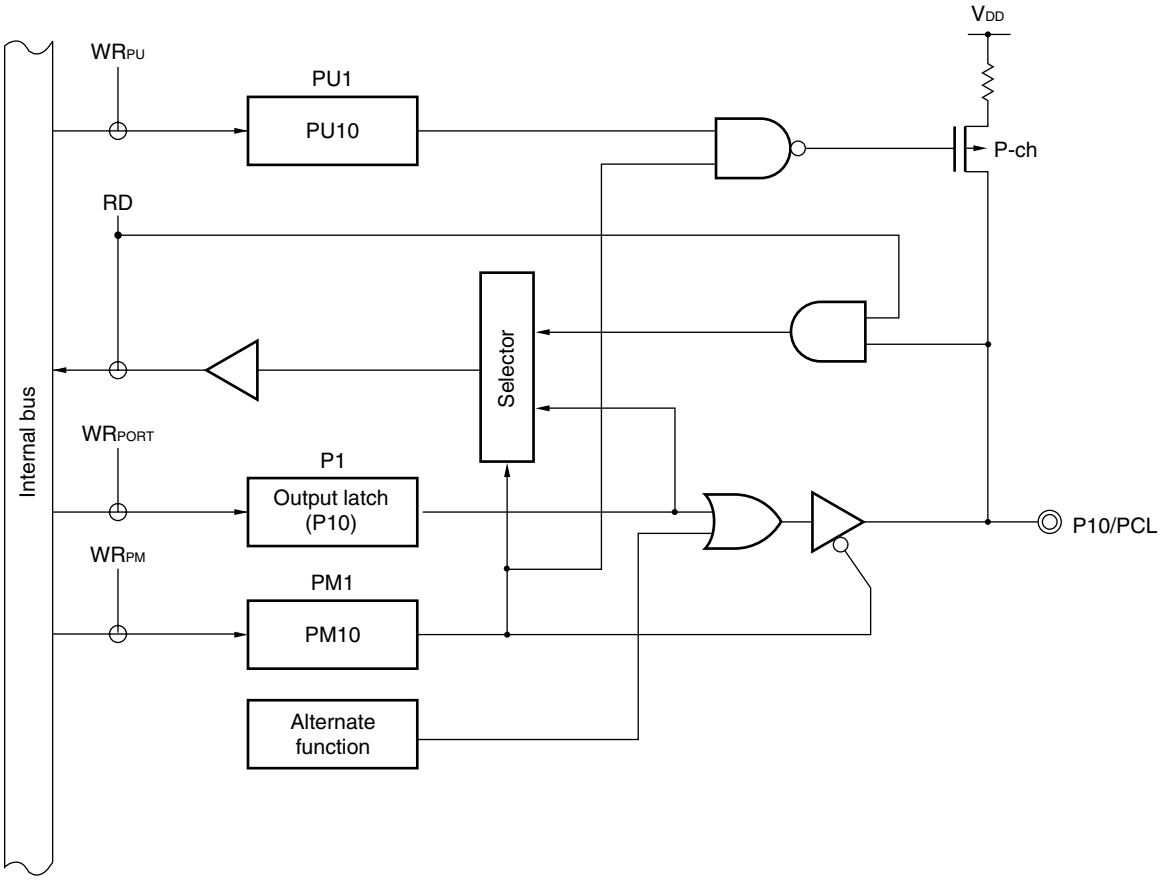
This port can also be used for serial clock I/O, serial interface data I/O, and maskable external interrupt input.

Reset signal generation sets port 1 to input mode.

Figures 4-2 to 4-7 show block diagrams of port 1.

Caution To use P11/$\overline{\text{SCK10}}$, P12/SI10/RxD0, and P13/SO10/TxD0 as general-purpose ports, set serial operation mode register 10 (CSIM10) and serial clock selection register 10 (CSIC10) to the default status (00H).

Figure 4-2. Block Diagram of P10



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Notes 1. μPD78F048x and 78F049x only.

2. The functions of the P20/ANI0/DS0−, P21/ANI1/DS0+, P22/ANI2/DS1−, P23/ANI3/DS1+, P24/ANI4/DS2−, P25/ANI5/DS2+, P26/ANI6/REF−, and P27/ANI7/REF+ pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), analog input channel specification register (ADS), and ΔΣ A/D converter mode register 0 (ADDCTL0).

Table 4-6. Setting Functions of P20/SEG39[Note 1]/ANI0[Note 2]/DS0−[Note 3] to P27/SEG32[Note 1]/ANI7[Note 2]/REF+[Note 3] Pins

PF2[Note 1]	ADPC0	PM2	ADS	ADDCTL0	P20/SEG39[Note 1]/ANI0[Note 2]/DS0−[Note 3] to P27/SEG32[Note 1]/ANI7[Note 2]/REF+[Note 3] Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Does not select DSn±.	Analog input (not to be converted)
			Selects ANI.	Does not select DSn±.	Analog input (to be converted by successive approximation type A/D converter)
			Does not select ANI.	Selects DSn±.	Analog input (to be converted by 16-bit ΔΣ type A/D converter)
			Selects ANI.	Selects DSn±.	Setting prohibited
		Output mode	−		Setting prohibited
	Digital I/O selection	Input mode	−		Digital input
		Output mode	−		Digital output
SEG output selection[Note 1]	−	−	−		Segment output[Note 1]

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

3. μPD78F049x only.

Remark n = 0 to 2

3. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are Input port pins).

4. Targeted at registers corresponding to each port.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. Input enable of TM52 via TMH2 can be controlled by setting ISC2 = 1.

7. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

8. μPD78F049x only.

9. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

10. Set PF13 = 0 when using as port function.

11. Set PF16 = 0 when using as port function.

12. μPD78F047x and 78F048x only.

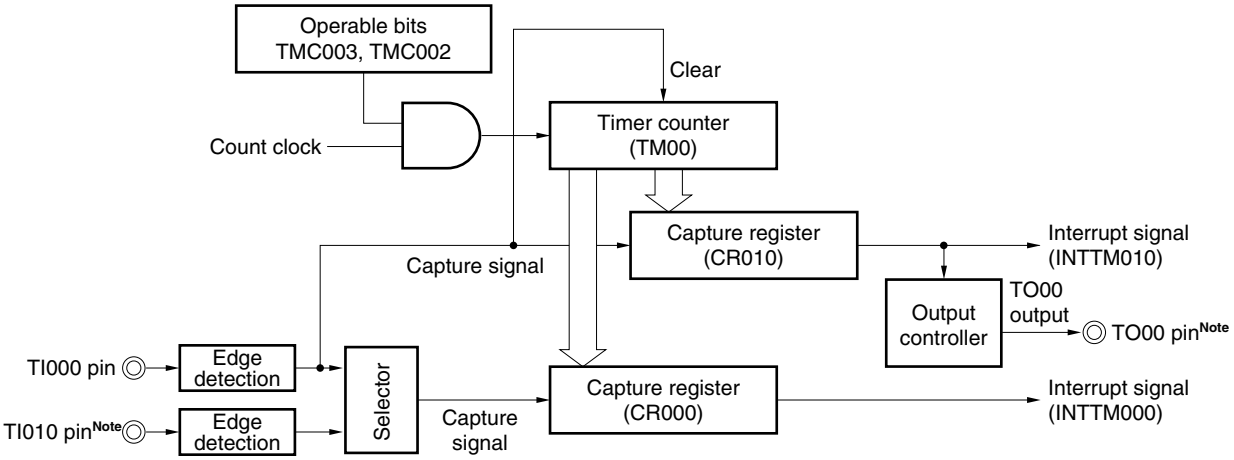
Remarks 1. ×: Don't care
−: Does not apply.
PM××: Port mode register
P××: Port output latch

2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

3. X1, X2 pins can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For detail, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION.**

(4) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: capture register, CR010: capture register)

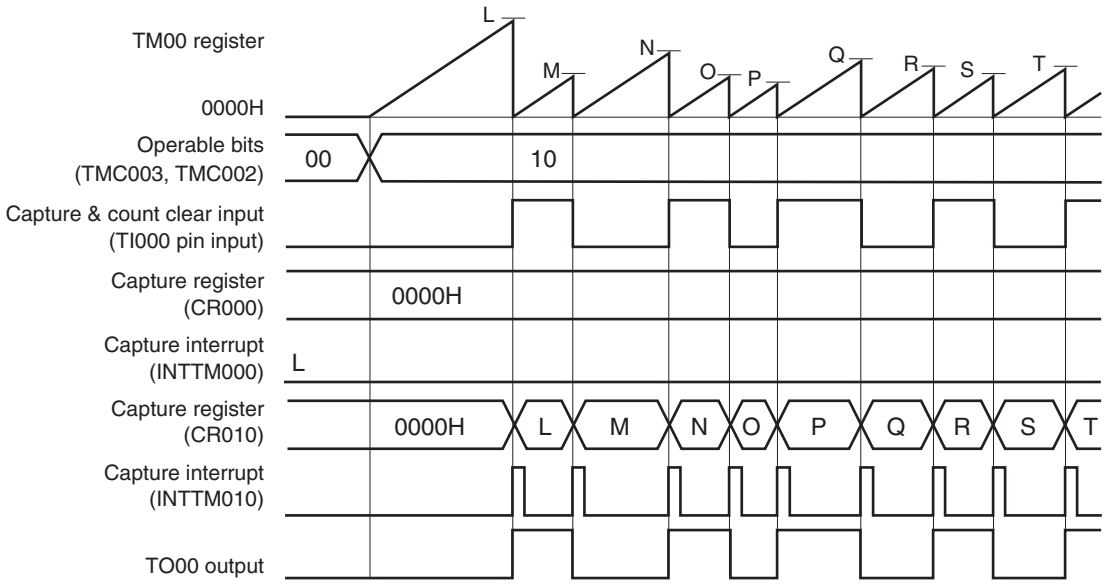
Figure 6-29. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register)



Note The timer output (TO00) cannot be used when detecting the valid edge of the TI010 pin is used.

Figure 6-30. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (1/3)

(a) TOC00 = 13H, PRM00 = 30H, CRC00 = 05H, TMC00 = 0AH

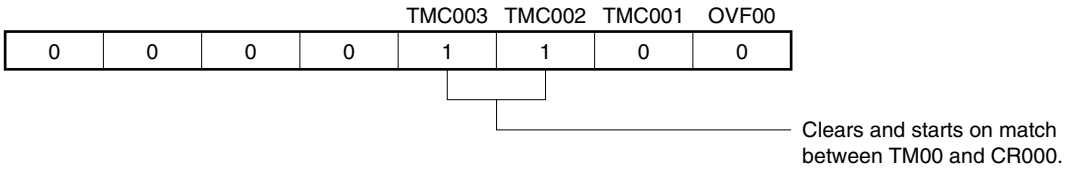


This is an application example where the count value is captured to CR010, TM00 is cleared, and the TO00 output is inverted when the rising or falling edge of the TI000 pin is detected.

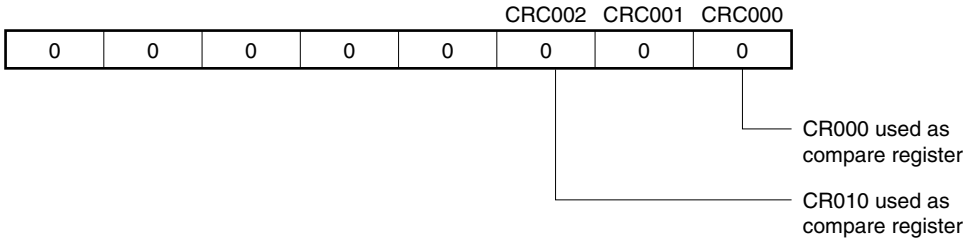
When the edge of the TI010 pin is detected, an interrupt signal (INTTM000) is generated. Mask the INTTM000 signal when it is not used.

Figure 6-42. Example of Register Settings for PPG Output Operation

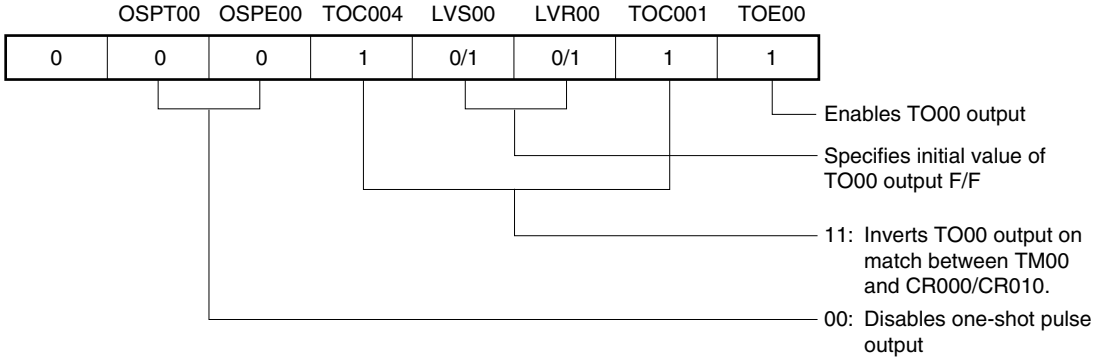
(a) 16-bit timer mode control register 00 (TMC00)



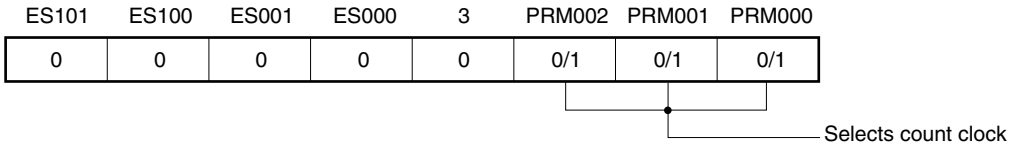
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

An interrupt signal (INTTM000) is generated when the value of this register matches the count value of TM00.

<R> The count value of TM00 is cleared.

(g) 16-bit capture/compare register 010 (CR010)

An interrupt signal (INTTM010) is generated when the value of this register matches the count value of TM00.

The count value of TM00 is not cleared.

Caution Set values to CR000 and CR010 such that the condition 0000H ≤ CR010 < CR000 ≤ FFFFH is satisfied.

Figure 6-52. Example of Register Settings for Pulse Width Measurement (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

This register is used as a capture register. Either the TI000 or TI010 pin is selected as a capture trigger. When a specified edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

This register is used as a capture register. The signal input to the TI000 pin is used as a capture trigger. When the capture trigger is detected, the count value of TM00 is stored in CR010.

7.4.2 Operation as external event counter

The external event counter counts the number of external clock pulses to be input to the TI5n pin by 8-bit timer counter 5n (TM5n).

TM5n is incremented each time the valid edge specified by timer clock selection register 5n (TCL5n) is input. Either the rising or falling edge can be selected.

When the TM5n count value matches the value of 8-bit timer compare register 5n (CR5n), TM5n is cleared to 0 and an interrupt request signal (INTTM5n) is generated.

Whenever the TM5n value matches the value of CR5n, INTTM5n is generated.

Setting

<1> Set each register.

- Set the port mode register (PM44, PM43, or PM34)[Note] to 1.
- TCL5n: Select TI5n pin input edge.
  TI5n pin falling edge → TCL5n = 00H
  TI5n pin rising edge → TCL5n = 01H
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on match of TM5n and CR5n, disable the timer F/F inversion operation, disable timer output.
  (TMC5n = 0000××00B × = Don't care)

<2> When TCE5n = 1 is set, the number of pulses input from the TI5n pin is counted.

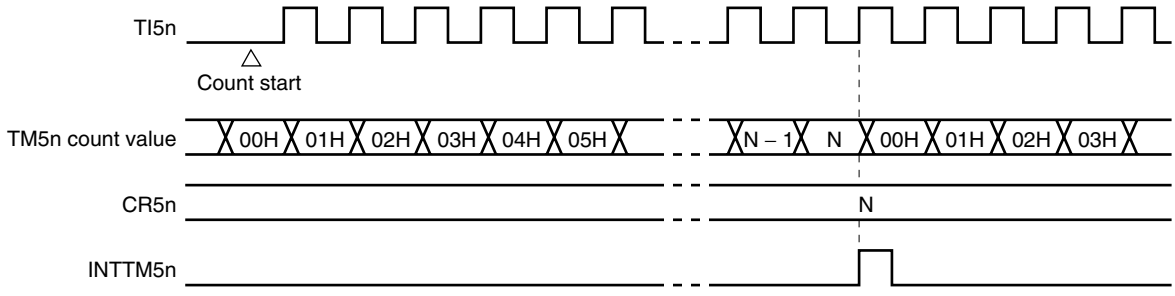
<3> When the values of TM5n and CR5n match, INTTM5n is generated (TM5n is cleared to 00H).

<4> After these settings, INTTM5n is generated each time the values of TM5n and CR5n match.

Note 8-bit timer/event counter 50: PM44
8-bit timer/event counter 51: PM43
8-bit timer/event counter 52: PM34

Remark For how to enable the INTTM5n signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

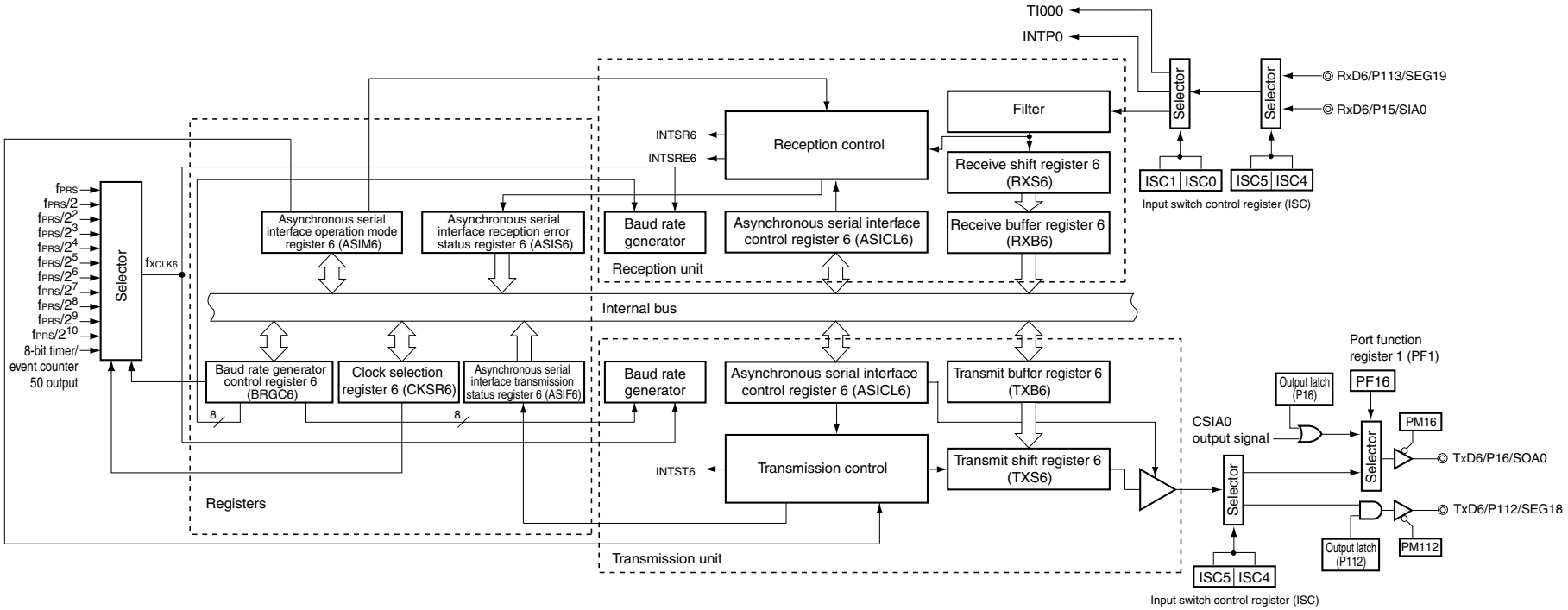
Figure 7-16. External Event Counter Operation Timing (with Rising Edge Specified)



Remark 1. 8-bit timer/event counter 52 (TM52) can be used as an external 24-bit event counter, by connecting it with 16-bit timer/event counter (TM00) in cascade. Also, input enable of TM52 can be controlled via TMH2. For details, see **6.4.9 External 24-bit event counter operation**.

2. N = 00H to FFH, n = 0 to 2

Figure 15-4. Block Diagram of Serial Interface UART6



(8) Port function register 1 (PF1)

This register sets the pin functions of P16/SOA0/TxD6 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PF1 to 00H.

Figure 15-12. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PF1	0	PF16	0	0	PF13	0	0	0

PF16	Port (P16), CSIA0, and UART6 output specification
0	Used as P16 or SOA0
1	Used as TxD6

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

(9) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P16/SOA0/TxD6 pin for serial interface data output, clear PM16 to 0. The output latch of P16 at this time may be 0 or 1.

When using the P15/SIA0/RxD6 pin for serial interface data input, set PM15 to 1. The output latch of P15 at this time may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 15-13. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(5) Automatic data transfer address point specification register 0 (ADTP0)

This is an 8-bit register used to specify the buffer RAM address that ends transfer during automatic data transfer (bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 1).

This register can be set by an 8-bit memory manipulation instruction. However, during transfer (TSF0 = 1), rewriting ADTP0 is prohibited.

In the 78K0/LF3, 00H to 1FH can be specified because 32 bytes of buffer RAM are incorporated.

Example When ADTP0 is set to 07H
8 bytes of FA00H to FA07H are transferred.

In repeat transfer mode (bit 5 (ATM0) of CSIMA0 = 1), transfer is performed repeatedly up to the address specified with ADTP0.

Example When ADTP0 is set to 07H (repeat transfer mode)
Transfer is repeated as FA00H to FA07H, FA00H to FA07H, … .

Figure 17-6. Format of Automatic Data Transfer Address Point Specification Register 0 (ADTP0)

Address: FF94H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTP0	0	0	0	ADTP04	ADTP03	ADTP02	ADTP01	ADTP00

Caution Be sure to clear bits 7 to 5 to "0".

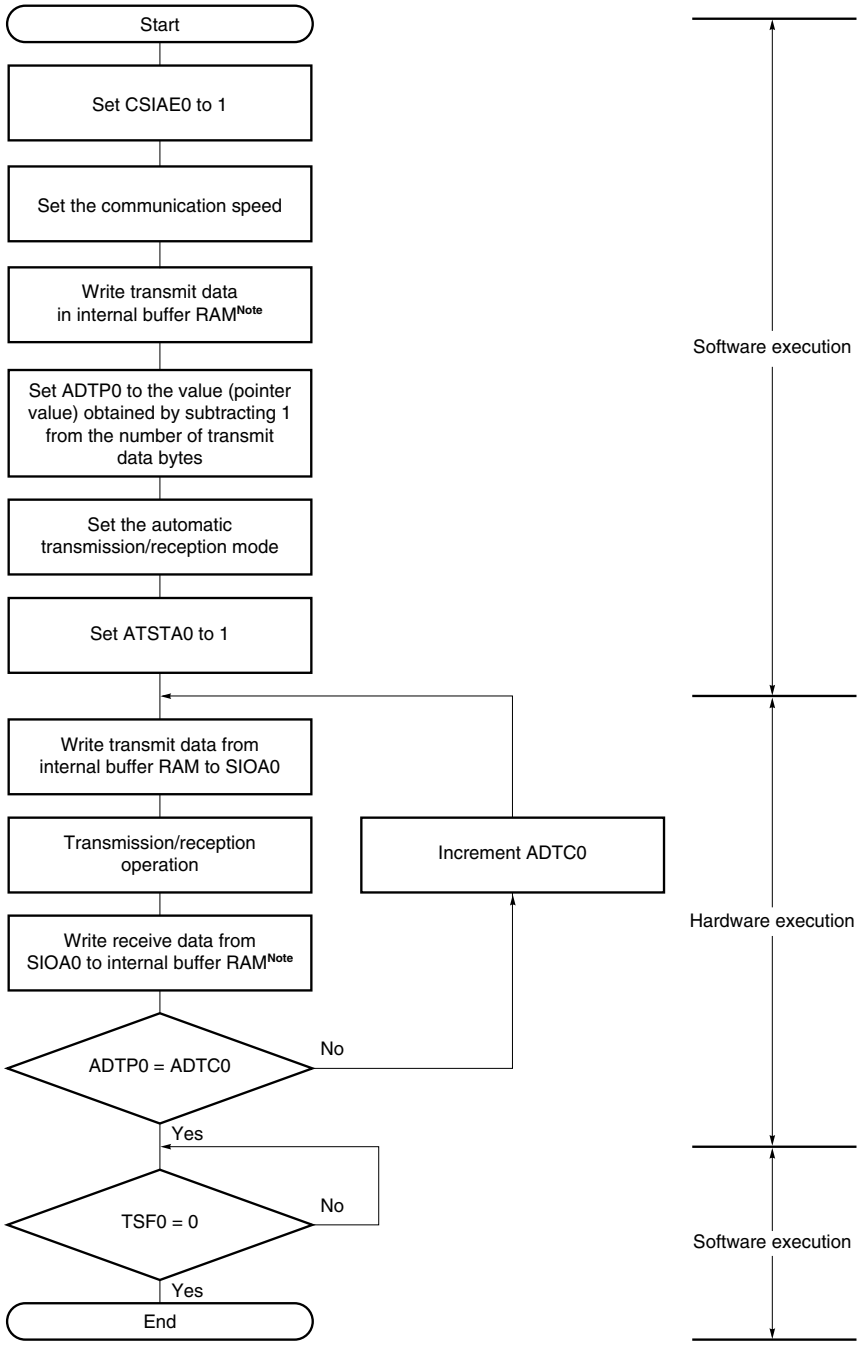
The relationship between transfer end buffer RAM address values and ADTP0 setting values is shown below.

Table 17-2. Relationship Between Transfer End Buffer RAM Address Values and ADTP0 Setting Values

Transfer End Buffer RAM Address Value	ADTP0 Setting Value
FAxxH	xxH

Remark xx: 00 to 1F

Figure 17-15. Automatic Transmission/Reception Mode Flowchart



CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ADTP0: Automatic data transfer address point specification register 0
ADTI0: Automatic data transfer interval specification register 0
ATSTA0: Bit 0 of serial trigger register 0 (CSIT0)
SIOA0: Serial I/O shift register 0
ADTC0: Automatic data transfer address count register 0
TSF0: Bit 0 of serial status register 0 (CSIS0)

Note A wait state may be generated when data is written to the buffer RAM. For details, see **CHAPTER 34 CAUTIONS FOR WAIT**.

(b) Automatic transmission mode

In this mode, the specified data is transmitted in 8-bit unit.

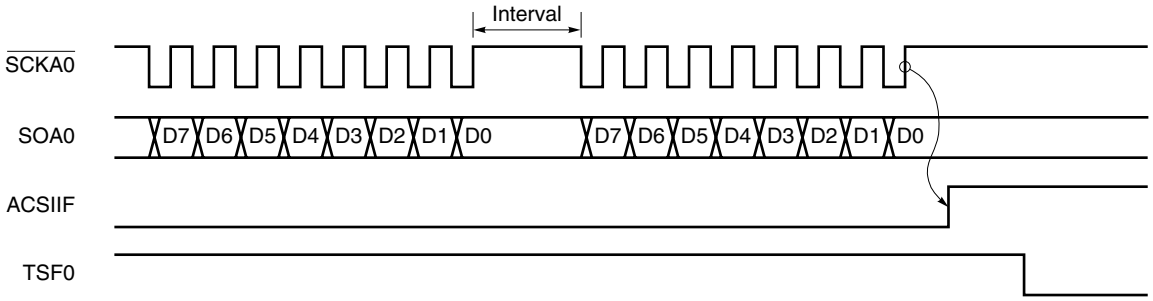
Serial communication is started when bit 0 (ATSTA0) of serial trigger register 0 (CSIT0) is set to 1 while bit 7 (CSIAE0), bit 6 (ATE0), and bit 3 (TXEA0) of serial operation mode specification register 0 (CSIMA0) are set to 1.

When the final byte has been transmitted, an interrupt request flag (ACSIIF) is set. The termination of automatic transmission can also be judged by bit 0 (TSF0) of serial status register 0 (CSIS0).

If a receive operation, busy control and strobe control are not executed, the SIA0/P15 pin can be used as normal I/O port pins.

Figure 17-18 shows the example of the automatic transmission mode operation timing, and Figure 17-19 shows the operation flowchart.

Figure 17-18. Example of Automatic Transmission Mode Operation Timing



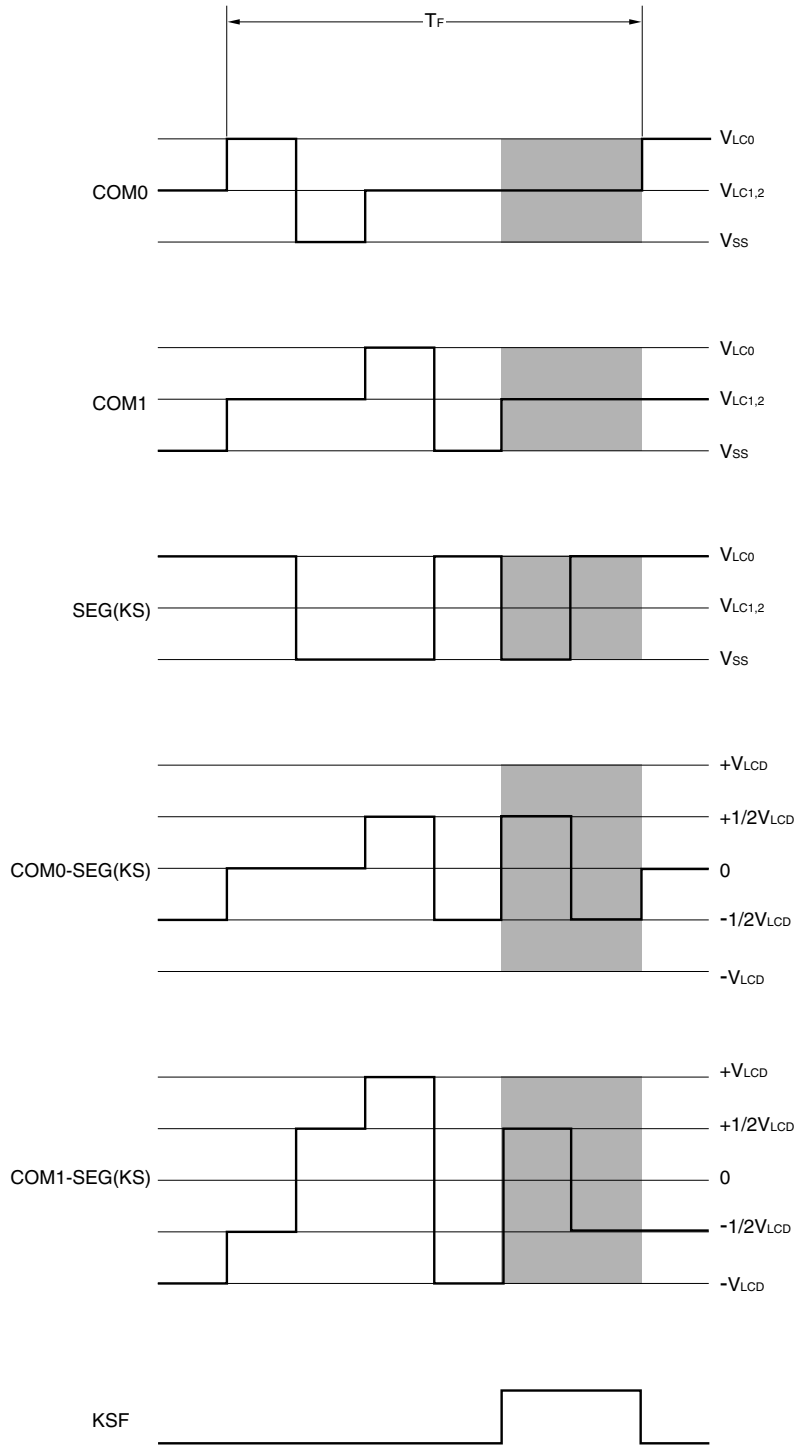
Cautions 1. Because, in the automatic transmission mode, the automatic transmit/receive function reads data from the internal buffer RAM after 1-byte transmission, an interval is inserted until the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon the set value of automatic data transfer interval specification register 0 (ADTI0).

2. If an access to the buffer RAM by the CPU conflicts with an access to the buffer RAM by serial interface CSIA0 during the interval period, the interval time specified by automatic data transfer interval specification register 0 (ADTI0) may be extended.

Remark ACSIIF: Interrupt request flag
TSF0: Bit 0 of serial status register 0 (CSIS0)

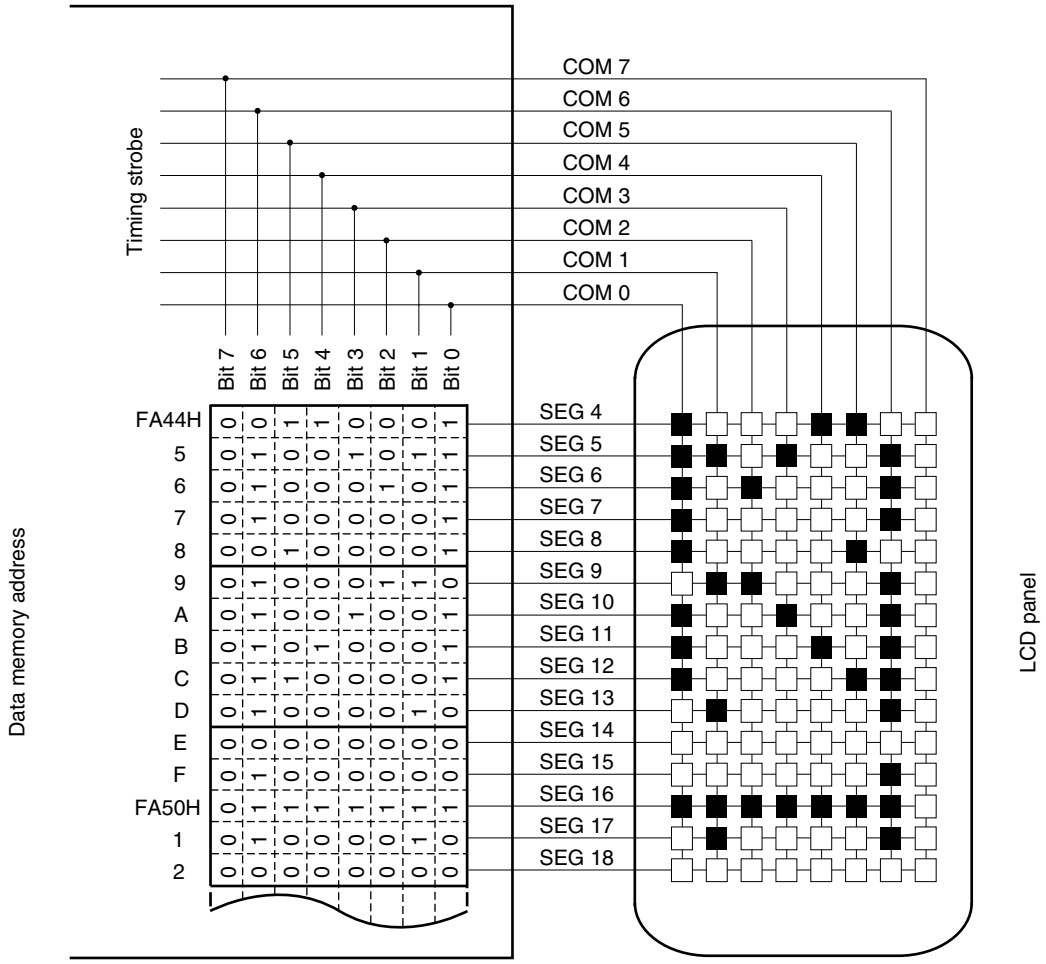
(b) When segment key scan function is used (KSON = 1)

<Key input wait>



Shaded sections: Segment key scan output period

Figure 18-31. Example of Connecting Eight-Time-Slice LCD Panel



18.9 Cautions When Using Segment Key Scan Function

(1) Conditions for use

Use the segment key scan function if V_{DD} is equal to V_{LC0}.

(2) Segment key scan input pins

Only the KR0 to KR7 pins can be used as input pins for the segment key scan function.

Other pins cannot be used as input pins for the segment key scan function.

(3) Allowable input range of KR0 to KR7 pins

Due to a delay caused by a pull-up resistor, segment key scan input cannot be performed for the KR pin for a period of two f_{LCD} clocks from the start of the segment key scan output period.

Similarly, due to input end processing, segment key scan input cannot be performed for the KR pin for the period of the last f_{LCD} clock of the segment key scan output period.

(4) Key return mode register (KRM) setting

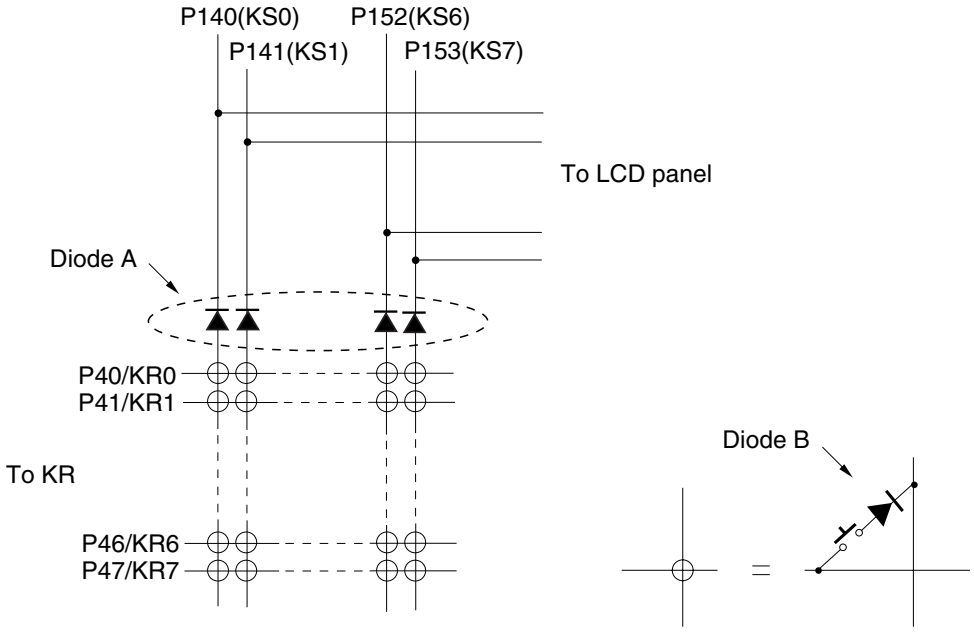
When the segment key scan function is used (KSON = 1), set KRMn to 1 or 0 to use or not use the KRn pin as a segment key scan input pin.

(5) Circuit configuration

When using the segment key scan function, at least diode A or diode B shown in Figure 18-38 is required.

The following problems will occur when diodes A and B are missing.

Figure 18-38. Key Matrix Configuration Example



(8) Remote controller receive DLS compare register (RMDLS)

This register is used to detect the low level of a remote controller data (short side).

RMDLS is set with an 8-bit memory manipulation instruction.

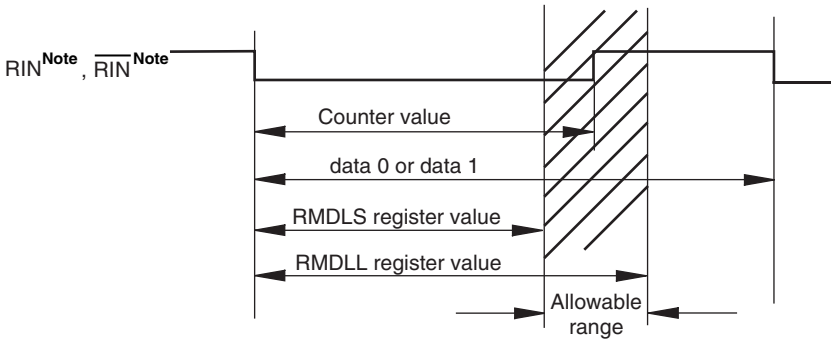
Reset signal generation sets RMDLS to 00H.

(9) Remote controller receive DLL compare register (RMDLL)

This register is used to detect the low level of a remote controller data (long side).

RMDLL is set with an 8-bit memory manipulation instruction.

Reset signal generation sets RMDLL to 00H.



If RMDLS ≤ counter value < RMDLL is satisfied, it is assumed that the low level of data 0 or data 1 has been successfully received.

Note RIN is generated in type A reception mode, and $\overline{\text{RIN}}$ is generated in type B and type C reception modes.

(10) Remote controller receive DH0S compare register (RMDH0S)

This register is used to detect the high level of a remote controller data 0 (short side).

RMDH0S is set with an 8-bit memory manipulation instruction.

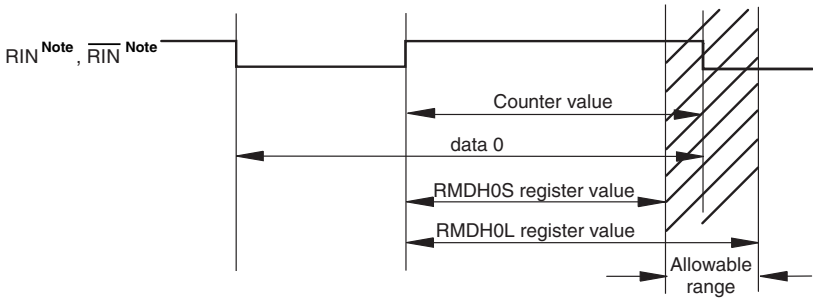
Reset signal generation sets RMDH0S to 00H.

(11) Remote controller receive DH0L compare register (RMDH0L)

This register is used to detect the high level of a remote controller data 0 (long side).

RMDH0L is set with an 8-bit memory manipulation instruction.

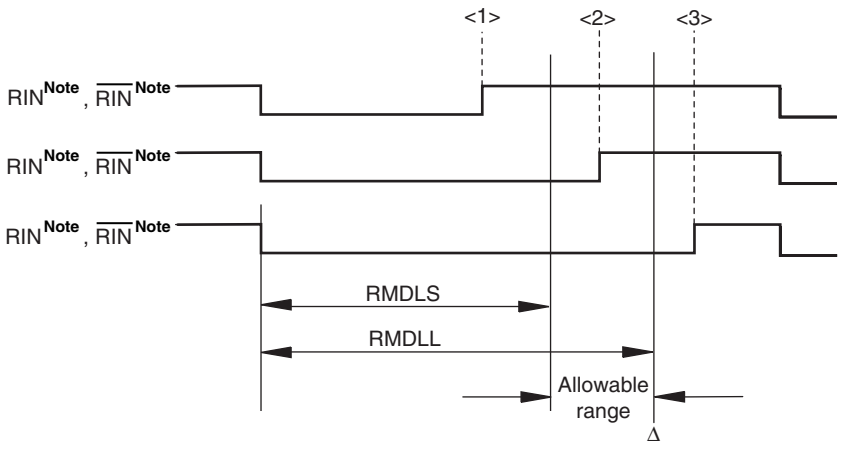
Reset signal generation sets RMDH0L to 00H.



If RMDH0S ≤ counter value < RMDH0L is satisfied, it is assumed that the high level of data 0 has been successfully received, and therefore RMSR receives the data.

Note RIN is generated in type A reception mode, and $\overline{\text{RIN}}$ is generated in type B and type C reception modes.

(3) Data low level width determination



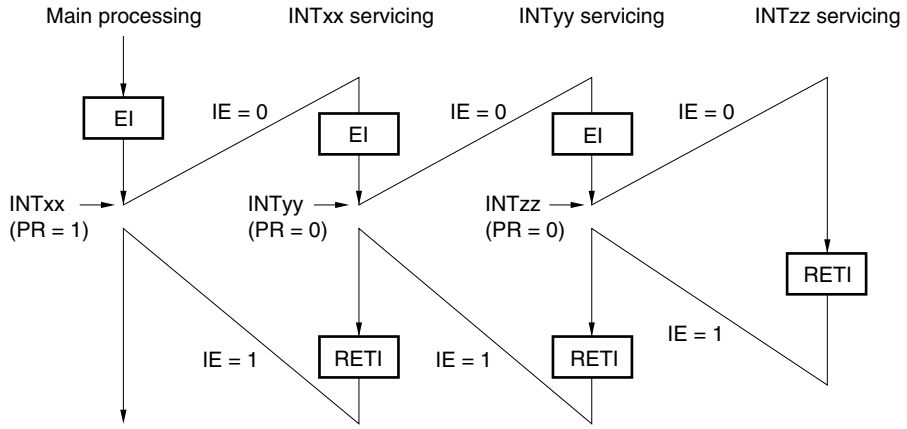
Note RIN is generated in type A reception mode, and $\overline{\text{RIN}}$ is generated in type B and type C reception modes.

Relationship Between RMDLS/RMDLL/Counter	Position of Waveform	Corresponding Operation
Counter < RMDLS	<1>: Short	Error interrupt INTRERR is generated note. Measuring guide pulse high-level width is started.
RMDLS ≤ counter < RMDLL	<2>: Within the range	Measuring data high-level width is started.
RMDLL ≤ counter	<3>: Long	(Type A reception mode) Measuring the end width is started from the Δ point. (Type B, Type C reception modes) Error interrupt INTRERR is generated at the Δ point. note.

Note In type C reception mode, before the first INTDFULL interrupt is generated, INTRERR will not be generated. However, RMSR and RMSCR will be cleared.

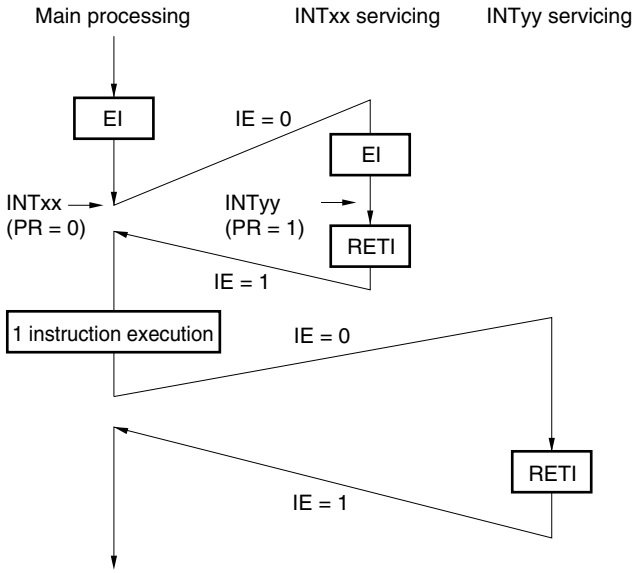
Figure 21-10. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control



Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
PR = 1: Lower priority level
IE = 0: Interrupt request acknowledgment disabled

CHAPTER 26 LOW-VOLTAGE DETECTOR

26.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVI}) or the input voltage from an external input pin (EXLVI) with the detection voltage (V_{EXLVI} = 1.21 V (TYP.): fixed), and generates an internal reset or internal interrupt signal.
- The supply voltage (V_{DD}) or input voltage from an external input pin (EXLVI) can be selected by software.
- Reset or interrupt function can be selected by software.
- Detection levels (16 levels) of supply voltage can be changed by software.
- Operable in STOP mode.

The reset and interrupt signals are generated as follows depending on selection by software.

Selection of Level Detection of Supply Voltage (V_{DD}) (LVISEL = 0)		Selection Level Detection of Input Voltage from External Input Pin (EXLVI) (LVISEL = 1)	
Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).	Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).
Generates an internal reset signal when $V_{DD} < V_{LVI}$ and releases the reset signal when $V_{DD} \geq V_{LVI}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).	Generates an internal reset signal when EXLVI < V_{EXLVI} and releases the reset signal when EXLVI ≥ V_{EXLVI}.	Generates an internal interrupt signal when EXLVI drops lower than V_{EXLVI} (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).

Remark LVISEL: Bit 2 of low-voltage detection register (LVIM)
LVIMD: Bit 1 of LVIM

While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

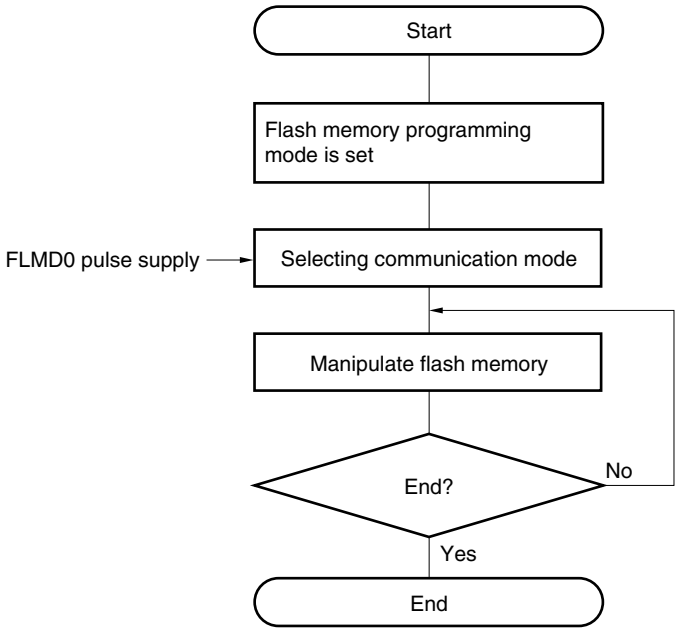
When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, see **CHAPTER 24 RESET FUNCTION**.

28.7 Programming Method

28.7.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

<R> **Figure 28-12. Flash Memory Manipulation Procedure**



28.7.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the 78K0/LF3 in the flash memory programming mode. To set the mode, set the FLMD0 pin to V_{DD} and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 28-13. Flash Memory Programming Mode

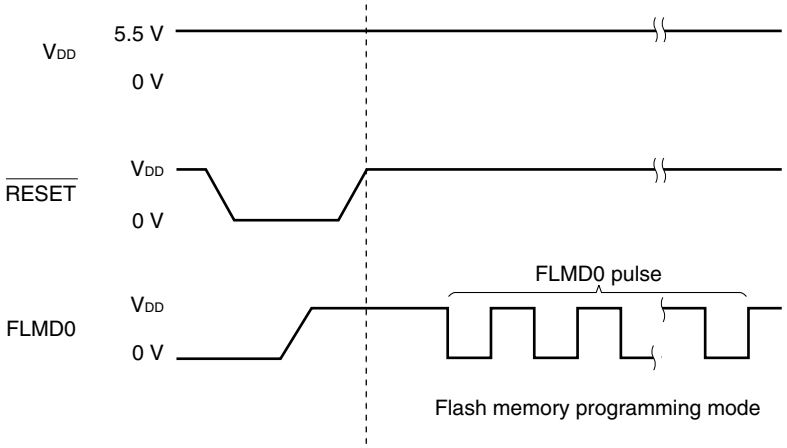


Table 28-6. Relationship Between FLMD0 Pin and Operation Mode After Reset Release

FLMD0	Operation Mode
0	Normal operation mode
V_{DD}	Flash memory programming mode