Renesas Electronics America Inc - UPD78F0491GC-GAD-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b, 3x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0491gc-gad-ax

CHAPTER 29 ON-CHIP DEBUG FUNCTION 731

29.1 Connecting QB-MINI2 to 78K0/LF3 731
29.2 Reserved Area Used by QB-MINI2 732

CHAPTER 30 INSTRUCTION SET 733

30.1 Conventions Used in Operation List 733
30.1.1 Operand identifiers and specification methods 733
30.1.2 Description of operation column 734
30.1.3 Description of flag operation column 734
30.2 Operation List 735
30.3 Instructions Listed by Addressing Type 743

CHAPTER 31 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) 746

CHAPTER 32 PACKAGE DRAWINGS 770

CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS 772

CHAPTER 34 CAUTIONS FOR WAIT 773

34.1 Cautions for Wait 773
34.2 Peripheral Hardware That Generates Wait 774

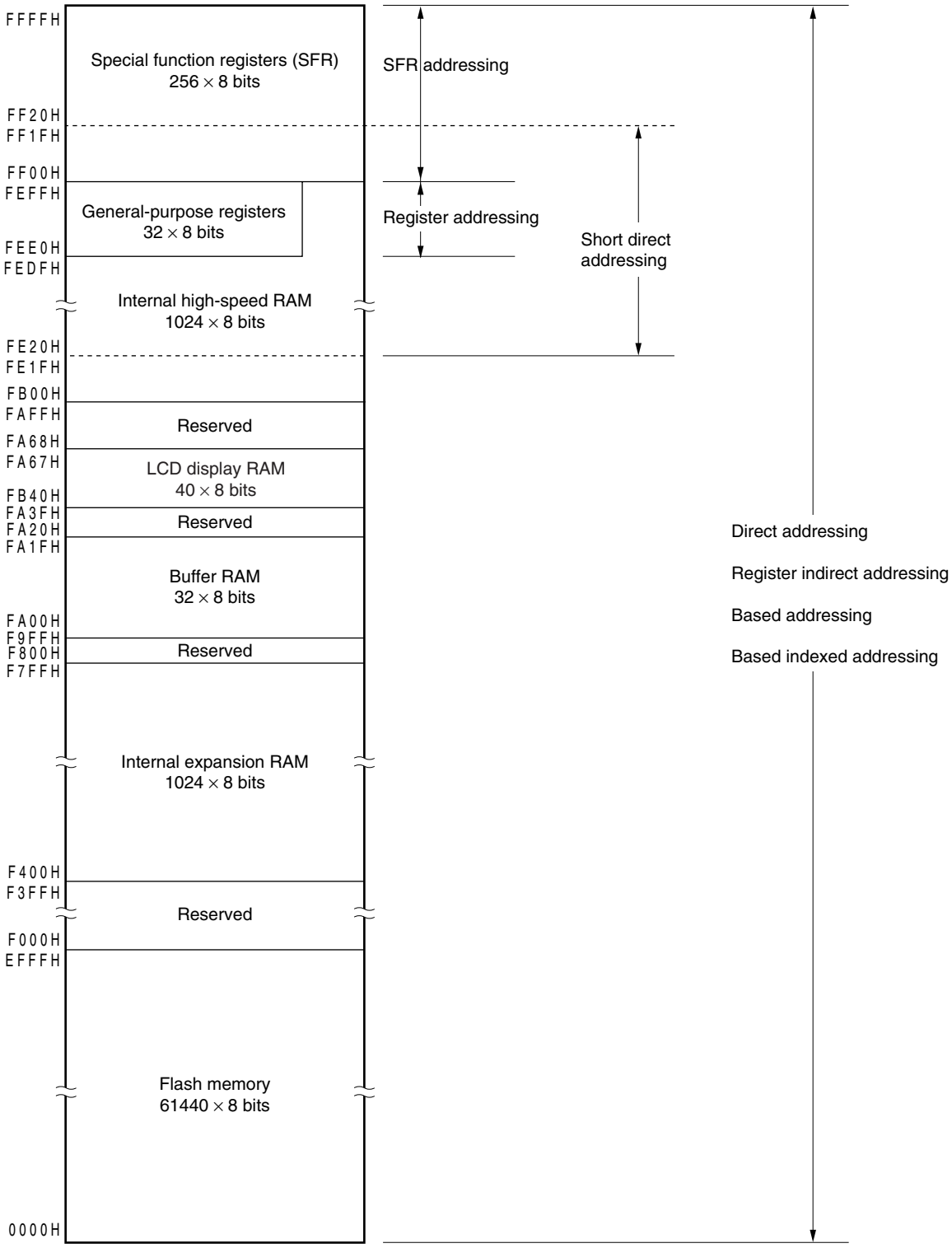
APPENDIX A DEVELOPMENT TOOLS 775

A.1 Software Package 778
A.2 Language Processing Software 778
A.3 Control Software 779
A.4 Flash Memory Writing Tools 780
A.4.1 When using flash memory programmer PG-FP5 and FL-PR5 780
A.4.2 When using on-chip debug emulator with programming function QB-MINI2 780
A.5 Debugging Tools (Hardware) 781
A.5.1 When using in-circuit emulator QB-78K0LX3 781
A.5.2 When using on-chip debug emulator with programming function QB-MINI2 782
A.6 Debugging Tools (Software) 782

APPENDIX B REVISION HISTORY 783

B.1 Major Revisions in This Edition 783
B.2 Revision History up to Previous Editions 786

Figure 3-19. Correspondence Between Data Memory and Addressing (μPD78F0475, 78F0485)



3.3.3 Table indirect addressing

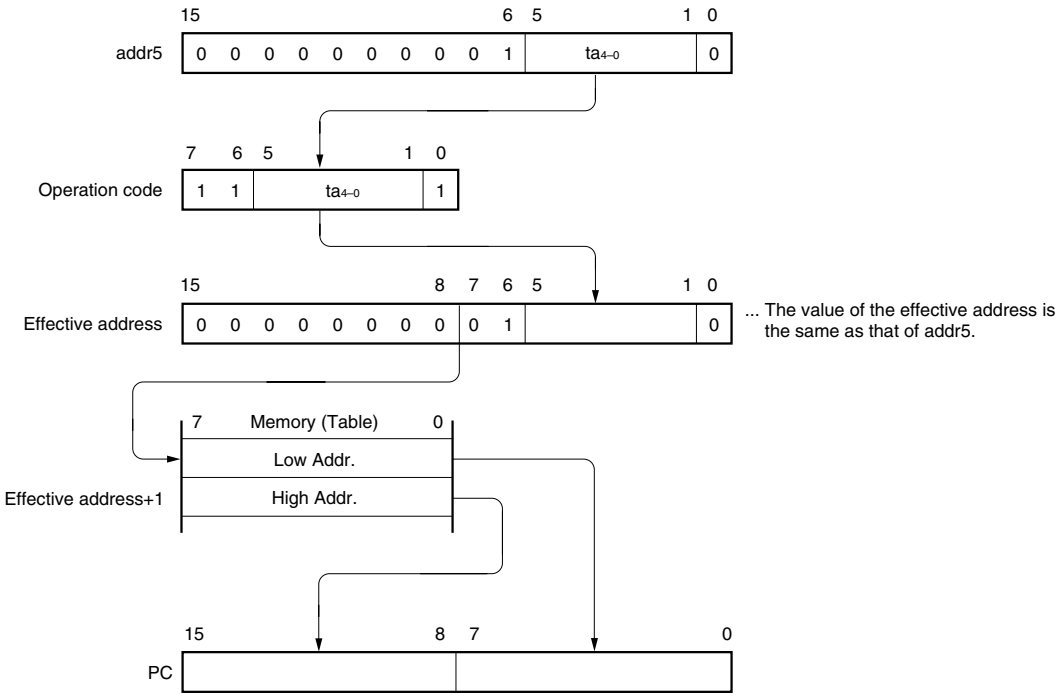
[Function]

Table contents (branch destination address) of the particular location to be addressed by bits 1 to 5 of the immediate data of an operation code are transferred to the program counter (PC) and branched.

This function is carried out when the CALLT [addr5] instruction is executed.

This instruction references the address stored in the memory table from 40H to 7FH, and allows branching to the entire memory space.

<R> **[Illustration]**



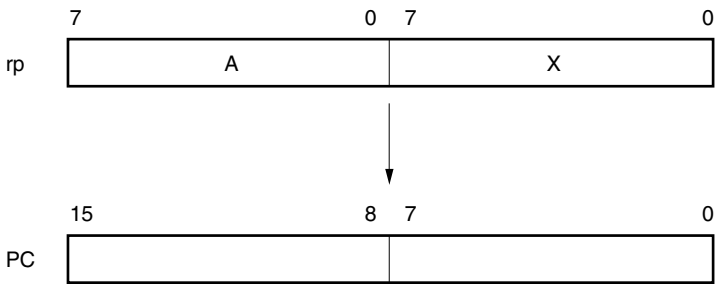
3.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

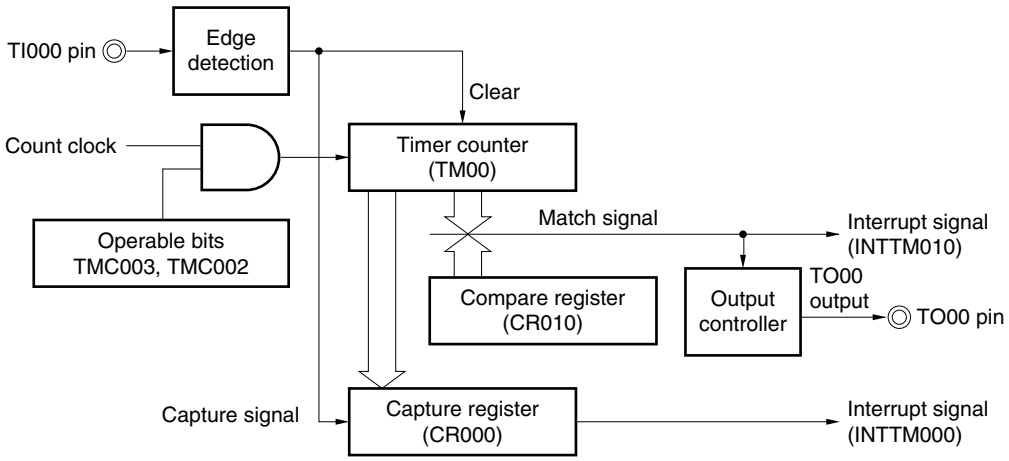
This function is carried out when the BR AX instruction is executed.

[Illustration]



(3) Operation in clear & start mode by entered TI000 pin valid edge input (CR000: capture register, CR010: compare register)

Figure 6-27. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register)



7.4.2 Operation as external event counter

The external event counter counts the number of external clock pulses to be input to the TI5n pin by 8-bit timer counter 5n (TM5n).

TM5n is incremented each time the valid edge specified by timer clock selection register 5n (TCL5n) is input. Either the rising or falling edge can be selected.

When the TM5n count value matches the value of 8-bit timer compare register 5n (CR5n), TM5n is cleared to 0 and an interrupt request signal (INTTM5n) is generated.

Whenever the TM5n value matches the value of CR5n, INTTM5n is generated.

Setting

<1> Set each register.

- Set the port mode register (PM44, PM43, or PM34)[Note] to 1.
- TCL5n: Select TI5n pin input edge.
  TI5n pin falling edge → TCL5n = 00H
  TI5n pin rising edge → TCL5n = 01H
- CR5n: Compare value
- TMC5n: Stop the count operation, select the mode in which clear & start occurs on match of TM5n and CR5n, disable the timer F/F inversion operation, disable timer output.
  (TMC5n = 0000××00B × = Don't care)

<2> When TCE5n = 1 is set, the number of pulses input from the TI5n pin is counted.

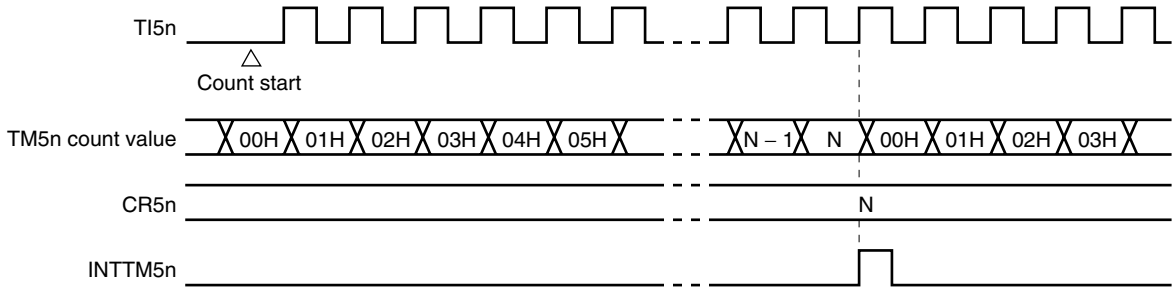
<3> When the values of TM5n and CR5n match, INTTM5n is generated (TM5n is cleared to 00H).

<4> After these settings, INTTM5n is generated each time the values of TM5n and CR5n match.

Note 8-bit timer/event counter 50: PM44
8-bit timer/event counter 51: PM43
8-bit timer/event counter 52: PM34

Remark For how to enable the INTTM5n signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 7-16. External Event Counter Operation Timing (with Rising Edge Specified)



Remark 1. 8-bit timer/event counter 52 (TM52) can be used as an external 24-bit event counter, by connecting it with 16-bit timer/event counter (TM00) in cascade. Also, input enable of TM52 can be controlled via TMH2. For details, see **6.4.9 External 24-bit event counter operation**.

2. N = 00H to FFH, n = 0 to 2

(1) 8-bit timer H compare register 0n (CMP0n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in all of the timer operation modes.

This register constantly compares the value set to CMP0n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn) and inverts the output level of TOHn.

Rewrite the value of CMP0n while the timer is stopped (TMHEn = 0).

A reset signal generation sets this register to 00H.

Figure 8-4. Format of 8-Bit Timer H Compare Register 0n (CMP0n)

Address: FF18H (CMP00), FF1AH (CMP01), FF44H (CMP02) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP0n (n = 0 to 2)								

Caution CMP0n cannot be rewritten during timer count operation. CMP0n can be refreshed (the same value is written) during timer count operation.

(2) 8-bit timer H compare register 1n (CMP1n)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, inverts the output level of TOHn. No interrupt request signal is generated.

In the carrier generator mode, the CMP1n register always compares the value set to CMP1n with the count value of the 8-bit timer counter Hn and, when the two values match, generates an interrupt request signal (INTTMHn). At the same time, the count value is cleared.

CMP1n can be rewritten during timer count operation.

If the value of CMP1n is rewritten while the timer is operating, the new value is latched and transferred to CMP1n when the count value of the timer matches the old value of CMP1n, and then the value of CMP1n is changed to the new value. If matching of the count value and the CMP1n value and writing a value to CMP1n conflict, the value of CMP1n is not changed.

A reset signal generation sets this register to 00H.

Figure 8-5. Format of 8-Bit Timer H Compare Register 1n (CMP1n)

Address: FF19H (CMP10), FF1BH (CMP11), FF45H (CMP12) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP1n (n = 0 to 2)								

Caution In the PWM output mode and carrier generator mode, be sure to set CMP1n when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to CMP1n).

Remark n = 0 to 2, however, TOH0 and TOH1 only for TOHn

8.3 Registers Controlling 8-Bit Timers H0, H1, and H2

The following four registers are used to control 8-bit timers H0, H1, and H2.

- 8-bit timer H mode register n (TMHMDn)
- 8-bit timer H carrier control register 1 (TMCYC1)[Note]
- Port mode register 3 (PM3)
- Port register 3 (P3)

Note 8-bit timer H1 only

(1) 8-bit timer H mode register n (TMHMDn)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Remark n = 0 to 2

(2) 8-bit timer H carrier control register 1 (TMCYC1)

This register controls the remote control output and carrier pulse output status of 8-bit timer H1.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 8-9. Format of 8-Bit Timer H Carrier Control Register 1 (TMCYC1)

Address: FF6DH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	<0>
TMCYC1	0	0	0	0	0	RMC1	NRZB1	NRZ1

RMC1	NRZB1	Remote control output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

NRZ1	Carrier pulse output status flag
0	Carrier output disabled status (low-level status)
1	Carrier output enabled status (RMC1 = 1: Carrier pulse output, RMC1 = 0: High-level status)

Note Bit 0 is read-only.

Caution Do not rewrite RMC1 when TMHE1 = 1. However, TMCYC1 can be refreshed (the same value is written).

(3) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO and P31/TOH1/INTP3 pins for timer output, clear PM32 and PM31 and the output latches of P32 and P31 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 8-10. Format of Port Mode Register 3 (PM3)

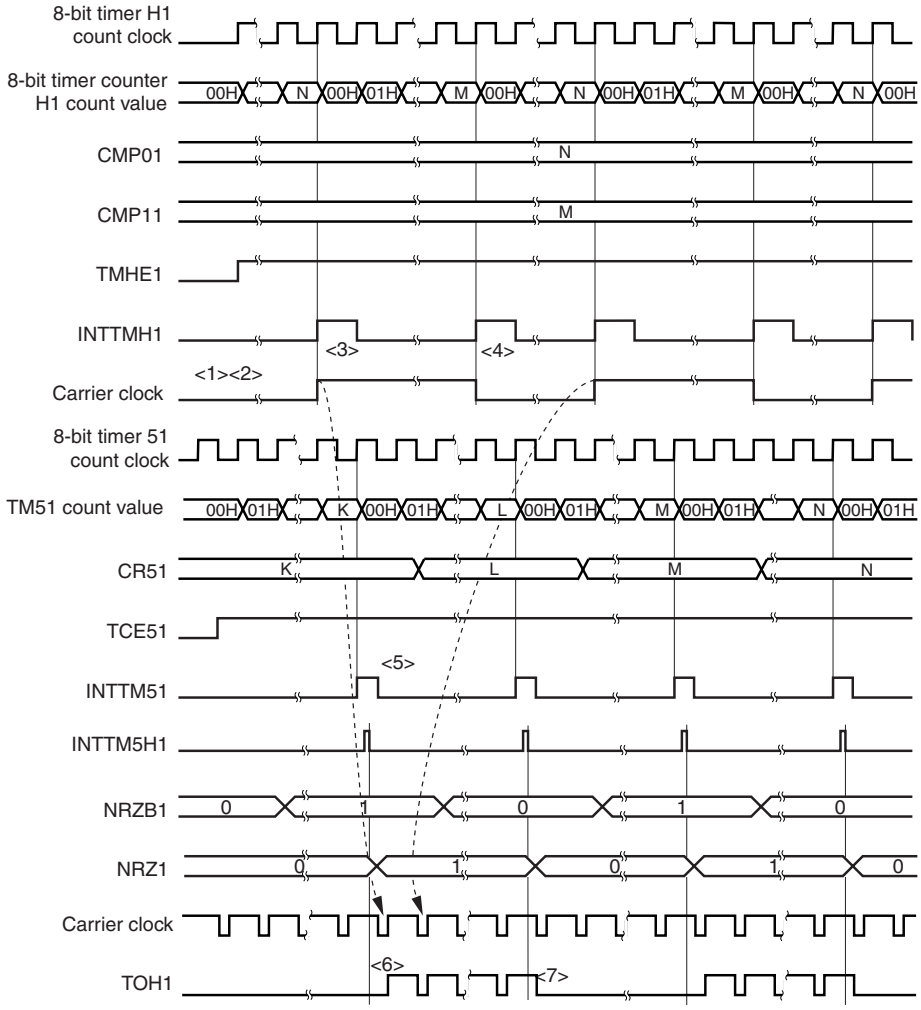
Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 8-17. Carrier Generator Mode Operation Timing (2/3)

(b) Operation when CMP01 = N, CMP11 = M



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to other than 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

<6> A carrier signal is output at the first rising edge of the carrier clock if NRZ1 is set to 1.

<7> When NRZ1 = 0, the TOH1 output is held at the high level and is not changed to low level while the carrier clock is high level (from <6> and <7>, the high-level width of the carrier clock waveform is guaranteed).

Remark INTTM5H1 is an internal signal and not an interrupt source.

11.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

Table 11-1. Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output selection register (CKS) Port mode register 3 (PM3) Port register 3 (P3) Port mode register 1 (PM1) Port register 1 (P1)

11.3 Registers Controlling Clock Output/Buzzer Output Controller

The following two registers are used to control the clock output/buzzer output controller.

- Clock output selection register (CKS)
- Port mode register 3 (PM3)
- Port mode register 1 (PM1)

(1) Clock output selection register (CKS)

This register sets output enable/disable for clock output (PCL) and for the buzzer frequency output (BUZ), and sets the output clock.

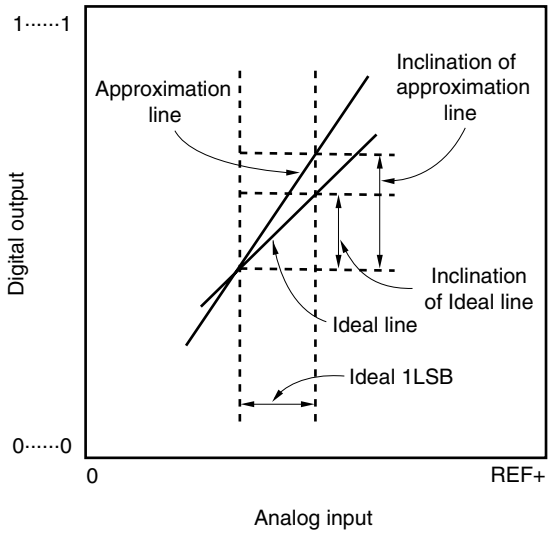
CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

(5) Gain error

The gain error is the ratio of the ideal inclination to the inclination of the approximation line.

Figure 13-18. Gain Error

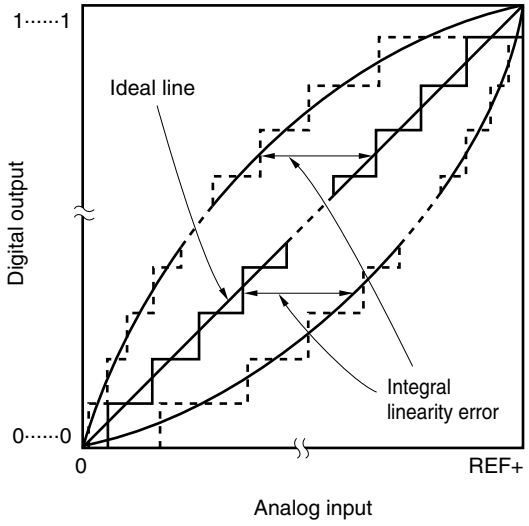


$$\text{Gain error} = \frac{\text{Inclination of approximation line} - 1}{\text{Inclination of Ideal line}} \times 100\ [\%]$$

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the approximation line. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the offset and gain error are 0.

Figure 13-19. Integral linearity error



14.2 Configuration of Serial Interface UART0

Serial interface UART0 includes the following hardware.

Table 14-1. Configuration of Serial Interface UART0

Item	Configuration
Registers	Receive buffer register 0 (RXB0) Receive shift register 0 (RXS0) Transmit shift register 0 (TXS0)
Control registers	Asynchronous serial interface operation mode register 0 (ASIM0) Asynchronous serial interface reception error status register 0 (ASIS0) Baud rate generator control register 0 (BRGC0) Port function register 1 (PF1) Port mode register 1 (PM1) Port register 1 (P1)

14.4.2 Asynchronous serial interface (UART) mode

In this mode, 1-byte data is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port mode register 1 (PM1)
- Port register 1 (P1)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the BRGC0 register (see **Figure 14-4**).
<2> Set bits 1 to 4 (SL0, CL0, PS00, and PS01) of the ASIM0 register (see **Figure 14-2**).
<3> Set bit 7 (POWER0) of the ASIM0 register to 1.
<4> Set bit 6 (TXE0) of the ASIM0 register to 1. → Transmission is enabled.
Set bit 5 (RXE0) of the ASIM0 register to 1. → Reception is enabled.
<5> Write data to the TXS0 register. → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 14-2. Relationship Between Register Settings and Pins

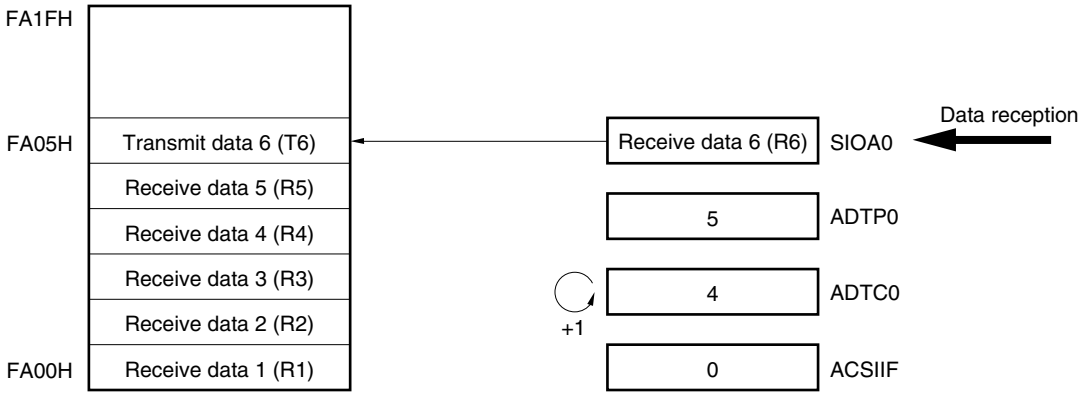
POWER0	TXE0	RXE0	PM13	P13	PM12	P12	UART0 Operation	Pin Function	
								TxD0/SO10/P13	RxD0/SI10/P12
0	0	0	×Note	×Note	×Note	×Note	Stop	SO10/P13	SI10/P12
1	0	1	×Note	×Note	1	×	Reception	SO10/P13	RxD0
	1	0	0	×	×Note	×Note	Transmission	TxD0	SI10/P12
	1	1	0	×	1	×	Transmission/ reception	TxD0	RxD0

Note Can be set as port function or serial interface CSI10.

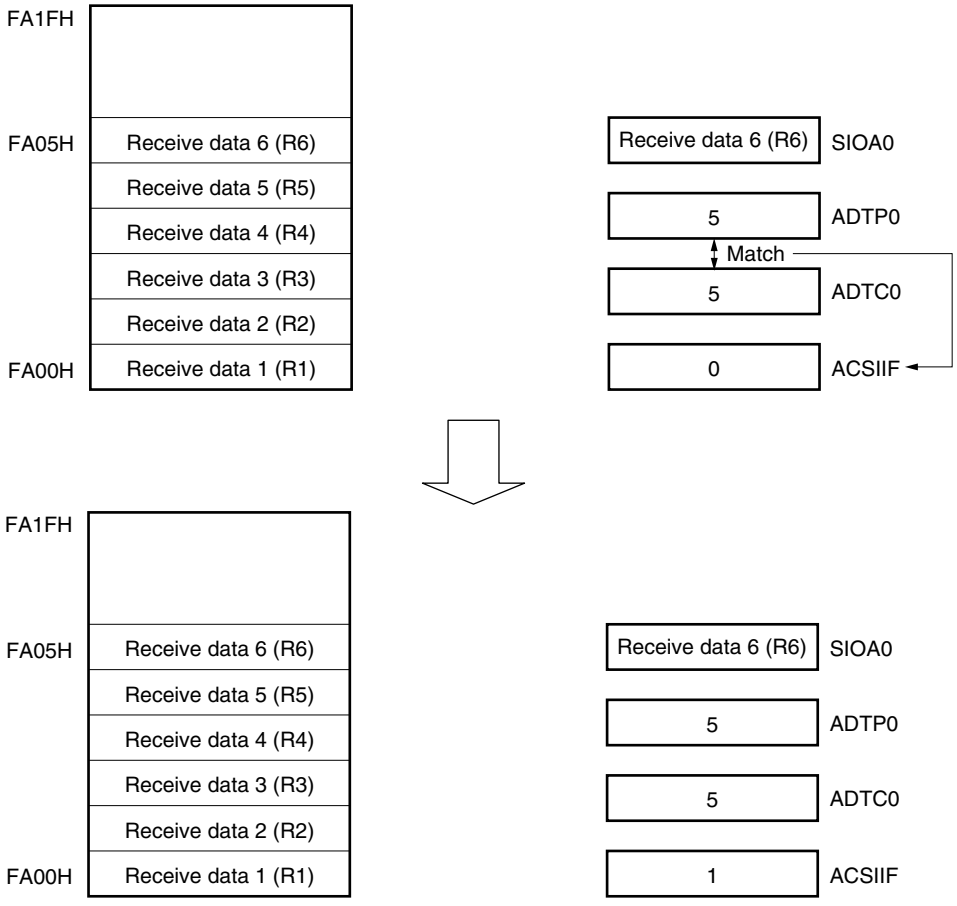
Remark ×: don't care
POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
PM1×: Port mode register
P1×: Port output latch

Figure 17-17. Internal Buffer RAM Operation in Automatic Transmission/Reception Mode (End of Transmission/Reception)

<1> End of 6th byte transmission/reception



<2> End of automatic transmission/reception



(7) Port mode register 4 (PM4)

This register sets port 4 input/output in 1-bit units.

When using the segment key scan function, set the port mode register of the port to be used to 1 (PM4n = 1), in order to set the P4n pin as a key scan input pin.

PM4 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets FFH.

Figure 18-8. Format of Port mode register 4 (PM4)

Address: FF24H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PF4n	P4n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(8) Pull-up resistor option register 4 (PU4)

This register is used to set whether to use the on-chip pull-up resistors of P40 to P47.

When using the segment key scan function, set the pull-up resistor option register of the port to be used to 0 (PU4n = 0), in order to set the P4n pin as a key scan input pin.

An external pull-up resistor cannot be used, because it affects the LCD display output.

PU4 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets 00H.

Figure 18-9. Format of Pull-up Resistor Option Register 4

Address: FF34H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40

PF4n	P4n pin on-chip pull-up resistor selection (n = 0 to 7)	
	Pin using segment key scan function	Pin not using segment key scan function
0	On-chip pull-up resistor connected only during segment key scan output period	On-chip pull-up resistor not connected
1	Setting prohibited	On-chip pull-up resistor connected

CHAPTER 19 MANCHESTER CODE GENERATOR

19.1 Functions of Manchester Code Generator

The following three types of modes are available for the Manchester code generator.

(1) Operation stop mode

This mode is used when output by the Manchester code generator/bit sequential buffer is not performed. This mode reduces the power consumption.

For details, refer to **19.4.1 Operation stop mode**.

(2) Manchester code generator mode

This mode is used to transmit Manchester code from the MCGO pin.

The transfer bit length can be set and transfers of various bit lengths are enabled. Also, the output level of the data transfer and LSB- or MSB-first can be set for 8-bit transfer data.

(3) Bit sequential buffer mode

This mode is used to transmit bit sequential data from the MCGO pin.

The transfer bit length can be set and transfers of various bit lengths are enabled. Also, the output level of the data transfer and LSB- or MSB-first can be set for 8-bit transfer data.

19.2 Configuration of Manchester Code Generator

The Manchester code generator includes the following hardware.

Table 19-1. Configuration of Manchester Code Generator

Item	Configuration
Registers	MCG transmit buffer register (MC0TX) MCG transmit bit count specification register (MC0BIT)
Control registers	MCG control register 0 (MC0CTL0) MCG control register 1 (MC0CTL1) MCG control register 2 (MC0CTL2) MCG status register (MC0STR) Port mode register 3 (PM3) Port register 3 (P3)

Table 21-2. Flags Corresponding to Interrupt Request Sources (2/2)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTAD[Note 1]	ADIF[Note 1]	IF1L	ADMK[Note 1]	MK1L	ADPR[Note 1]	PR1L
INTSR0	SRIF0		SRMK0		SRPR0	
INTRTC	RTCIF		RTCMK		RTCPR	
INTTM51[Note 2]	TMIF51		TMMK51		TMPR51	
INTKR	KRIF		KRMK		KRPR	
INTRTCI	RTCIIF		RTCIMK		RTCIPR	
INTDSAD[Note 3]	DSADIF[Note 3]		DSADMK[Note 3]		DASDPR[Note 3]	
INTTM52	TMIF52		TMMK52		TMPR52	
INTTMH2	TMHIF2	IF1H	TMHMK2	MK1H	TMHPR2	PR1H
INTMCG	MCGIF		MCGMK		MCGPR	
INTRIN	RINIF		RINMK		RINPR	
INTRERR INTGP INTREND INTDFULL	RERRIF[Note 4] GPIF[Note 4] RENDIF[Note 4] DFULLIF[Note 4]		RERRMK[Note 5] GPMK[Note 5] RENDMK[Note 5] DFULLMK[Note 5]		RERRPR[Note 6] GPPR[Note 6] RENDPR[Note 6] DFULLPR[Note 6]	
INTACSI	ACSIIF		ACSIMK		ACSIPR	

Notes 1. μPD78F048x and 78F049x only.

2. When 8-bit timer/event counter 51 and 8-bit timer H1 are used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (see **Figure 8-15 Transfer Timing**).

3. μPD78F049x only.

4. If either interrupt source INTRERR, INTGP, INTREND, or INTDFULL is generated, bit 3 of IF1H is set (1).

5. Bit 3 of MK1H supports all of interrupt sources INTRERR, INTGP, INTREND, and INTDFULL.

6. Bit 3 of PR1H supports all of interrupt sources INTRERR, INTGP, INTREND, and INTDFULL.

DC Characteristics (2/5)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10, P16, P17, P32, P80 to P83, P90 to P93, P100 to P103, P110 to P112, P121 to P124, P130 to P133, P140 to P143, P150 to P153		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P11 to P15, P30, P31, P33, P34, P40 to P47, P113, P120, $\overline{\text{RESET}}$, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
Input voltage, low	V_{IL1}	P10, P16, P17, P32, P80 to P83, P90 to P93, P100 to P103, P110 to P112, P121 to P124, P130 to P133, P140 to P143, P150 to P153		0		0.3V_{DD}	V
	V_{IL2}	P11 to P15, P30, P31, P33, P34, P40 to P47, P113, P120, $\overline{\text{RESET}}$, EXCLK		0		0.2V_{DD}	V
	V_{IL3}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
Output voltage, high	V_{OH1}	P10 to P17, P30 to P34, P40 to P47, P120	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
		P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	I_{OH1} = –0.1 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P10 to P17, P30 to P34, P40 to P47, P120	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA			0.7	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA			0.4	V
		P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153	I_{OL1} = 0.4 mA			0.4	V
	V_{OL2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The high-level and low-level input voltages of P122/EXCLK vary between the input port mode and external clock mode.

10-bit successive approximation type A/D Converter Characteristics (μPD78F048x and 78F049x only)
(T_A = –40 to +85°C, 2.3 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES1}				10	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	μs
		2.7 V ≤ AV_{REF} < 4.0 V	12.2		36.7	μs
		2.3 V ≤ AV_{REF} < 2.7 V	27		66.6	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.3 V ≤ AV_{REF} < 2.7 V			±0.6	%FSR
Integral non-linearity error[Note 1]	I_{LE1}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±6.5	LSB
Differential non-linearity error[Note 1]	D_{LE1}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		2.3 V ≤ AV_{REF} < 2.7 V			±2.0	LSB
Analog input voltage	V_{AIN1}		AV_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3/3)

Edition	Description	Applied to:
2nd edition	Change of and addition of **Remark** to **Figure 28-17 Boot Swap Function**	**CHAPTER 28 FLASH MEMORY**
	Change of **Figure 28-18 Example of Executing Boot Swapping**	
	Change to formal spec from target spec	**CHAPTER 31 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS)**
	Addition of explanation to **Table 33-1. Registers That Generate Wait and Number of CPU Wait Clocks**	**CHAPTER 33 CAUTIONS FOR WAIT**
	Change of **Table 33-2. RAM Accesses That Generate Wait and Number of CPU Wait Clocks**	
	Addition of appendix	**APPENDIX REVISION HISTORY**