Renesas Electronics America Inc - UPD78F0492GK-GAK-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b, 3x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0492gk-gak-ax

(2) Control mode

P140 to P143 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

<R> **(a) SEG24 (KS0) to SEG27 (KS3)**

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.12 P150 to P153 (port 15)

P150 to P153 function as a 4-bit I/O port. These pins also function as pins for segment signal output and simultaneous output of segment key source signal for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

(1) Port mode

P150 to P153 function as a 4-bit I/O port. P150 to P153 can be set to input or output port in 1-bit units using port mode register 15 (PM15). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 15 (PU15).

(2) Control mode

P150 to P153 function as segment signal output and simultaneous output of segment key source signal for the LCD controller/driver.

<R> **(a) SEG28 (KS4) to SEG31 (KS7)**

These pins are the segment signal output pins for the LCD controller/driver.

The segment key source signal output can be simultaneously used by setting the LCD mode register (LCDMD).

2.2.13 AV_{REF} (μPD78F048x and 78F049x only)

This is the 10-bit successive approximation type A/D converter reference voltage input pin and the positive power supply pin of port 2 and 16-bit $\Delta\Sigma$ type A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note When one or more of the pins of port 2 is used as the digital port pins or for segment output, make AV_{REF} the same potential as V_{DD}.

2.2.14 AV_{SS} (μPD78F048x and 78F049x only)

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

2.2.15 COM0 to COM7

These pins are the common signal output pins for the LCD controller/driver.

2.2.16 V_{LC0} to V_{LC3}

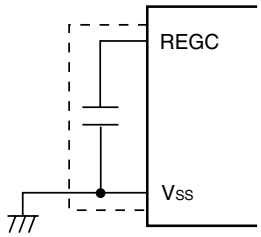
These pins are the power supply voltage pins for driving the LCD.

2.2.17 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.2.18 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF: recommended).



Caution Keep the wiring length as short as possible in the area enclosed by the broken lines in the above figures.

2.2.19 V_{DD}

This is the positive power supply pin.

2.2.20 V_{SS}

This is the ground potential pin.

2.2.21 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to V_{SS} in the normal operation mode.

In flash memory programming mode, connect this pin to the flash memory programmer.

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)
When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)
Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

(2) Example of setting procedure when using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock

<1>
- Restarting oscillation of the internal high-speed oscillation clock[Note]
(See **5.6.2 (1) Example of setting procedure when restarting internal high-speed oscillation clock**).
- Oscillating the high-speed system clock[Note]
(This setting is required when using the high-speed system clock as the peripheral hardware clock. See **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when the internal high-speed oscillation clock or high-speed system clock is already operating.

<2> Selecting the clock supplied as the main system clock and peripheral hardware clock (MCM register)
Set the main system clock and peripheral hardware clock using XSEL and MCM0.

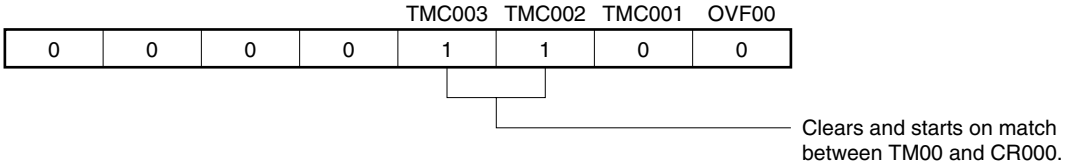
XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})

<3> Selecting the CPU clock division ratio (PCC register)
When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

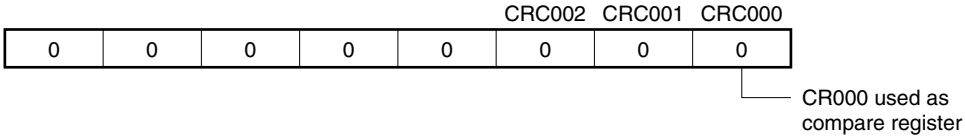
CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	f_{XP}/2 (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

Figure 6-18. Example of Register Settings for Square Wave Output Operation

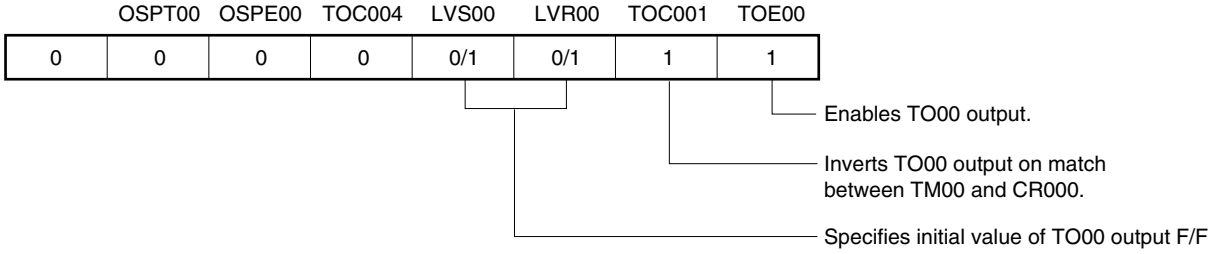
(a) 16-bit timer mode control register 00 (TMC00)



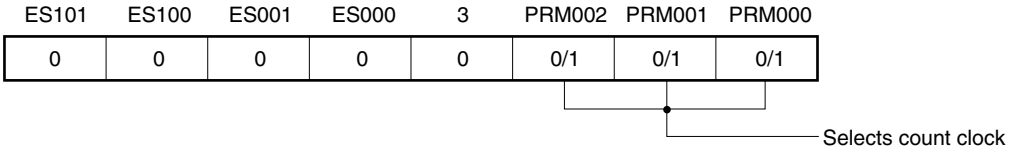
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

If M is set to CR000, the interval time is as follows.

- Square wave frequency = 1 / [2 × (M + 1) × Count clock cycle]

Setting CR000 to 0000H is prohibited.

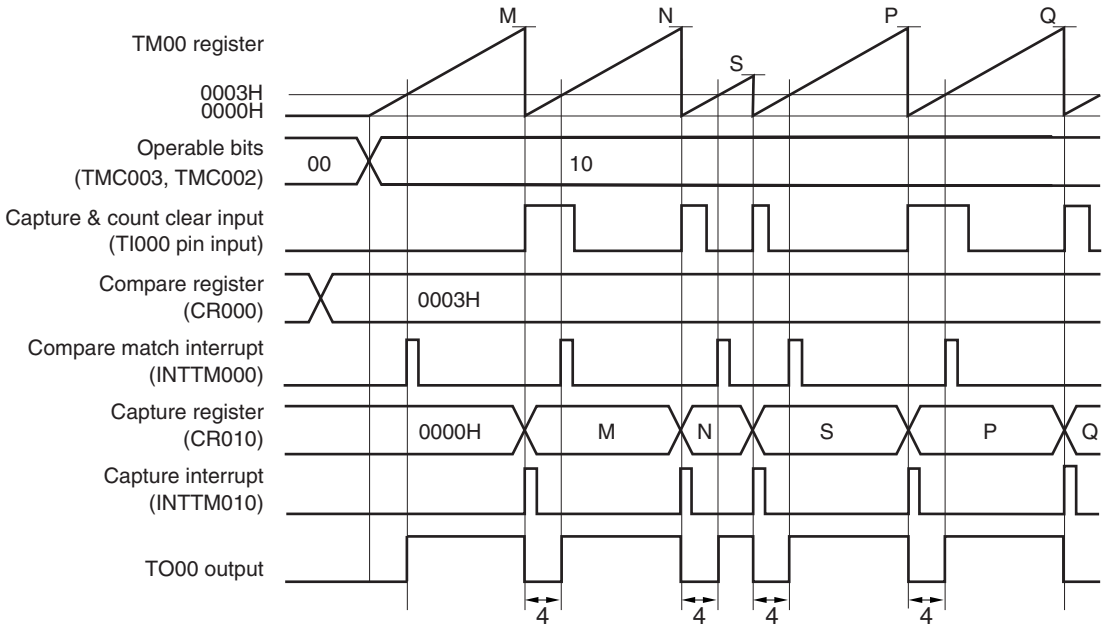
(g) 16-bit capture/compare register 010 (CR010)

Usually, CR010 is not used for the square wave output function. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00, = 04H, TMC00 = 0AH, CR000 = 0003H

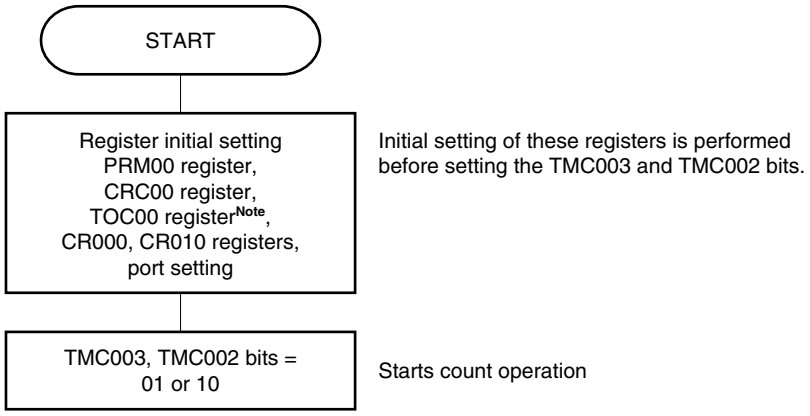


This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

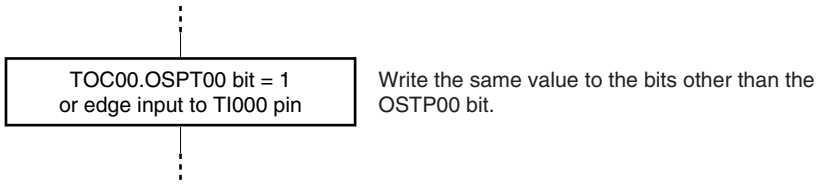
The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

Figure 6-46. Example of Software Processing for One-Shot Pulse Output Operation (2/2)

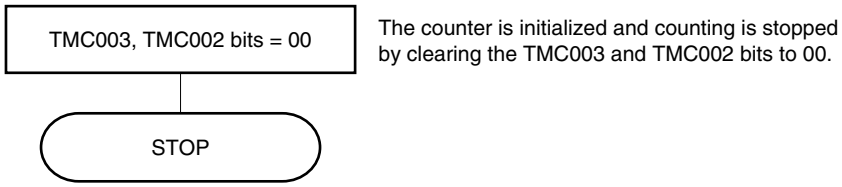
<1> Count operation start flow



<2> One-shot trigger input flow



<3> Count operation stop flow



Note Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50, 51, AND 52

7.1 Functions of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50 and 51 have the following functions.

- Interval timer
- External event counter[Note 1]
- Square-wave output[Note 2]
- PWM output[Note 2]

Notes 1. TM52 and TM00 can be connected in cascade to be used as an external 24-bit event counter. Also, the external event input of TM52 can be input enable-controlled via TMH2. For details, see **CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00**.

2. TM50 and TM51 only.

7.2 Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

8-bit timer/event counters 50, 51, and 52 include the following hardware.

Table 7-1. Configuration of 8-Bit Timer/Event Counters 50, 51, and 52

Item	Configuration
Timer register	8-bit timer counter 5n (TM5n)
Register	8-bit timer compare register 5n (CR5n)
Timer input	TI5n
Timer output	TO50, TO51
Control registers	Timer clock selection register 5n (TCL5n) 8-bit timer mode control register 5n (TMC5n) Input switch control register (ISC) Port mode register 3 (PM3) or port mode register 4 (PM4) Port register 3 (P3) or port register 4 (P4)

Remark n = 0 to 2

Figures 7-1 to 7-3 show the block diagrams of 8-bit timer/event counters 50, 51, and 52.

(2) 8-bit timer mode control register 5n (TMC5n)

TMC5n is a register that performs the following five types of settings.

<1> 8-bit timer counter 5n (TM5n) count operation control
<2> 8-bit timer counter 5n (TM5n) operating mode selection[Note]
<3> Timer output F/F (flip flop) status setting[Note]
<4> Active level selection in timer F/F control or PWM (free-running) mode[Note]
<5> Timer output control[Note]

TMC5n can be set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets this register to 00H.

Note TM50 and TM51 only.
Remark n = 0 to 2

Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50)

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

(**Cautions** and **Remarks** are listed on the next page.)

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

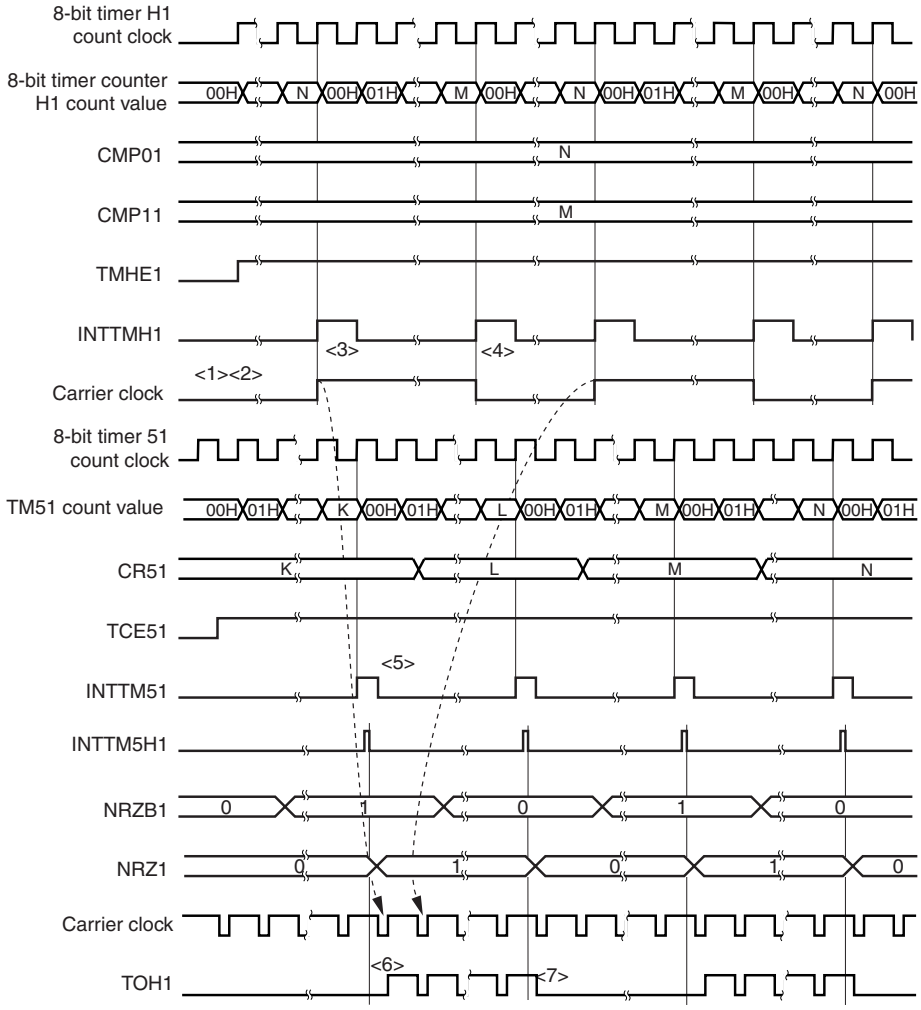
4. The actual TOH1/P31/INTP3 pin output is determined depending on PM31 and P31, besides TOH1 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. f_{RL}: Internal low-speed oscillation clock frequency

Figure 8-17. Carrier Generator Mode Operation Timing (2/3)

(b) Operation when CMP01 = N, CMP11 = M



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to other than 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

<6> A carrier signal is output at the first rising edge of the carrier clock if NRZ1 is set to 1.

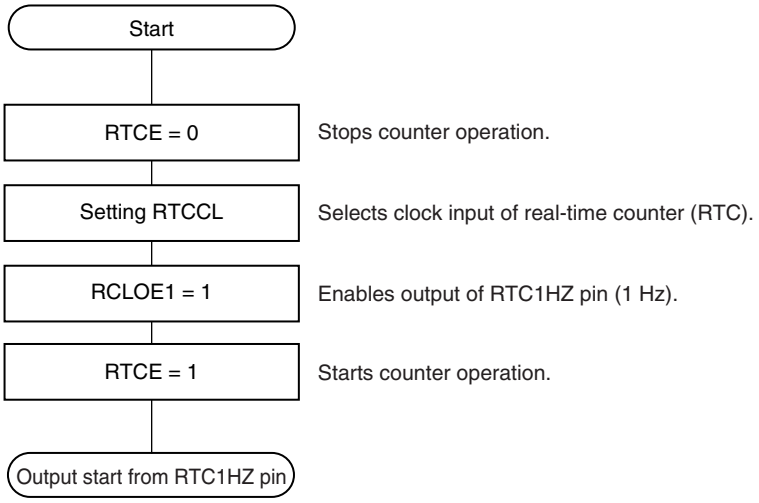
<7> When NRZ1 = 0, the TOH1 output is held at the high level and is not changed to low level while the carrier clock is high level (from <6> and <7>, the high-level width of the carrier clock waveform is guaranteed).

Remark INTTM5H1 is an internal signal and not an interrupt source.

<R> 9.4.5 1 Hz output of real-time counter

Set 1 Hz output after setting 0 to RTCE first.

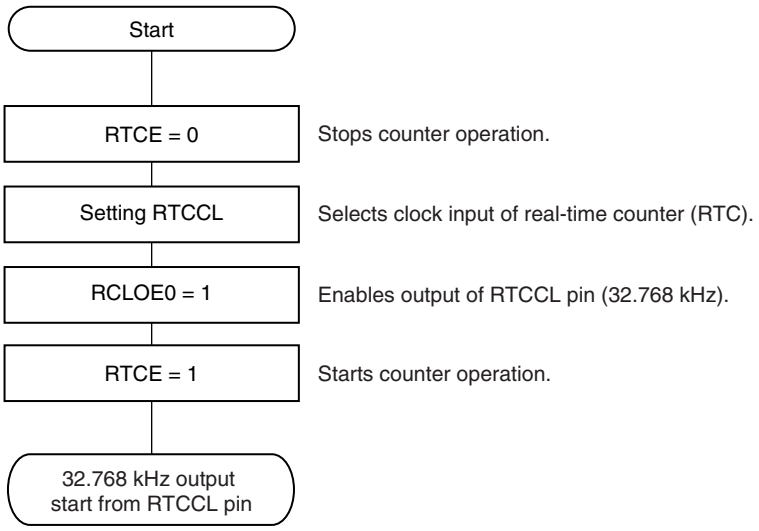
Figure 9-23. 1 Hz Output Setting Procedure



<R> 9.4.6 32.768 kHz output of real-time counter

Set 32.768 kHz output after setting 0 to RTCE first.

Figure 9-24. 32.768 kHz Output Setting Procedure



(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

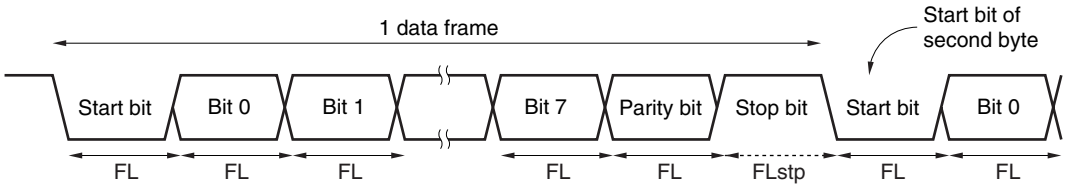
Baud rate = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(5) Data frame length during continuous transmission

When data is continuously transmitted, the data frame length from a stop bit to the next start bit is extended by two clocks of base clock from the normal value. However, the result of communication is not affected because the timing is initialized on the reception side when the start bit is detected.

Figure 15-28. Data Frame Length During Continuous Transmission



Where the 1-bit data length is FL, the stop bit length is FLstp, and base clock frequency is f_{XCLK6}, the following expression is satisfied.

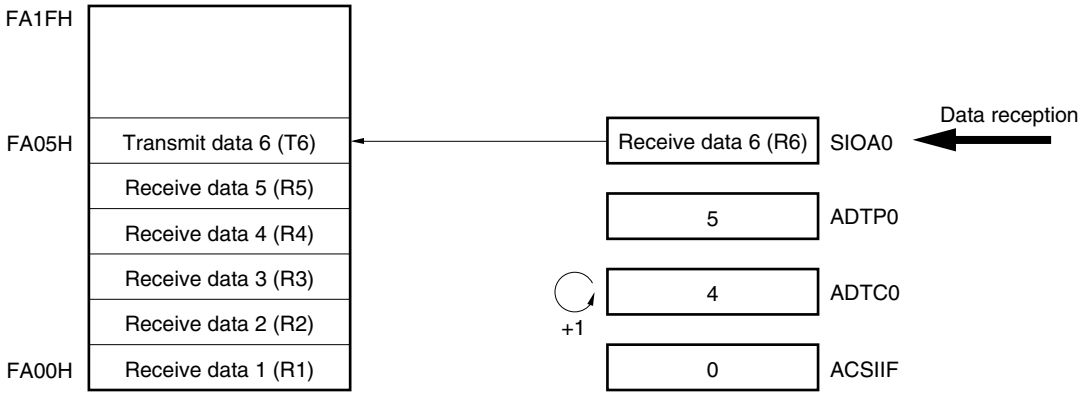
$$FLstp = FL + 2/f_{XCLK6}$$

Therefore, the data frame length during continuous transmission is:

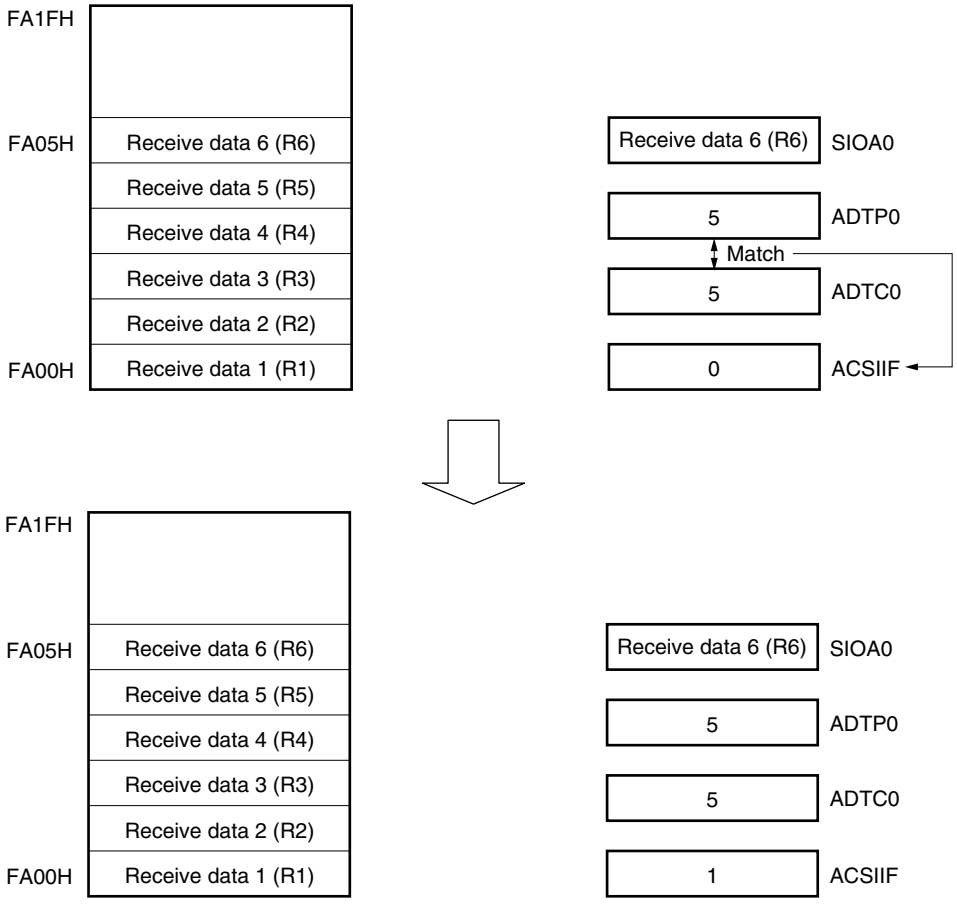
$$\text{Data frame length} = 11 \times FL + 2/f_{XCLK6}$$

Figure 17-17. Internal Buffer RAM Operation in Automatic Transmission/Reception Mode (End of Transmission/Reception)

<1> End of 6th byte transmission/reception



<2> End of automatic transmission/reception



<R>

CHAPTER 18 LCD CONTROLLER/DRIVER

18.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the 78K0/LF3 are as follows.

(1) The LCD driver voltage generator can switch external resistance division and internal resistance division.
(2) Automatic output of segment and common signals based on automatic display data memory read
(3) Six different display modes:
- Static
- 1/2 duty (1/2 bias)
- 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)
- 1/8 duty (1/4 bias)

(4) Six different frame frequencies, selectable in each display mode
(5) μPD78F047x: Segment signal outputs: 40[Note] (SEG0 to SEG39),
Common signal outputs: 8[Note] (COM0 to COM7)
μPD78F048x: Segment signal outputs: 40[Note] (SEG0 to SEG39),
Common signal outputs: 8[Note] (COM0 to COM7)
μPD78F049x: Segment signal outputs: 32[Note] (SEG0 to SEG31),
Common signal outputs: 8[Note] (COM0 to COM7)
(6) Output of LCD segment signals and time division output of segment key source signals in each display mode (except static mode)
Segment key source signal outputs: Max. 8 (SEG24 (KS0) to SEG31 (KS7))

Note The four segment signal outputs (SEG0 to SEG3) and four common signal outputs (COM4 to COM7) are alternate-function pins. COM4 to COM7 can be used only when eight-time-slice mode is selected by the setting of the LCD display mode register (LCDM).

(4) Remote controller receive GPLS compare register (RMGPLS) (Type B reception mode)

This register is used to detect the low level of a remote controller guide pulse (short side).

RMGPLS is set with an 8-bit memory manipulation instruction.

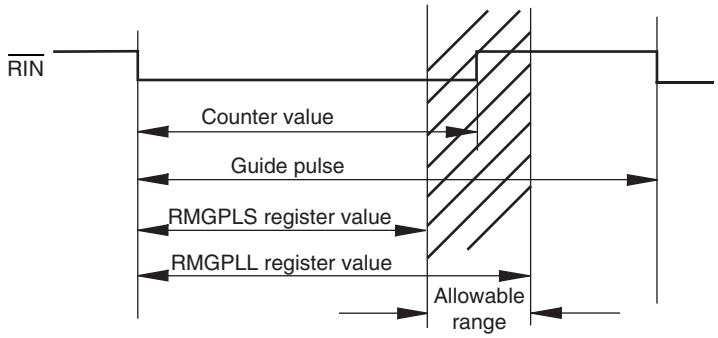
Reset signal generation sets RMGPLS to 00H.

(5) Remote controller receive GPLL compare register (RMGPLL) (Type B reception mode)

This register is used to detect the low level of a remote controller guide pulse (long side).

RMGPLL is set with an 8-bit memory manipulation instruction.

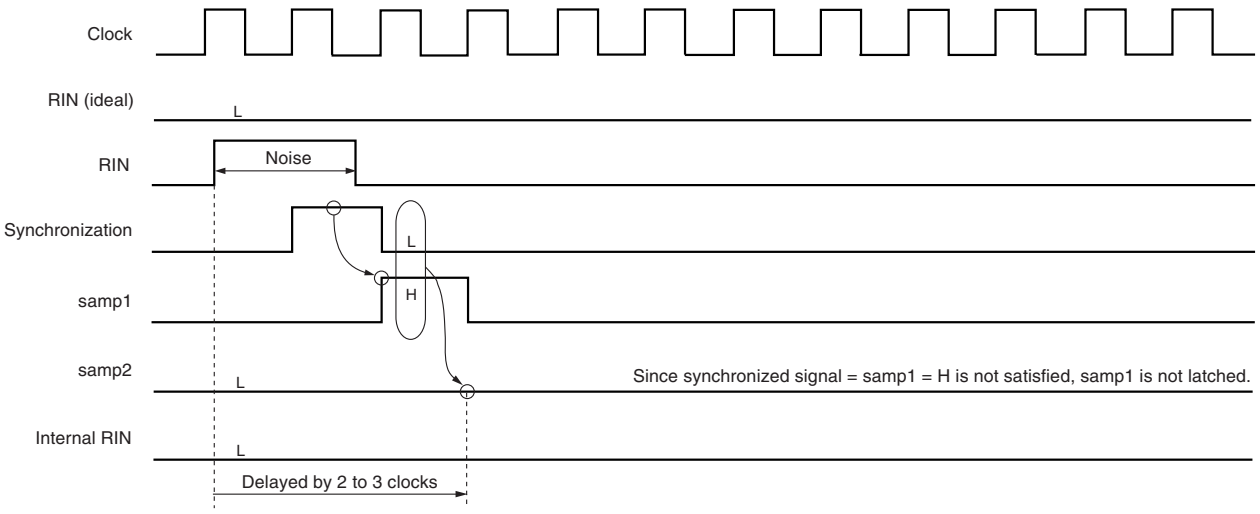
Reset signal generation sets RMGPLL to 00H.



If RMGPLS ≤ counter value < RMGPLL is satisfied, it is assumed that the low level of the guide pulse has been successfully received.

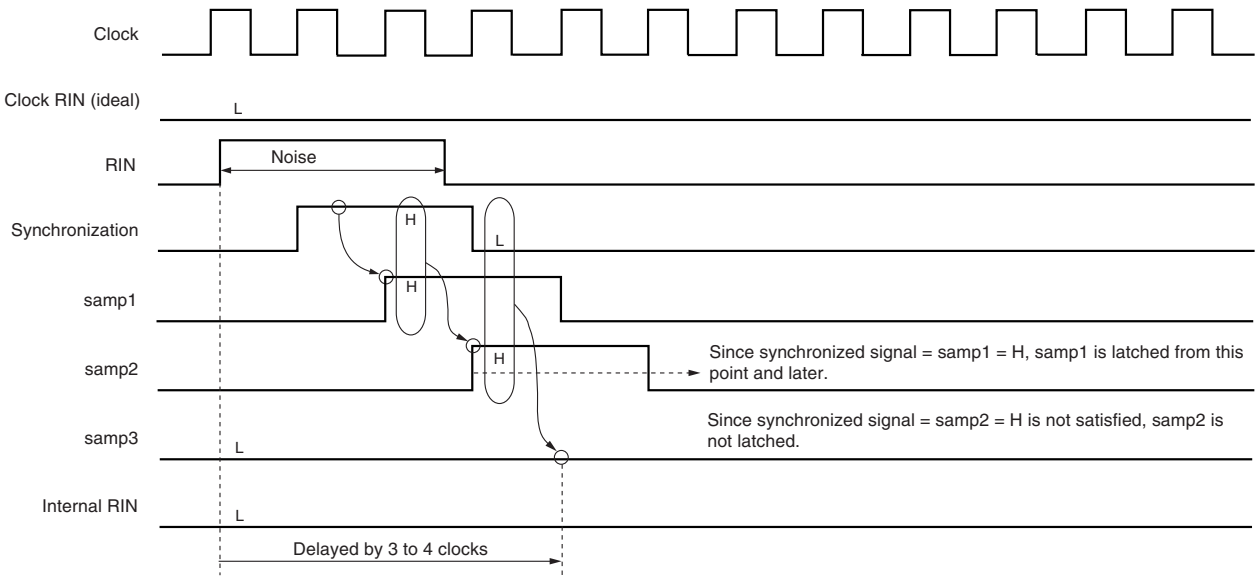
Figure 20-16. Noise Elimination Operation Example (1/2)

(a) 1-clock noise elimination (PRSEN = 0, NCW = 0)



Remark Internal RIN is a signal after synchronization and sampling are performed twice, and is therefore later than the actual signal input from the outside to the RIN pin by two to three clocks.

(b) 2-clock noise elimination (PRSEN = 0, NCW = 1)

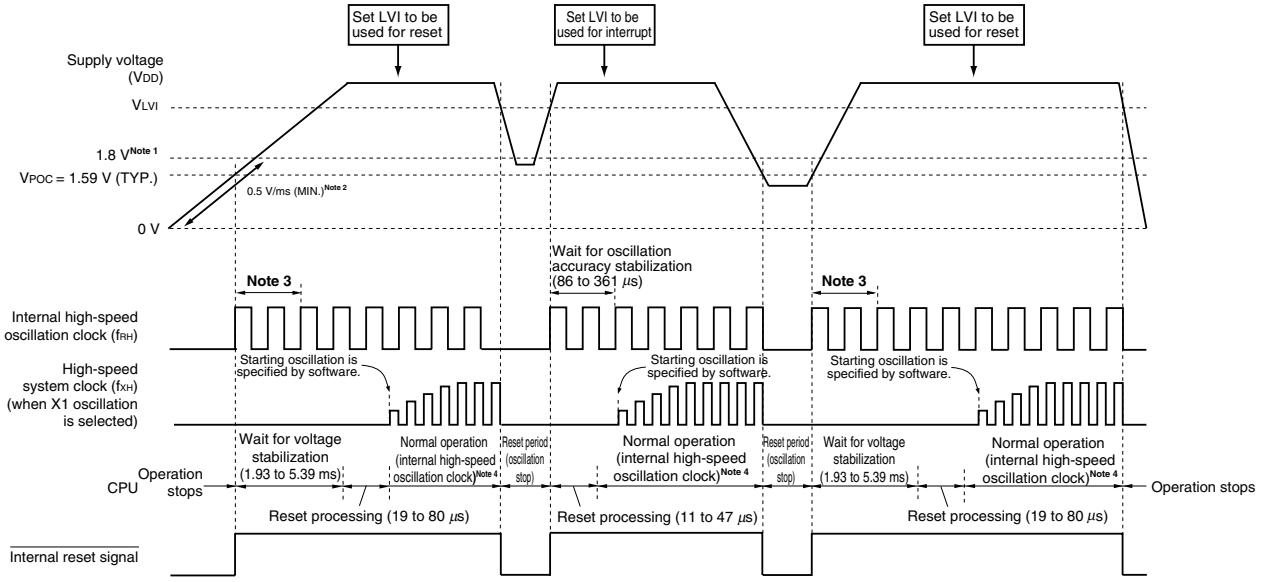


Remark Internal RIN is a signal after synchronization and sampling are performed three times, and is therefore later than the actual signal input from the outside to the RIN pin by 3 to 4 clocks.

<R>

Figure 25-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)

(1) In 1.59 V POC mode (option byte: POCMODE = 0)



Notes 1. The operation guaranteed range is 1.8 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 1.8 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. If the voltage rises to 1.8 V at a rate slower than 0.5 V/ms (MIN.) on power application, input a low level to the $\overline{\text{RESET}}$ pin after power application and before the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using an option byte (POCMODE = 1).

3. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

4. The internal high-speed oscillation clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

Caution Set the low-voltage detector by software after the reset status is released (see CHAPTER 26 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POC}: POC detection voltage

DC Characteristics (5/5)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Watchdog timer operating current	I_{WDT} Note 1	During 240 kHz internal low-speed oscillation clock operation			5	10	μA
LVI operating current	I_{LVI} Note 2				9	18	μA
Successive approximation type A/D converter operating current	I_{ADC1} Note 3		2.3 V ≤ AV_{REF} ≤ V_{DD}		0.86	1.9	mA
<R> ΔΣ type A/D converter operating current	I_{ADC2} Note 3		2.7 V ≤ AV_{REF} ≤ V_{DD}		1.4	2.7	mA
LCD operating current	I_{LCD1} Note 4	LCD display off (deselect signal output) (LCDON = 0, SCOC = 1)	V_{DD} = 5.0 V		3.0	8.0	μA
			V_{DD} = 3.0 V		2.0	5.0	μA
	I_{LCD2} Note 4	LCD display on (LCDON = 1, SCOC = 1)	V_{DD} = 5.0 V		3.0	8.0	μA
			V_{DD} = 3.0 V		2.0	5.0	μA

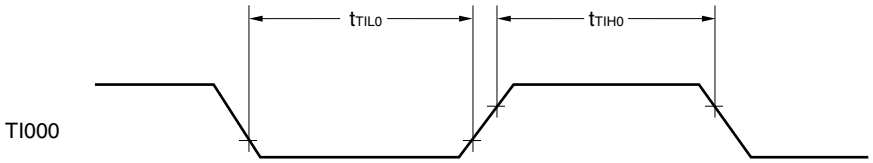
Notes 1. This includes only the current that flows through the watchdog timer (including the operating current of the 240 kHz internal oscillator). When the watchdog timer is operating in HALT mode or STOP mode, the current value of the 78K0/LF3 is obtained by adding I_{WDT} to I_{DD2} or I_{DD3}.

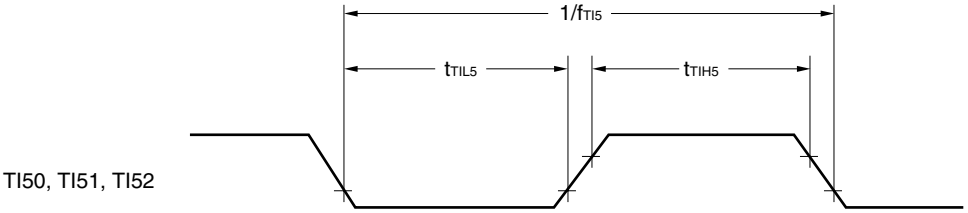
2. This includes only the current that flows through the LVI circuit. When the LVI circuit is operating in HALT mode or STOP mode, the current value of the 78K0/LF3 is obtained by adding I_{LVI} to I_{DD2} or I_{DD3}.

3. This includes only the current that flows through the A/D converter (AV_{REF}). When the A/D converter is operating in HALT mode or STOP mode, the current value of the 78K0/LF3 is obtained by adding I_{ADC1} or I_{ADC2} to I_{DD1} or I_{DD2}.

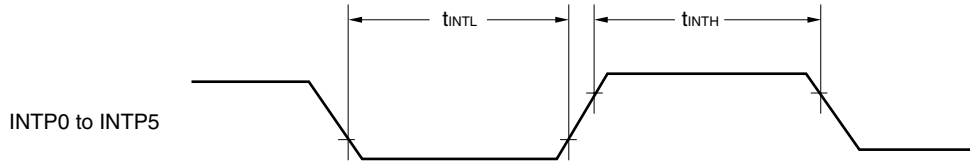
4. This includes only the current that flows through the LCD controller/driver. Not including the current that flows through the LCD divider resistor. The current value of the 78K0/LF3 is obtained by adding the LCD operating current (I_{LCD1} or I_{LCD2}) to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).

TI Timing

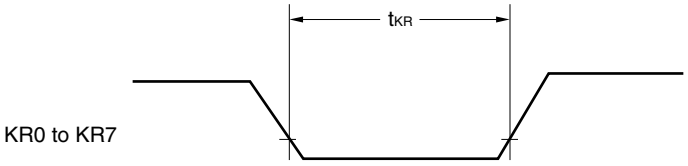




Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing