Renesas Electronics America Inc - UPD78F0493GK-GAK-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b, 3x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0493gk-gak-ax

(2) Non-port pins **(1/4)**

Function Name	I/O	Function	After Reset	Alternate Function
ANI0[Note 2]	Input	10-bit successive approximation type A/D converter analog input.	Digital input port	P20/SEG39[Note 1]/ DS0−[Note 3]
ANI1[Note 2]				P21/SEG38[Note 1]/ DS0+[Note 3]
ANI2[Note 2]				P22/SEG37[Note 1]/ DS1−[Note 3]
ANI3[Note 2]				P23/SEG36[Note 1]/ DS1+[Note 3]
ANI4[Note 2]				P24/SEG35[Note 1]/ DS2−[Note 3]
ANI5[Note 2]				P25/SEG34[Note 1]/ DS2+[Note 3]
ANI6[Note 2]				P26/SEG33[Note 1]/ REF−[Note 3]
ANI7[Note 2]				P27/SEG32[Note 1]/ REF+[Note 3]
DS0−[Note 3]	Input	16-bit ΔΣ type A/D converter analog input.	Digital input port	P20 /ANI0[Note 2]
DS0+[Note 3]				P21/ANI1[Note 2]
DS1−[Note 3]				P22/ANI2[Note 2]
DS1+[Note 3]				P23/ANI3[Note 2]
DS2−[Note 3]				P24/ANI4[Note 2]
DS2+[Note 3]				P25/ANI5[Note 2]
REF−[Note 3]		16-bit ΔΣ type A/D converter reference voltage input. Make the same potential as V_{SS} and AV_{SS}.		P26/ANI6[Note 2]
REF+[Note 3]		16-bit ΔΣ type A/D converter reference voltage input. Make the same potential as AV_{REF}.		P27/ANI7[Note 2]
AV_{REF}[Note 2]	Input	10-bit successive approximation type A/D converter reference voltage input, positive power supply for port 2, and 16-bit ΔΣ type A/D converter [Note3]	–	–
AV_{SS}[Note 2]	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

3. μPD78F049x only.

Table 2-2. Pin I/O Circuit Types (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P110/SEG16, P111/SEG17	17-P	I/O	<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P112/SEG18/TxD6			
P113/SEG19/RxD6	17-Q		
P120/INTP0/EXLVI	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P121/X1/OCD0A[Note 1]	37-A	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK/OCD0B[Note 1]			
P123/XT1[Note 1]			
P124/XT2[Note 1]			
P130/SEG20 to P133/SEG23	17-P	I/O	<Port setting> Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open. <Segment setting> Leave open.
P140/SEG24 (KS0) to P143/SEG27 (KS3)			
P150/SEG28 (KS4) to P153/SEG31 (KS7)			
COM0 to COM3	18-E	Output	Leave open.
COM4/SEG0 to COM7/SEG3	18-F		
V_{LC0} to V_{LC2}	–	–	
$\overline{\text{RESET}}$	2	Input	Connect directly or via a resistor to V_{DD}.
FLMD0	38		Connect to V_{SS}.[Note 3]
AV_{REF}[Note 2]	–	–	Connect directly to V_{DD}.[Note 4]
AV_{SS}[Note 2]			Connect directly to V_{SS}.

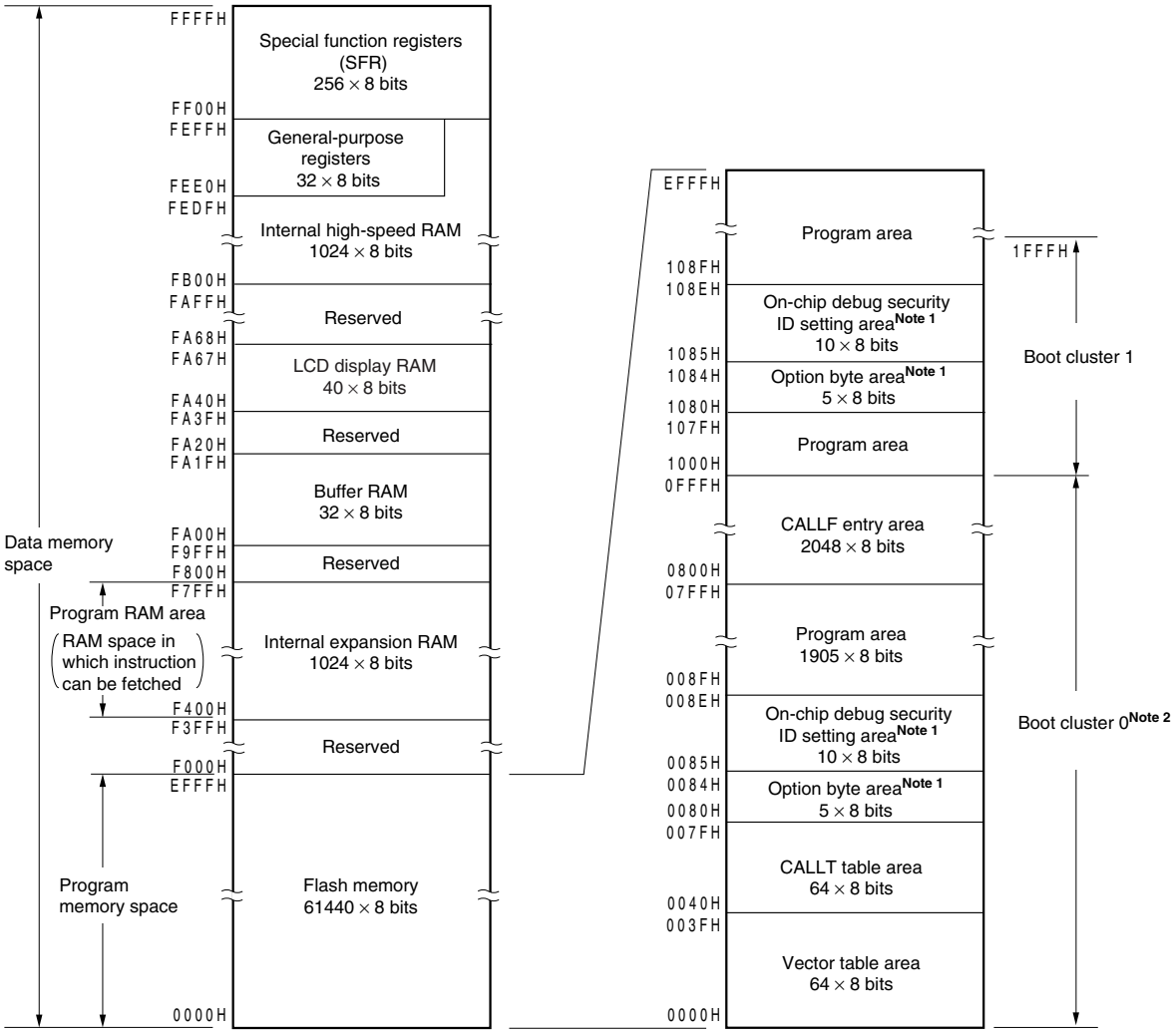
Notes 1. Use recommended connection above in I/O port mode (see **Figure 5-2 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

2. μPD78F048x and 78F049x only.

3. FLMD0 is a pin used when writing data to flash memory. When rewriting flash memory data on-board or performing on-chip debugging, connect this pin to V_{SS} via a resistor (10 kΩ: recommended).

4. When using port 2 as a digital port or for segment output, set it to the same potential as that of V_{DD}.

Figure 3-9. Memory Map (μPD78F0475, 78F0485)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (see **28.8 Security Setting**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.

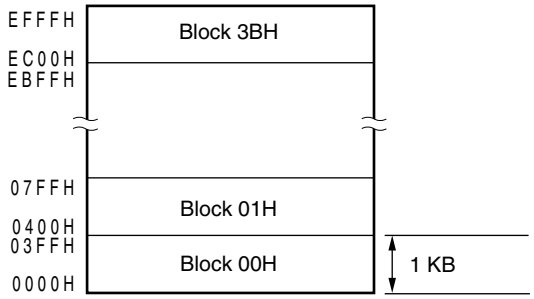
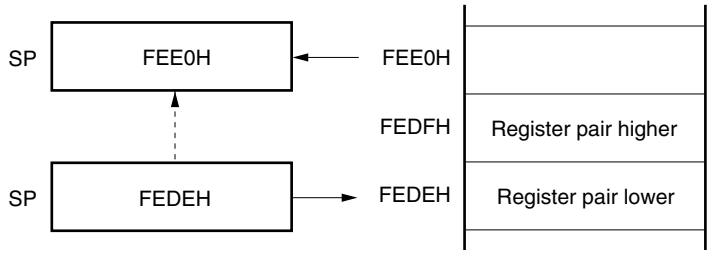
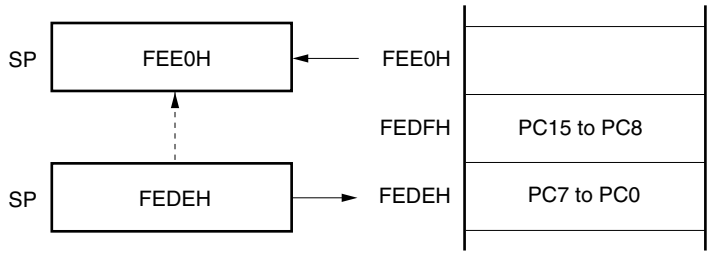


Figure 3-25. Data to Be Restored from Stack Memory

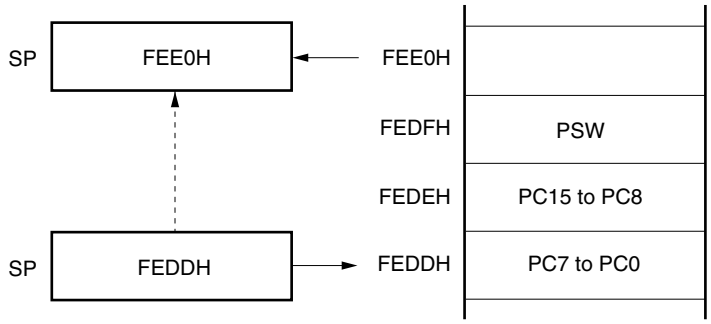
(a) POP rp instruction (when SP = FEDEH)



(b) RET instruction (when SP = FEDEH)



(c) RETI, RETB instructions (when SP = FEDDH)



3.4.2 Register addressing

[Function]

The general-purpose register to be specified is accessed as an operand with the register bank select flags (RBS0 to RBS1) and the register specify codes of an operation code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

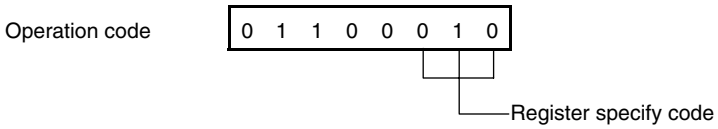
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

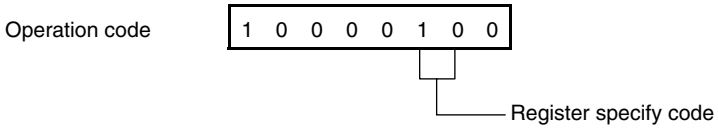
'r' and 'rp' can be described by absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp



3.4.6 Register indirect addressing

[Function]

Register pair contents specified by a register pair specify code in an instruction word and by a register bank select flag (RBS0 and RBS1) serve as an operand address for addressing the memory. This addressing can be carried out for all of the memory spaces.

[Operand format]

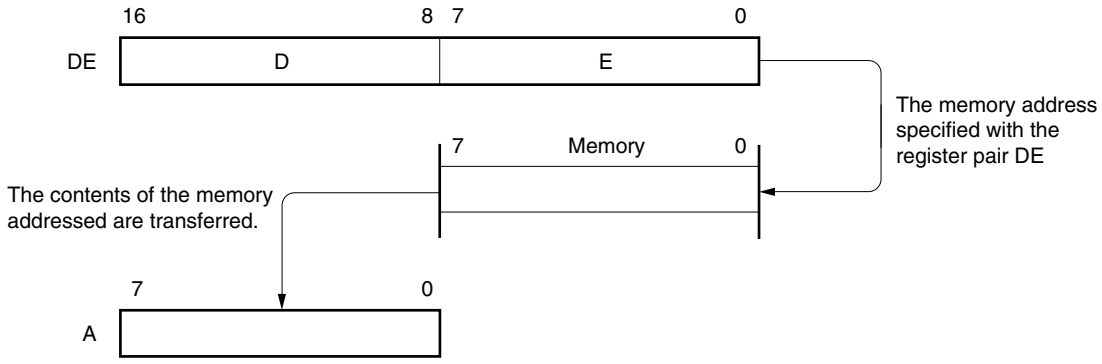
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; when selecting [DE] as register pair

Operation code	1	0	0	0	0	1	0	1

[Illustration]



4.2.6 Port 9

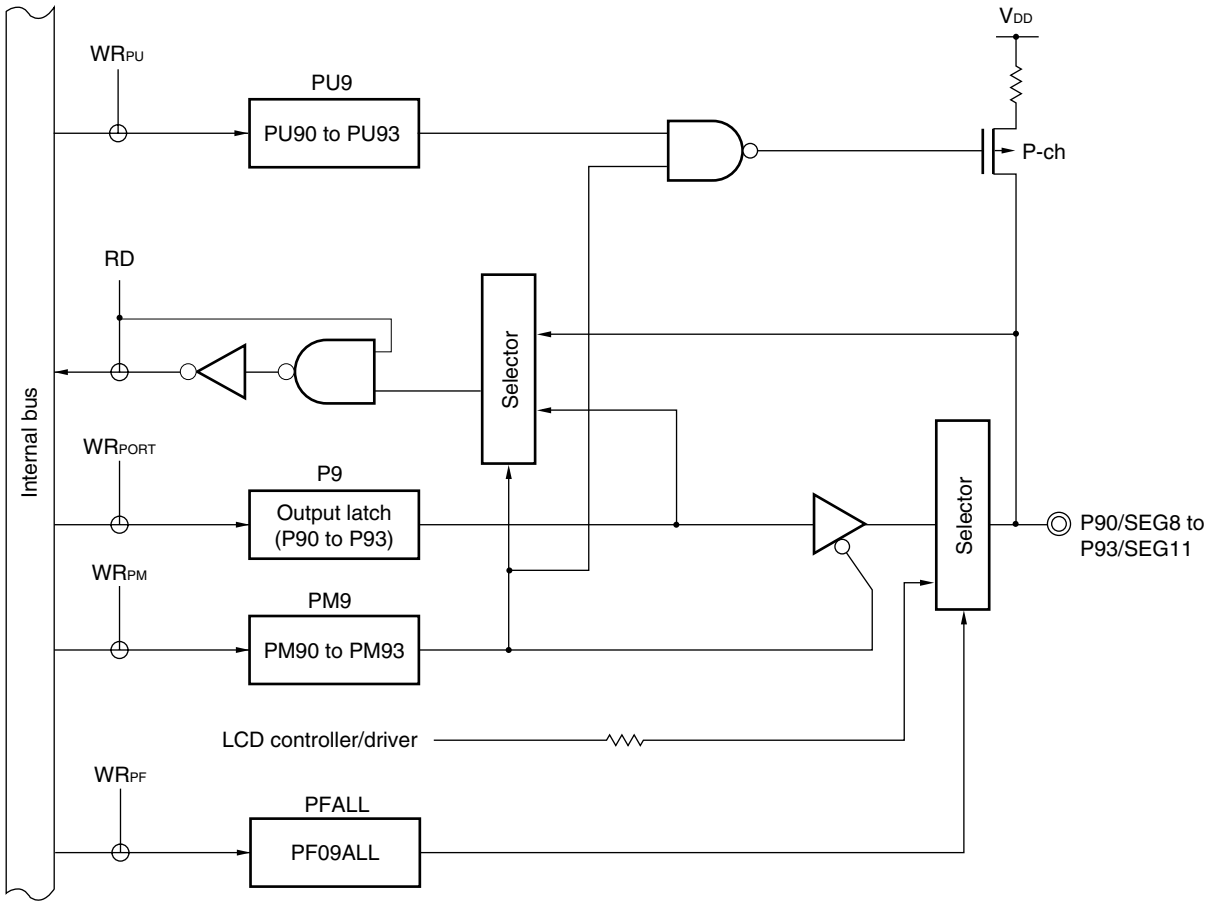
Port 9 is a 4-bit I/O port with an output latch. Port 9 can be set to the input mode or output mode in 1-bit units using port mode register 9 (PM9). When the P90 to P93 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 9 (PU9).

This port can also be used for segment output.

Reset signal generation sets port 9 to input mode.

Figure 4-16 shows block diagrams of port 9.

Figure 4-16. Block Diagram of P90 to P93



P9: Port register 9
PU9: Pull-up resistor option register 9
PM9: Port mode register 9
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

5.4 System Clock Oscillator

5.4.1 X1 oscillator

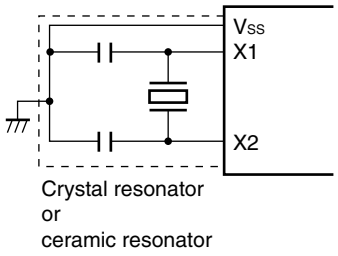
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (2 to 10 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

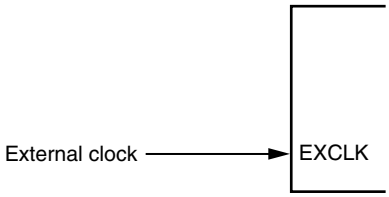
Figure 5-10 shows an example of the external circuit of the X1 oscillator.

Figure 5-10. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



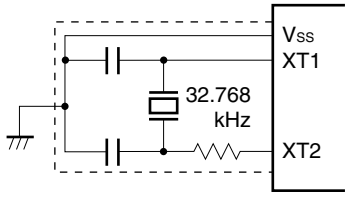
5.4.2 XT1 oscillator

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

Figure 5-11 shows an example of the external circuit of the XT1 oscillator.

Figure 5-11. Example of External Circuit of XT1 Oscillator

(a) Crystal oscillation



Caution 1. When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in the Figures 5-10 and 5-11 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Note that the XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption.

Table 5-5. CPU Clock Transition and SFR Register Setting Examples (3/4)

(6) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(7) CPU clock changing from high-speed system clock (C) to subsystem clock (D)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	OSCSELS	Waiting for Oscillation Stabilization	CSS
(C) → (D)	1	Necessary	1

Unnecessary if the CPU is operating with the subsystem clock

(8) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0	CSS
(D) → (B)	0	Confirm this flag is 1.	0	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

↑ Unnecessary if XSEL is 0

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-15.

2. MCM0: Bit 0 of the main clock mode register (MCM)
OSCSELS: Bit 4 of the clock operation mode select register (OSCCTL)
RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)
CSS: Bit 4 of the processor clock control register (PCC)

Table 5-8. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		$1 + 2f_{RH}/f_{XH}$ clock
1	$1 + 2f_{XH}/f_{RH}$ clock	

Caution When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

Remarks 1. The number of clocks listed in Table 5-8 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-8 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{RH} = 8 MHz, f_{XH} = 10 MHz)

$1 + 2f_{RH}/f_{XH} = 1 + 2 \times 8/10 = 1 + 2 \times 0.8 = 1 + 1.6 = 2.6 \rightarrow 2$ clocks

5.6.9 Conditions before clock oscillation is stopped

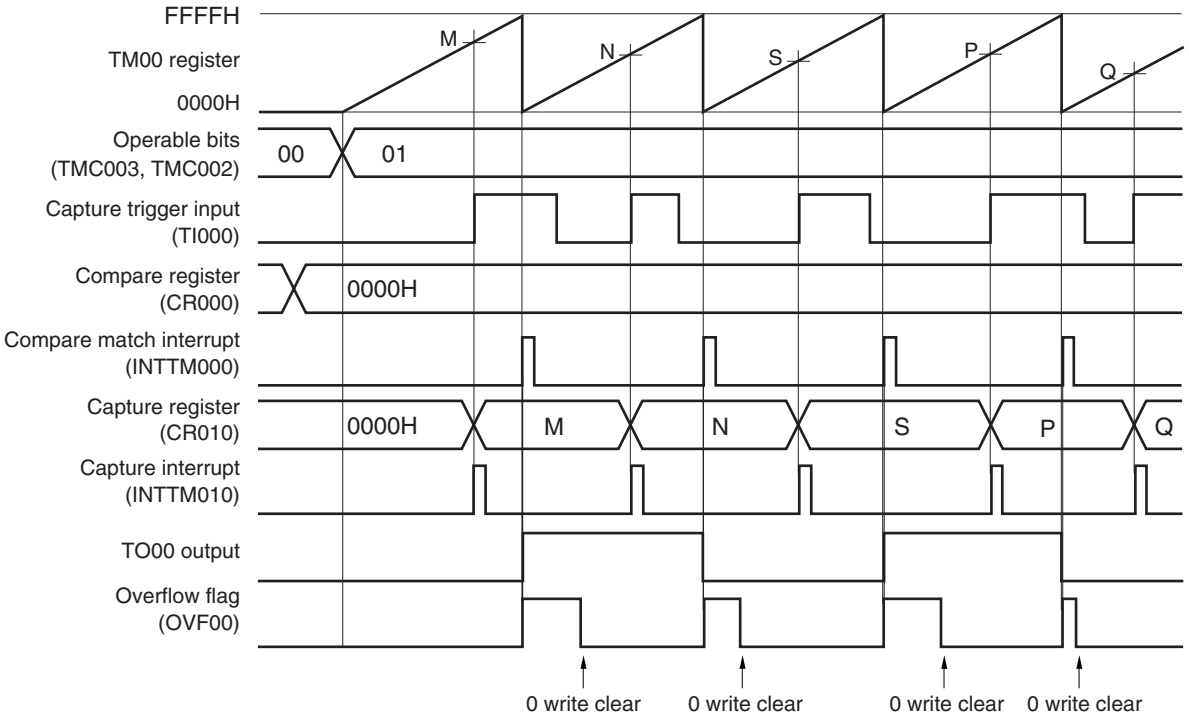
The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-9. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 or CLS = 1 (The CPU is operating on a clock other than the internal high-speed oscillation clock)	RSTOP = 1
X1 clock External main system clock	MCS = 0 or CLS = 1 (The CPU is operating on a clock other than the high-speed system clock)	MSTOP = 1
XT1 clock	CLS = 0 (The CPU is operating on a clock other than the subsystem clock)	OSCSELS = 0

Figure 6-36. Timing Example of Free-Running Timer Mode (CR000: Compare Register, CR010: Capture Register)

• TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 04H



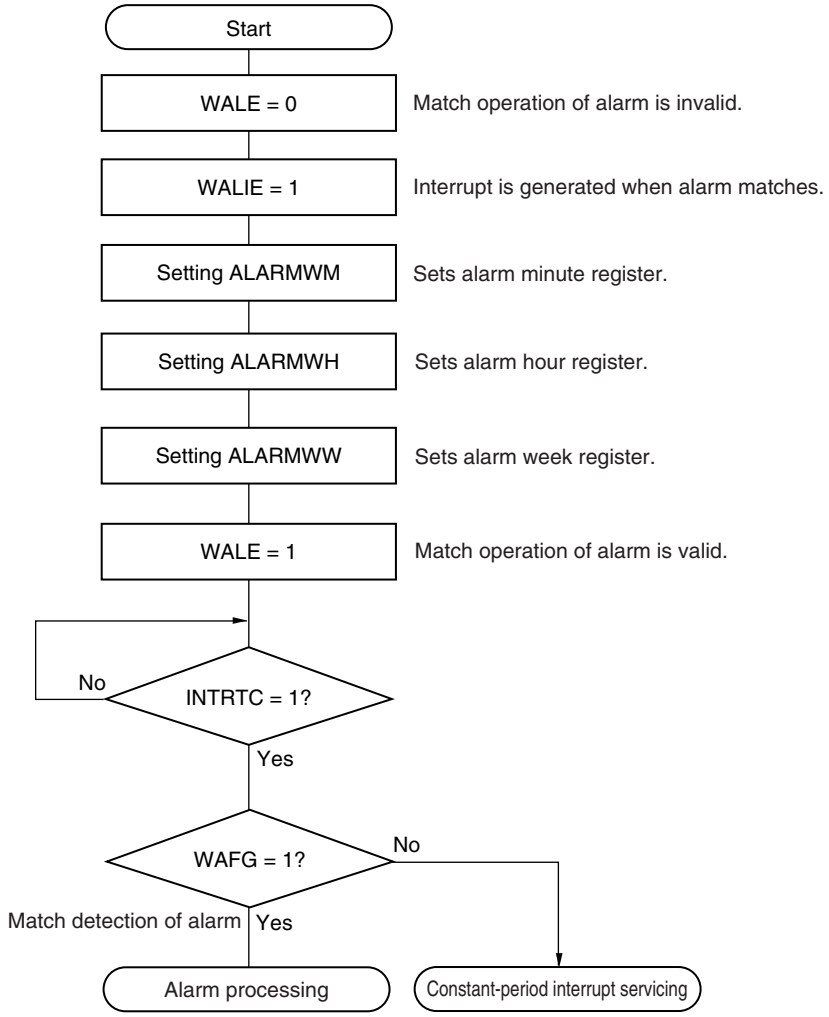
This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

In this example, the INTTM000 signal is generated and the TO00 output is reversed each time the count value of TM00 matches the set value of CR000 (compare register). In addition, the INTTM010 signal is generated and the count value of TM00 is captured to CR010 each time the valid edge of the TI000 pin is detected.

9.4.4 Setting alarm of real-time counter

Set time of alarm after setting 0 to WALE first.

Figure 9-22. Alarm Setting Procedure



Remarks 1. ALARMWM, ALARMWH, and ALARMWW may be written in any sequence.

2. Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

(5) Port mode register 1 (PM1)

This register sets port 1 input/output in 1-bit units.

When using the P13/SO10/TxD0 pin for serial interface data output, clear PM13 to 0. The output latch of P13 at this time may be 0 or 1.

When using the P12/SI10/RxD0 pin for serial interface data input, set PM12 to 1. The output latch of P12 at this time may be 0 or 1.

PM1 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 14-6. Format of Port Mode Register 1 (PM1)

Address: FF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

PM1n	P1n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(2) Generation of serial clock

A serial clock to be generated can be specified by using baud rate generator control register 0 (BRGC0).

Select the clock to be input to the 5-bit counter by using bits 7 and 6 (TPS01 and TPS00) of BRGC0.

Bits 4 to 0 (MDL04 to MDL00) of BRGC0 can be used to select the division value (f_{XCLK0}/8 to f_{XCLK0}/31) of the 5-bit counter.

14.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK0}}{2 \times k}$ [bps]

f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits of the BRGC0 register

k: Value set by the MDL04 to MDL00 bits of the BRGC0 register (k = 8, 9, 10, ..., 31)

Table 14-4. Set Value of TPS01 and TPS00

TPS01	TPS00	Base clock (f_{XCLK0}) selection[Note 1]				
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 8 MHz	f_{PRS} = 10 MHz
0	0	TM50 output[Note 2]				
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	4 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1 MHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	250 kHz	312.5 kHz

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- Error (%) = $\left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1\right) \times 100$ [%]

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

(2) Asynchronous serial interface reception error status register 6 (ASIS6)

This register indicates an error status on completion of reception by serial interface UART6. It includes three error flag bits (PE6, FE6, OVE6).

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 5 (RXE6) of ASIM6 to 0 clears this register to 00H. 00H is read when this register is read. If a reception error occurs, read ASIS6 and then read receive buffer register 6 (RXB6) to clear the error flag.

Figure 15-6. Format of Asynchronous Serial Interface Reception Error Status Register 6 (ASIS6)

Address: FF53H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS6	0	0	0	0	0	PE6	FE6	OVE6

PE6	Status flag indicating parity error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the parity of transmit data does not match the parity bit on completion of reception

FE6	Status flag indicating framing error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the stop bit is not detected on completion of reception

OVE6	Status flag indicating overrun error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If receive data is set to the RXB6 register and the next reception operation is completed before the data is read.

Cautions 1. The operation of the PE6 bit differs depending on the set values of the PS61 and PS60 bits of asynchronous serial interface operation mode register 6 (ASIM6).

2. For the stop bit of the receive data, only the first stop bit is checked regardless of the number of stop bits.

3. If an overrun error occurs, the next receive data is not written to receive buffer register 6 (RXB6) but discarded.

4. If data is read from ASIS6, a wait cycle is generated. Do not read data from ASIS6 when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 34 CAUTIONS FOR WAIT.

(1) Serial I/O shift register 0 (SIOA0)

This is an 8-bit register used to store transmit/receive data in 1-byte transfer mode (bit 6 (ATE0) of serial operation mode specification register 0 (CSIMA0) = 0). Writing transmit data to SIOA0 starts the communication. In addition, after a communication completion interrupt request (INTACSI) is output (bit 0 (TSF0) of serial status register 0 (CSIS0) = 0), data can be received by reading data from SIOA0.

This register can be written or read by an 8-bit memory manipulation instruction. However, writing to SIOA0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

Reset signal generation clears this register to 00H.

Cautions 1. A communication operation is started by writing to SIOA0. Consequently, when transmission is disabled (bit 3 (TXEA0) of CSIMA0 = 0), write dummy data to the SIOA0 register to start the communication operation, and then perform a receive operation.

2. Do not write data to SIOA0 while the automatic transmit/receive function is operating.

17.3 Registers Controlling Serial Interface CSIA0

Serial interface CSIA0 is controlled by the following ten registers.

- Serial operation mode specification register 0 (CSIMA0)
- Serial status register 0 (CSIS0)
- Serial trigger register 0 (CSIT0)
- Divisor selection register 0 (BRGCA0)
- Automatic data transfer address point specification register 0 (ADTP0)
- Automatic data transfer interval specification register 0 (ADTI0)
- Automatic data transfer address count register 0 (ADTC0)
- Port function register 1 (PF1)
- Port mode register 1 (PM1)
- Port register 1 (P1)

Table 18-1 lists the maximum number of pixels that can be displayed in each display mode.

Table 18-1. Maximum Number of Pixels

(a) μPD78F047x, 78F048x

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	40	40 (40 segment signals, 1 common signal)Note 2
	1/2	2 Note 1	COM0, COM1		80 (40 segment signals, 2 common signals)Note 3
		3 Note 1	COM0 to COM2		120 (40 segment signals, 3 common signals)Note 4
	1/3	3 Note 1	COM0 to COM2		
		4 Note 1	COM0 to COM3		160 (40 segment signals, 4 common signals)Note 5
	1/4	8 Note 1	COM0 to COM7	36	288 (36 segment signals, 8 common signals)Note 6

Notes 1. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

2. 5-digit LCD panel, each digit having an 8-segment 8. configuration.

3. 10-digit LCD panel, each digit having a 4-segment 8. configuration.

4. 15-digit LCD panel, each digit having a 3-segment 8. configuration.

5. 20-digit LCD panel, each digit having a 2-segment 8. configuration.

6. 36-digit LCD panel, each digit having a 1-segment 8. configuration.

(b) μPD78F049x

LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	32	32 (32 segment signals, 1 common signal)Note 2
	1/2	2 Note 1	COM0, COM1		64 (32 segment signals, 2 common signals)Note 3
		3 Note 1	COM0 to COM2		96 (32 segment signals, 3 common signals)Note 4
	1/3	3 Note 1	COM0 to COM2		
		4 Note 1	COM0 to COM3		128 (32 segment signals, 4 common signals)Note 5
	1/4	8 Note 1	COM0 to COM7	28	224 (28 segment signals, 8 common signals)Note 6

Notes 1. When using the segment key scan function (KSON = 1), “number of time slices + 1” is added for segment key scan signal output.

2. 4-digit LCD panel, each digit having an 8-segment 8. configuration.

3. 8-digit LCD panel, each digit having a 4-segment 8. configuration.

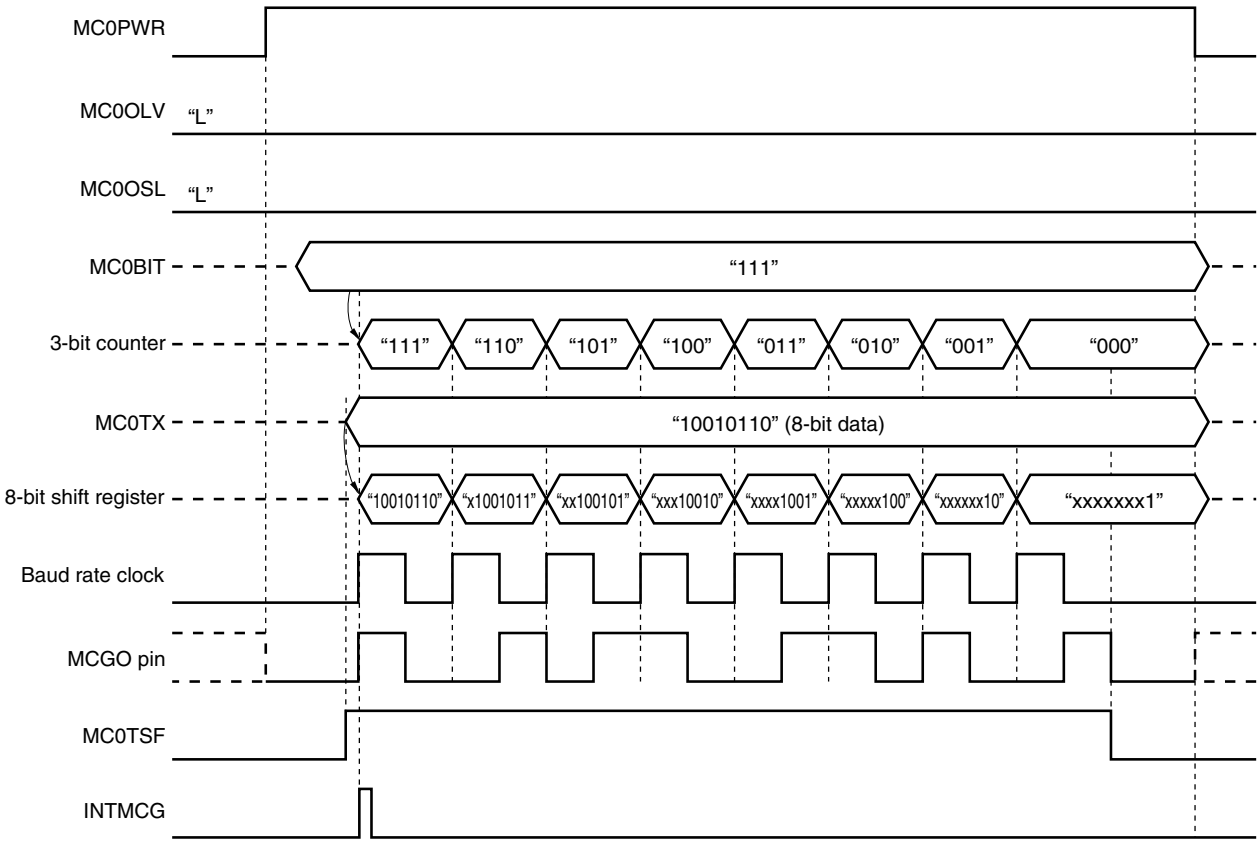
4. 12-digit LCD panel, each digit having a 3-segment 8. configuration.

5. 16-digit LCD panel, each digit having a 2-segment 8. configuration.

6. 28-digit LCD panel, each digit having a 1-segment 8. configuration.

Figure 19-8. Timing of Manchester Code Generator Mode (LSB First) (2/4)

(2) Transmit timing (MC0OLV = 0, total transmit bit length = 8 bits)



(6) Remote controller receive GPHS compare register (RMGPHS) (Type A, Type B reception mode only)

This register is used to detect the high level of a remote controller guide pulse (short side).

RMGPHS is set with an 8-bit memory manipulation instruction.

Reset signal generation sets RMGPHS to 00H.

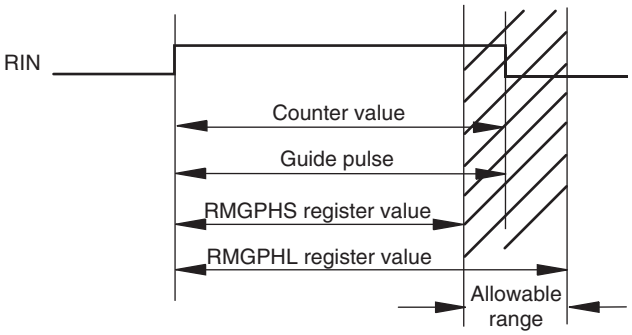
(7) Remote controller receive GPHL compare register (RMGPHL) (Type A, Type B reception mode only)

This register is used to detect the high level of a remote controller guide pulse (long side).

RMGPHL is set with an 8-bit memory manipulation instruction.

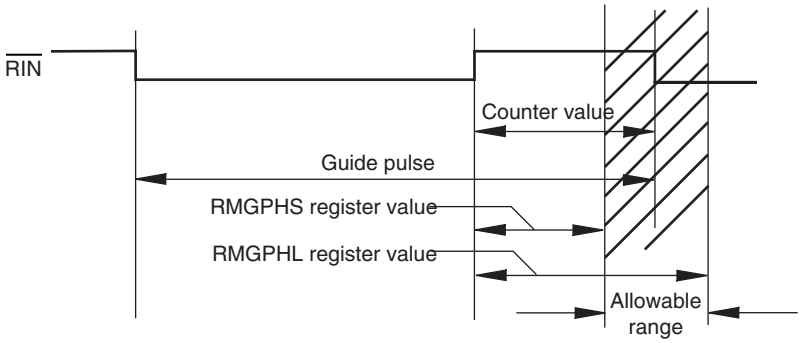
Reset signal generation sets RMGPHL to 00H.

(a) Type A reception mode



If RMGPHS ≤ counter value < RMGPHL is satisfied, it is assumed that the high level of the guide pulse has been successfully received.

(b) Type B reception mode



If RMGPHS ≤ counter value < RMGPHL is satisfied, it is assumed that the high level of the guide pulse has been successfully received.

20.4.9 Error interrupt generation timing

(1) Type A reception mode

After the guide pulse has been detected normally, the INTRERR signal is generated under any of the following conditions.

- Counter < RMDLS at the rising edge of RIN
- RMDLL ≤ counter and counter after RMDLL < RMER at the rising edge of RIN
- Counter < RMDH0S at the falling edge of RIN
- RMDH0L ≤ counter < RMDH1S at the falling edge of RIN
- Register changes so that RMDH1L ≤ counter while RIN is at high level

The INTRERR signal is not generated until the guide pulse is detected.

Once the INTRERR signal has been generated, it will not be generated again until the next guide pulse is detected. The generation timing of the INTRERR signal is shown in Figure 20-13.