# Renesas Electronics America Inc - UPD78F0495GC-GAD-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0 |
| Core Size | 8-Bit |
| Speed | 10MHz |
| Connectivity | 3-Wire SIO, LINbus, UART/USART |
| Peripherals | LCD, LVD, POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 60KB (60K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b, 3x16b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0495gc-gad-ax |

### 3.4.3 Direct addressing

**[Function]**

The memory to be manipulated is directly addressed with immediate data in an instruction word becoming an operand address.

**[Operand format]**

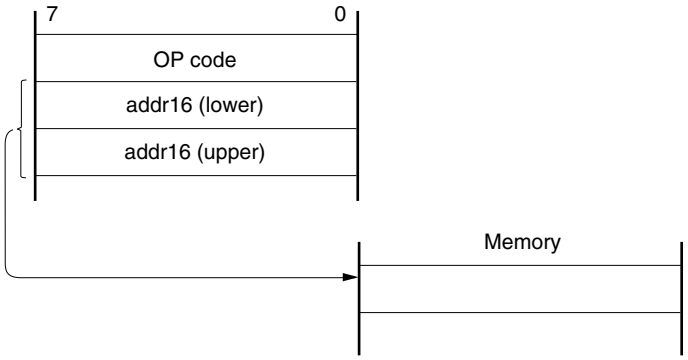
| Identifier | Description |
|---|---|
| addr16 | Label or 16-bit immediate data |

**[Description example]**

MOV A, !0FE00H; when setting !addr16 to FE00H

| | | |
|---|---|---|
| Operation code | 1 0 0 0 1 1 1 0 | OP code |
| | 0 0 0 0 0 0 0 0 | 00H |
| | 1 1 1 1 1 1 1 0 | FEH |

**[Illustration]**



**(2) Port registers (P1 to P4, P8 to P15)**

These registers write the data that is output from the chip when data is output from a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 4-28. Format of Port Register**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P1 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | FF01H | 00H (output latch) | R/W |
| P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | FF02H | 00H (output latch) | R/W |
| P3 | 0 | 0 | 0 | P34 | P33 | P32 | P31 | P30 | FF03H | 00H (output latch) | R/W |
| P4 | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | FF04H | 00H (output latch) | R/W |
| P8 | 0 | 0 | 0 | 0 | P83 | P82 | P81 | P80 | FF08H | 00H (output latch) | R/W |
| P9 | 0 | 0 | 0 | 0 | P93 | P92 | P91 | P90 | FF09H | 00H (output latch) | R/W |
| P10 | 0 | 0 | 0 | 0 | P103 | P102 | P101 | P100 | FF0AH | 00H (output latch) | R/W |
| P11 | 0 | 0 | 0 | 0 | P113 | P112 | P111 | P110 | FF0BH | 00H (output latch) | R/W |
| <R> P12 | 0 | 0 | 0 | P124Note 2 | P123Note 2 | P122Note 2 | P121Note 2 | P120 | FF0CH | 00HNote 1 (output latch) | R/WNote 1 |
| P13 | 0 | 0 | 0 | 0 | P133 | P132 | P131 | P130 | FF0DH | 00H (output latch) | R/W |
| <R> P14 | PK143Note 3 | PK142Note 3 | PK141Note 3 | PK140Note 3 | P143 | P142 | P141 | P140 | FF0EH | 00H (output latch) | R/W |
| <R> P15 | PK153Note 3 | PK152Note 3 | PK151Note 3 | PK150Note 3 | P153 | P152 | P151 | P150 | FF0FH | 00H (output latch) | R/W |

| Pmn | m = 1 to 4, 8 to 15; n = 0 to 7 | |
|---|---|---|
| | Output data control (in output mode) | Input data read (in input mode) |
| 0 | Output 0 | Input low level |
| 1 | Output 1 | Input high level |

<R> **Notes 1.** P121 to P124 are read-only. These become undefined at reset.

<R> **2.** When the operation mode of the pin is the clock input mode, 0 is always read.

<R> **3.** This bit is used for the segment key scan function. For details, see **18.3 Registers Controlling LCD Controller/Driver**.

**(7) Oscillation stabilization time counter status register (OSTC)**

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock or subsystem clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

**Figure 5-7. Format of Oscillation Stabilization Time Counter Status Register (OSTC)**

Address: FFA3H After reset: 00H R

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| OSTC | 0 | 0 | 0 | MOST11 | MOST13 | MOST14 | MOST15 | MOST16 |

| MOST 11 | MOST 13 | MOST 14 | MOST 15 | MOST 16 | Oscillation stabilization time status | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | fx = 2 MHz | fx = 5 MHz | fx = 10 MHz |
| 1 | 0 | 0 | 0 | 0 | $2^{11}$/fx min. | 1.02 ms min. | 409.6 $\mu$s min. | 204.8 $\mu$s min. |
| 1 | 1 | 0 | 0 | 0 | $2^{13}$/fx min. | 4.10 ms min. | 1.64 ms min. | 819.2 $\mu$s min. |
| 1 | 1 | 1 | 0 | 0 | $2^{14}$/fx min. | 8.19 ms min. | 3.27 ms min. | 1.64 ms min. |
| 1 | 1 | 1 | 1 | 0 | $2^{15}$/fx min. | 16.38 ms min. | 6.55 ms min. | 3.27 ms min. |
| 1 | 1 | 1 | 1 | 1 | $2^{16}$/fx min. | 32.77 ms min. | 13.11 ms min. | 6.55 ms min. |

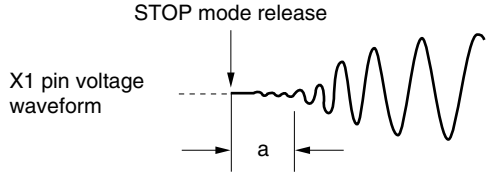
**Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.**

**2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.**

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

**Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.**

**3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).**




**Remark** fx: X1 clock oscillation frequency

<R> **Figure 5-9. Format of Internal High-speed Oscillation Trimming Register (HIOTRM)**

Address: FF30H After reset: 10H R/W

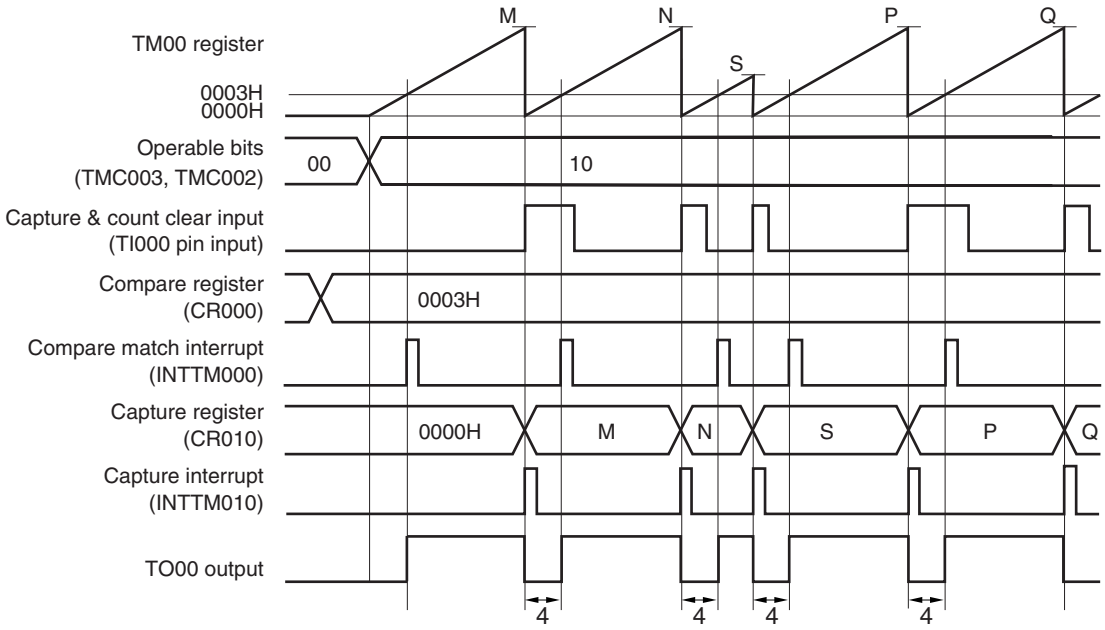
| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| HIOTRM | 0 | 0 | 0 | TTRM4 | TTRM3 | TTRM2 | TTRM1 | TTRM0 |

| TTRM4 | TTRM3 | TTRM2 | TTRM1 | TTRM0 | Clock correction value (2.7 V ≤ $V_{DD}$ ≤ 5.5 V) | | |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | TYP. | MAX. |
| 0 | 0 | 0 | 0 | 0 | –5.54% | –4.88% | –4.02% |
| 0 | 0 | 0 | 0 | 1 | –5.28% | –4.62% | –3.76% |
| 0 | 0 | 0 | 1 | 0 | –4.99% | –4.33% | –3.47% |
| 0 | 0 | 0 | 1 | 1 | –4.69% | –4.03% | –3.17% |
| 0 | 0 | 1 | 0 | 0 | –4.39% | –3.73% | –2.87% |
| 0 | 0 | 1 | 0 | 1 | –4.09% | –3.43% | –2.57% |
| 0 | 0 | 1 | 1 | 0 | –3.79% | –3.13% | –2.27% |
| 0 | 0 | 1 | 1 | 1 | –3.49% | –2.83% | –1.97% |
| 0 | 1 | 0 | 0 | 0 | –3.19% | –2.53% | –1.67% |
| 0 | 1 | 0 | 0 | 1 | –2.88% | –2.22% | –1.36% |
| 0 | 1 | 0 | 1 | 0 | –2.23% | –1.91% | –1.31% |
| 0 | 1 | 0 | 1 | 1 | –1.92% | –1.60% | –1.28% |
| 0 | 1 | 1 | 0 | 0 | –1.60% | –1.28% | –0.96% |
| 0 | 1 | 1 | 0 | 1 | –1.28% | –0.96% | –0.64% |
| 0 | 1 | 1 | 1 | 0 | –0.96% | –0.64% | –0.32% |
| 0 | 1 | 1 | 1 | 1 | –0.64% | –0.32% | ±0% |
| 1 | 0 | 0 | 0 | 0 | ±0% (default) | | |
| 1 | 0 | 0 | 0 | 1 | ±0% | +0.32% | +0.64% |
| 1 | 0 | 0 | 1 | 0 | +0.33% | +0.65% | +0.97% |
| 1 | 0 | 0 | 1 | 1 | +0.66% | +0.98% | +1.30% |
| 1 | 0 | 1 | 0 | 0 | +0.99% | +1.31% | +1.63% |
| 1 | 0 | 1 | 0 | 1 | +1.32% | +1.64% | +1.96% |
| 1 | 0 | 1 | 1 | 0 | +1.38% | +1.98% | +2.30% |
| 1 | 0 | 1 | 1 | 1 | +1.46% | +2.32% | +2.98% |
| 1 | 1 | 0 | 0 | 0 | +1.80% | +2.66% | +3.32% |
| 1 | 1 | 0 | 0 | 1 | +2.14% | +3.00% | +3.66% |
| 1 | 1 | 0 | 1 | 0 | +2.48% | +3.34% | +4.00% |
| 1 | 1 | 0 | 1 | 1 | +2.83% | +3.69% | +4.35% |
| 1 | 1 | 1 | 0 | 0 | +3.18% | +4.04% | +4.70% |
| 1 | 1 | 1 | 0 | 1 | +3.53% | +4.39% | +5.05% |
| 1 | 1 | 1 | 1 | 0 | +3.88% | +4.74% | +5.40% |
| 1 | 1 | 1 | 1 | 1 | +4.24% | +5.10% | +5.76% |

**Caution The internal high-speed oscillation frequency will increase in speed if the HIOTRM register value is incremented above a specific value, and will decrease in speed if decremented below that specific value. A reversal, such that the frequency decreases in speed by incrementing the value, or increases in speed by decrementing the value, will not occur.**

**Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)**

**(b) TOC00 = 13H, PRM00 = 10H, CRC00, = 04H, TMC00 = 0AH, CR000 = 0003H**




This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

### 6.4.7 One-shot pulse output operation

A one-shot pulse can be output by setting bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register 00 (TMC00) to 01 (free-running timer mode) or to 10 (clear & start mode entered by the TI000 pin valid edge) and setting bit 5 (OSPE00) of 16-bit timer output control register 00 (TOC00) to 1.

When bit 6 (OSPT00) of TOC00 is set to 1 or when the valid edge is input to the TI000 pin during timer operation, clearing & starting of TM00 is triggered, and a pulse of the difference between the values of CR000 and CR010 is output only once from the TO00 pin.

**Cautions 1. Do not input the trigger again (setting OSPT00 to 1 or detecting the valid edge of the TI000 pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.**

**2. To use only the setting of OSPT00 to 1 as the trigger of one-shot pulse output, do not change the level of the TI000 pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.**

**Remarks 1.** For the setting of the I/O pins, see **6.3 (6) Port mode register 3 (PM3)**.

**2.** For how to enable the INTTM000 signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

**Figure 6-44. Block Diagram of One-Shot Pulse Output Operation**

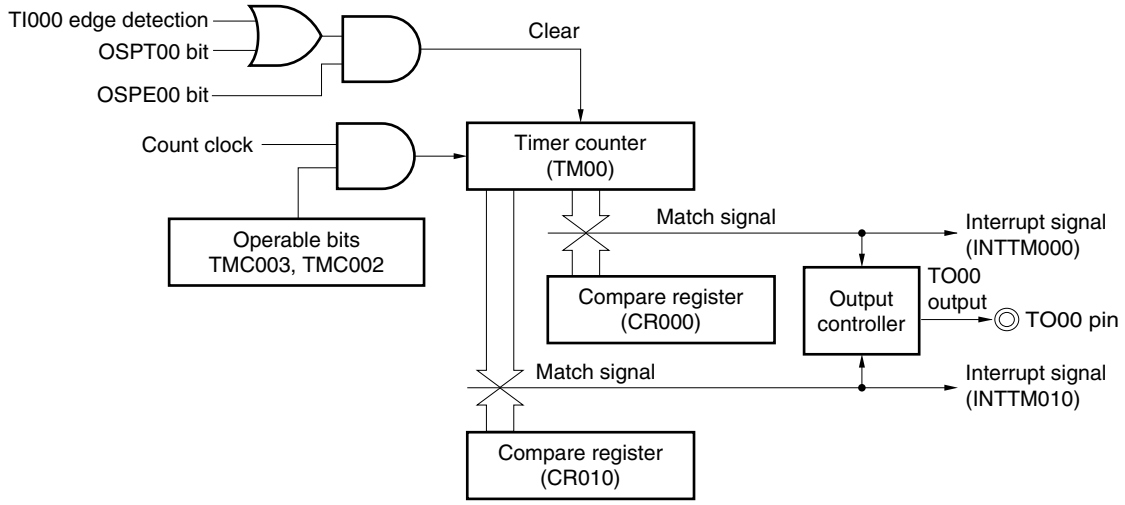
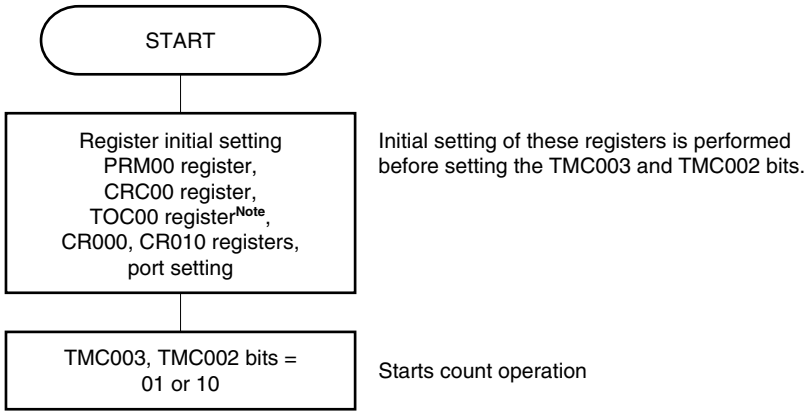
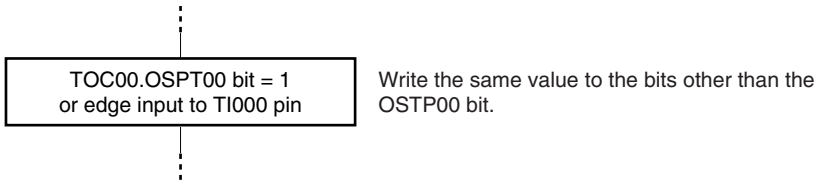


**Figure 6-46. Example of Software Processing for One-Shot Pulse Output Operation (2/2)**

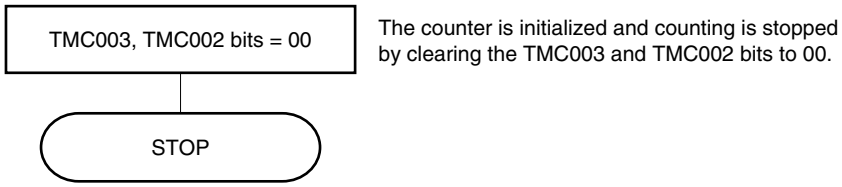
<1> Count operation start flow




<2> One-shot trigger input flow

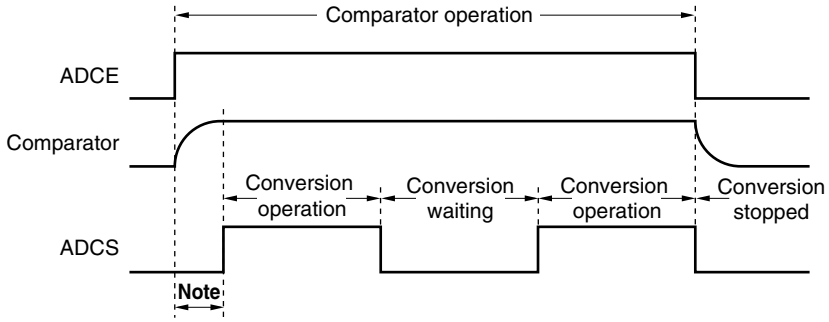



<3> Count operation stop flow




**Note** Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

**Figure 12-4. Timing Chart When Comparator Is Used**



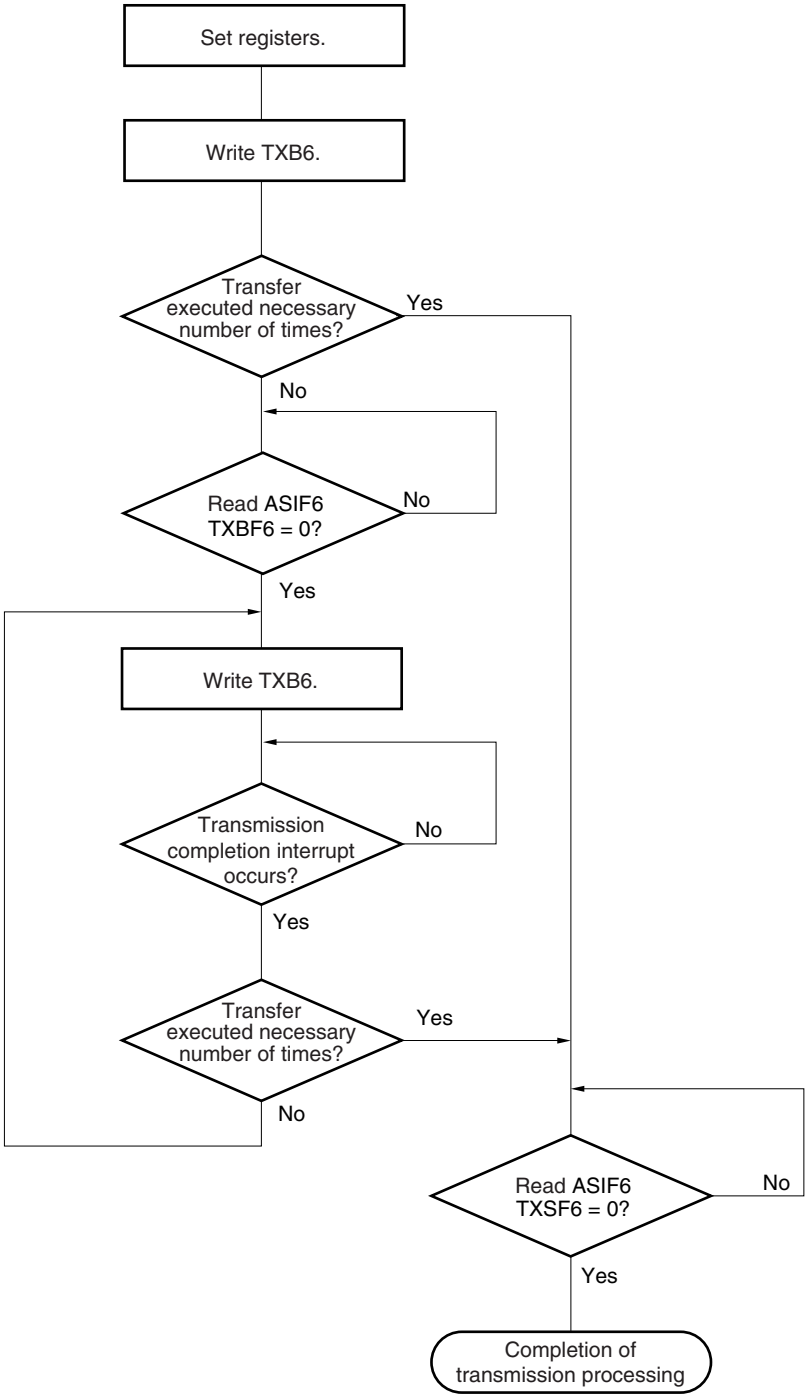

**Note** To stabilize the internal circuit, the time from the rising of the ADCE bit to the falling of the ADCS bit must be 1 μs or longer.

**Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR3, LV1, and LV0 to values other than the identical data.**

**2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 34 CAUTIONS FOR WAIT.**

Figure 15-18 shows an example of the continuous transmission processing flow.

**Figure 15-18. Example of Continuous Transmission Processing Flow**




**Remark** TXB6: Transmit buffer register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6 (transmit buffer data flag)
TXSF6: Bit 0 of ASIF6 (transmit shift register data flag)

**(i) SBF reception**

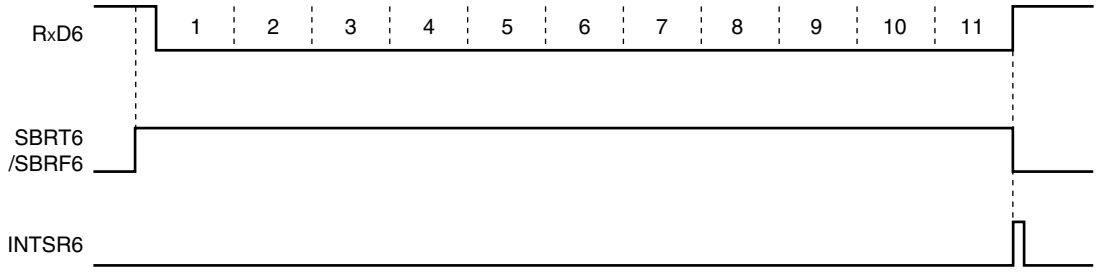
When the device is used in LIN communication operation, the SBF (Synchronous Break Field) reception control function is used for reception. For the reception operation of LIN, see **Figure 15-2 LIN Reception Operation**.

Reception is enabled when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is set to 1 and then bit 5 (RXE6) of ASIM6 is set to 1. SBF reception is enabled when bit 6 (SBRT6) of asynchronous serial interface control register 6 (ASICL6) is set to 1. In the SBF reception enabled status, the RxD6 pin is sampled and the start bit is detected in the same manner as the normal reception enable status.

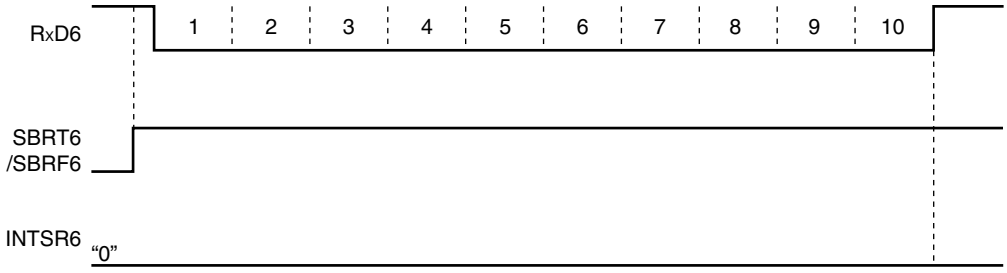
When the start bit has been detected, reception is started, and serial data is sequentially stored in the receive shift register 6 (RXS6) at the set baud rate. When the stop bit is received and if the width of SBF is 11 bits or more, a reception completion interrupt request (INTSR6) is generated as normal processing. At this time, the SBRF6 and SBRT6 bits are automatically cleared, and SBF reception ends. Detection of errors, such as OVE6, PE6, and FE6 (bits 0 to 2 of asynchronous serial interface reception error status register 6 (ASIS6)) is suppressed, and error detection processing of UART communication is not performed. In addition, data transfer between receive shift register 6 (RXS6) and receive buffer register 6 (RXB6) is not performed, and the reset value of FFH is retained. If the width of SBF is 10 bits or less, an interrupt does not occur as error processing after the stop bit has been received, and the SBF reception mode is restored. In this case, the SBRF6 and SBRT6 bits are not cleared.

**Figure 15-25. SBF Reception**

**1. Normal SBF reception (stop bit is detected with a width of more than 10.5 bits)**




**2. SBF reception error (stop bit is detected with a width of 10.5 bits or less)**




**Remark** RxD6: RxD6 pin (input)
SBRT6: Bit 6 of asynchronous serial interface control register 6 (ASICL6)
SBRF6: Bit 7 of ASICL6
INTSR6: Reception completion interrupt request

# CHAPTER 16 SERIAL INTERFACE CSI10

## 16.1 Functions of Serial Interface CSI10

Serial interface CSI10 has the following two modes.

**(1) Operation stop mode**

This mode is used when serial communication is not performed and can enable a reduction in the power consumption.

For details, see **16.4.1 Operation stop mode**.

**(2) 3-wire serial I/O mode (MSB/LSB-first selectable)**

This mode is used to communicate 8-bit data using three lines: a serial clock line ($\overline{\text{SCK10}}$) and two serial data lines (SI10 and SO10).

The processing time of data communication can be shortened in the 3-wire serial I/O mode because transmission and reception can be simultaneously executed.

In addition, whether 8-bit data is communicated with the MSB or LSB first can be specified, so this interface can be connected to any device.

The 3-wire serial I/O mode is used for connecting peripheral ICs and display controllers with a clocked serial interface.

For details, see **16.4.2 3-wire serial I/O mode**.

## 16.2 Configuration of Serial Interface CSI10

Serial interface CSI10 includes the following hardware.

**Table 16-1. Configuration of Serial Interface CSI10**

| Item | Configuration |
|---|---|
| Controller | Transmit controller<br>Clock start/stop controller & clock phase controller |
| Registers | Transmit buffer register 10 (SOTB10)<br>Serial I/O shift register 10 (SIO10) |
| Control registers | Serial operation mode register 10 (CSIM10)<br>Serial clock selection register 10 (CSIC10)<br>Port function register 1 (PF1)<br>Port mode register 1 (PM1)<br>Port register 1 (P1) |

**(1) Serial operation mode specification register 0 (CSIMA0)**

This is an 8-bit register used to control the serial communication operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 17-2. Format of Serial Operation Mode Specification Register 0 (CSIMA0)**

Address: FF90H After reset: 00H R/W

| Symbol | <7> | 6 | 5 | 4 | <3> | <2> | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CSIMA0 | CSIAE0 | ATE0 | ATM0 | MASTER0 | TXEA0 | RXEA0 | DIR0 | 0 |

| CSIAE0 | Control of CSIA0 operation enable/disable |
|---|---|
| 0 | CSIA0 operation disabled (SOA0: Low level, $\overline{\text{SCKA0}}$: High level) and asynchronously resets the internal circuit[Note]. |
| 1 | CSIA0 operation enabled |

| ATE0 | Control of automatic communication operation enable/disable |
|---|---|
| 0 | 1-byte communication mode |
| 1 | Automatic communication mode |

| ATM0 | Automatic communication mode specification |
|---|---|
| 0 | Single transfer mode (stops at the address specified by the ADTP0 register) |
| 1 | Repeat transfer mode (after transfer is complete, clear the ADTC0 register to 00H to resume transfer) |

| MASTER0 | CSIA0 master/slave mode specification |
|---|---|
| 0 | Slave mode (synchronous with $\overline{\text{SCKA0}}$ input clock) |
| 1 | Master mode (synchronous with internal clock) |

| TXEA0 | Control of transmit operation enable/disable |
|---|---|
| 0 | Transmit operation disabled (SOA0: Low level) |
| 1 | Transmit operation enabled |

| RXEA0 | Control of receive operation enable/disable |
|---|---|
| 0 | Receive operation disabled |
| 1 | Receive operation enabled |

| DIR0 | First bit specification |
|---|---|
| 0 | MSB |
| 1 | LSB |

**Note** Automatic data transfer address count register 0 (ADTC0), serial trigger register 0 (CSIT0), serial I/O shift register 0 (SIOA0), and bit 0 (TSF0) of serial status register 0 (CSIS0) are reset.

**Cautions 1. When CSIAE0 = 0, the buffer RAM cannot be accessed.**

**2. When CSIAE0 is changed from 1 to 0, the registers and bits mentioned in Note above are asynchronously initialized. To set CSIAE0 = 1 again, be sure to re-set the initialized registers.**

**3. When CSIAE0 is re-set to 1 after CSIAE0 is changed from 1 to 0, it is not guaranteed that the value of the buffer RAM will be retained.**

The relationship between the register settings and pins is shown below.

**Table 17-3. Relationship Between Register Settings and Pins**

| CSIAE0 | ATE0 | MASTER0 | PM15 | P15 | PM16 | P16 | PM14 | P14 | Serial I/O Shift Register 0 Operation | Serial Clock Counter Operation Control | Pin Function | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | SIA0/P15 | SOA0/P16 | $\overline{\text{SCKA0}}$/P14 /INTP4 |
| 0 | × | × | ×Note 1 | ×Note 1 | ×Note 1 | ×Note 1 | ×Note 1 | ×Note 1 | Operation stopped | Clear | P15 | P16 | P14/INTP4 |
| 1 | 0 | 0 | 1Note 2 | ×Note 2 | 0Note 3 | 0Note 3 | 1 | × | Operation enabled | Count operation | SIA0Note 2 | SOA0Note 3 | $\overline{\text{SCKA0}}$ (input) |
| | | 1 | | | | | 0 | 1 | | | | | $\overline{\text{SCKA0}}$ (output) |

**Notes 1.** Can be set as port function.

**2.** Can be used as P15 when only transmission is performed. Clear bit 2 (RXEA0) of CSIMA0 to 0.

**3.** Can be used as P16 when only reception is performed. Clear bit 3 (TXEA0) of CSIMA0 to 0.

**Remark** ×: don't care
CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ATE0: Bit 6 of CSIMA0
MASTER0: Bit 4 of CSIMA0
PM1×: Port mode register
P1×: Port output latch

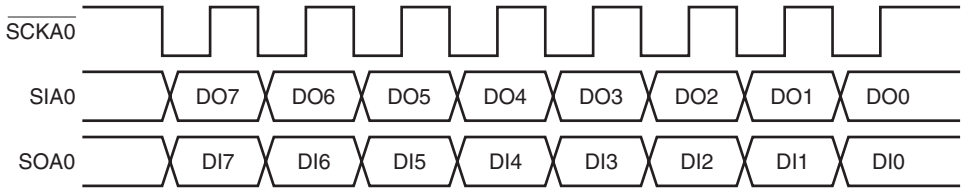
**(b) Data format**

In the data format, data is changed in synchronization with the $\overline{\text{SCKA0}}$ falling edge as shown below.

The data length is fixed to 8 bits and the data communication direction can be switched by the specification of bit 1 (DIR0) of serial operation mode specification register 0 (CSIMA0).

**Figure 17-12. Format of Transmit/Receive Data**

**(a) MSB-first (DIR0 bit = 0)**




**(b) LSB-first (DIR0 bit = 1)**

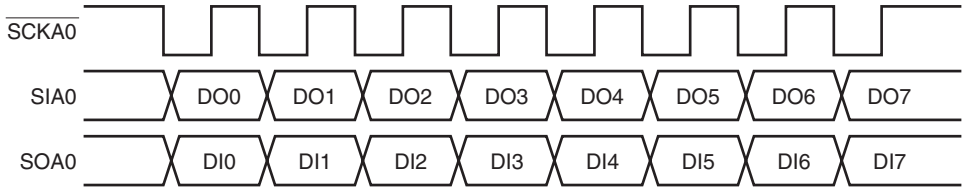
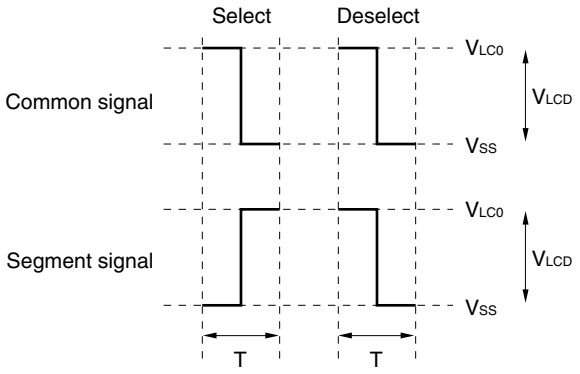


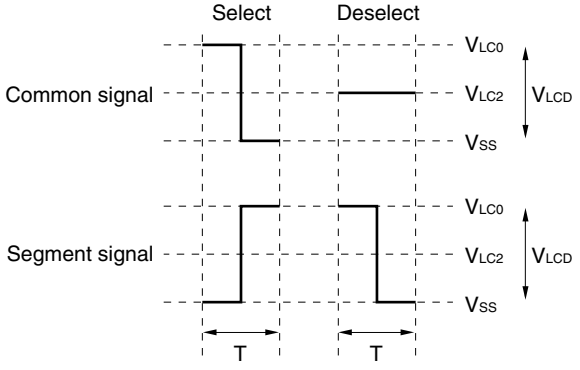
**Figure 18-14 Voltages and Phases of Common and Segment Signals**

**(a) Static display mode**



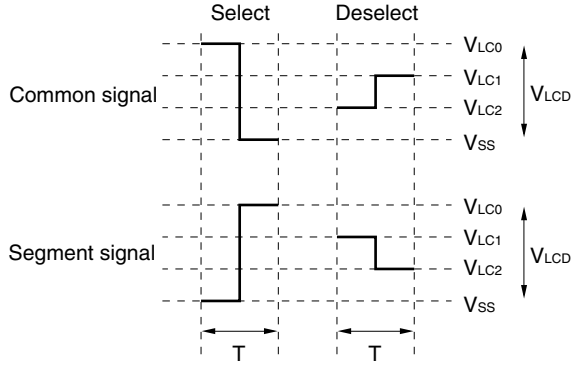

T: One LCD clock period

**(b) 1/2 bias method**




T: One LCD clock period

**(c) 1/3 bias method**

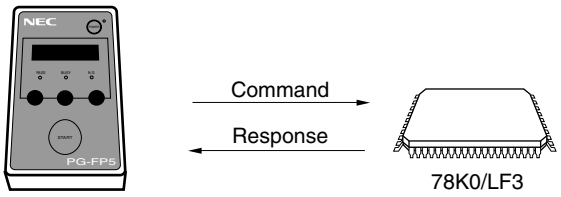



T: One LCD clock period

### 28.7.4 Communication commands

The 78K0/LF3 communicates with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0/LF3 are called commands, and the signals sent from the 78K0/LF3 to the dedicated flash memory programmer are called response.

**Figure 28-14. Communication Commands**




The flash memory control commands of the 78K0/LF3 are listed in the table below. All these commands are issued from the programmer and the 78K0/LF3 perform processing corresponding to the respective commands.

**Table 28-8. Flash Memory Control Commands**

| Classification | Command Name | Function |
|---|---|---|
| Verify | Verify | Compares the contents of a specified area of the flash memory with data transmitted from the programmer. |
| Erase | Chip Erase | Erases the entire flash memory. |
| | Block Erase | Erases a specified area in the flash memory. |
| Blank check | Block Blank Check | Checks if a specified block in the flash memory has been correctly erased. |
| Write | Programming | Writes data to a specified area in the flash memory. |
| Getting information | Status | Gets the current operating status (status data). |
| | Silicon Signature | Gets 78K0/Lx3 information (such as the part number and flash memory configuration). |
| | Version Get | Gets the 78K0/Lx3 version and firmware version. |
| | Checksum | Gets the checksum data for a specified area. |
| Security | Security Set | Sets security information. |
| Others | Reset | Used to detect synchronization status of communication. |
| | Oscillating Frequency Set | Specifies an oscillation frequency. |

The 78K0/LF3 return a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0/LF3 are listed below.

**Table 28-9. Response Names**

| Response Name | Function |
|---|---|
| ACK | Acknowledges command/data. |
| NAK | Acknowledges illegal command/data. |

| Instruction Group | Mnemonic | Operands | Bytes | Clocks | | Operation | Flag |
|---|---|---|---|---|---|---|---|
| | | | | Note 1 | Note 2 | | Z AC CY |
| Bit manipulate | **AND1** | CY, saddr.bit | 3 | 6 | 7 | CY ← CY ∧ (saddr.bit) | × |
| | | CY, sfr.bit | 3 | – | 7 | CY ← CY ∧ sfr.bit | × |
| | | CY, A.bit | 2 | 4 | – | CY ← CY ∧ A.bit | × |
| | | CY, PSW.bit | 3 | – | 7 | CY ← CY ∧ PSW.bit | × |
| | | CY, [HL].bit | 2 | 6 | 7 | CY ← CY ∧ (HL).bit | × |
| | **OR1** | CY, saddr.bit | 3 | 6 | 7 | CY ← CY ∨ (saddr.bit) | × |
| | | CY, sfr.bit | 3 | – | 7 | CY ← CY ∨ sfr.bit | × |
| | | CY, A.bit | 2 | 4 | – | CY ← CY ∨ A.bit | × |
| | | CY, PSW.bit | 3 | – | 7 | CY ← CY ∨ PSW.bit | × |
| | | CY, [HL].bit | 2 | 6 | 7 | CY ← CY ∨ (HL).bit | × |
| | **XOR1** | CY, saddr.bit | 3 | 6 | 7 | CY ← CY ⊻ (saddr.bit) | × |
| | | CY, sfr.bit | 3 | – | 7 | CY ← CY ⊻ sfr.bit | × |
| | | CY, A.bit | 2 | 4 | – | CY ← CY ⊻ A.bit | × |
| | | CY, PSW. bit | 3 | – | 7 | CY ← CY ⊻ PSW.bit | × |
| | | CY, [HL].bit | 2 | 6 | 7 | CY ← CY ⊻ (HL).bit | × |
| | **SET1** | saddr.bit | 2 | 4 | 6 | (saddr.bit) ← 1 | |
| | | sfr.bit | 3 | – | 8 | sfr.bit ← 1 | |
| | | A.bit | 2 | 4 | – | A.bit ← 1 | |
| | | PSW.bit | 2 | – | 6 | PSW.bit ← 1 | × × × |
| | | [HL].bit | 2 | 6 | 8 | (HL).bit ← 1 | |
| | **CLR1** | saddr.bit | 2 | 4 | 6 | (saddr.bit) ← 0 | |
| | | sfr.bit | 3 | – | 8 | sfr.bit ← 0 | |
| | | A.bit | 2 | 4 | – | A.bit ← 0 | |
| | | PSW.bit | 2 | – | 6 | PSW.bit ← 0 | × × × |
| | | [HL].bit | 2 | 6 | 8 | (HL).bit ← 0 | |
| | **SET1** | CY | 1 | 2 | – | CY ← 1 | 1 |
| | **CLR1** | CY | 1 | 2 | – | CY ← 0 | 0 |
| | **NOT1** | CY | 1 | 2 | – | CY ← $\overline{CY}$ | × |

**Notes 1.** When the internal high-speed RAM area is accessed or for an instruction with no data access

**2.** When an area except the internal high-speed RAM area is accessed

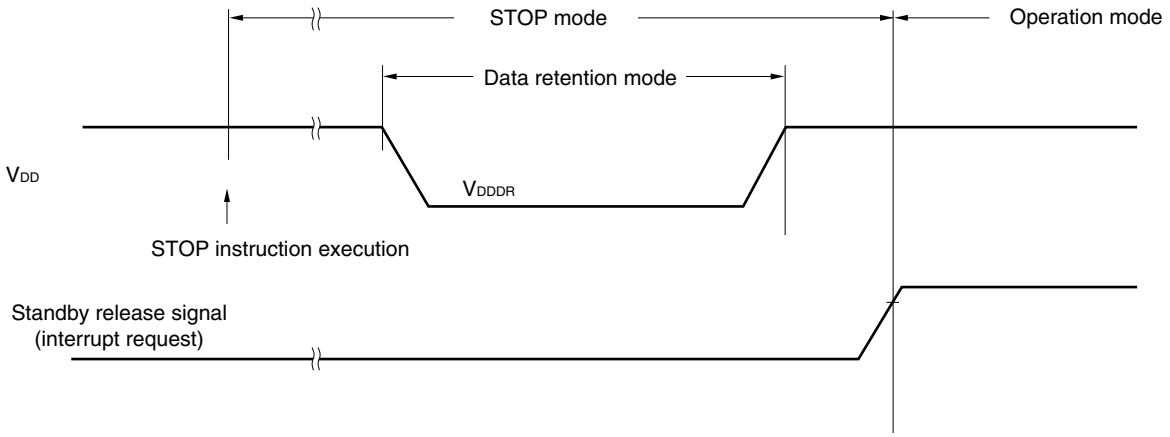
**Remarks 1.** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$) selected by the processor clock control register (PCC).

**2.** This clock cycle applies to the internal ROM program.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A$ = –40 to +85°C)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44[Note] | | 5.5 | V |

**Note** The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.




**Flash Memory Programming Characteristics**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

**• Basic characteristics**

| Parameter | | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ supply current | | $I_{DD}$ | | | | | 4.5 | 11.0 | mA |
| Erase time[Note 1, 2] | All block | $T_{eraca}$ | | | | | 20 | 200 | ms |
| | Block unit | $T_{erasa}$ | | | | | 20 | 200 | ms |
| Write time (in 8-bit units)[Note 1] | | $T_{wrwa}$ | | | | | 10 | 100 | μs |
| <R> Number of rewrites per chip | | $C_{erwr}$ | 1 erase + 1 write after erase = 1 rewrite[Note 3] | When a flash memory programmer is used, and the libraries provided by NEC Electronics are used | Retention: 15 years | 1000 | | | Times |
| | | | | When the EEPROM emulation libraries provided by NEC Electronics are used, and the rewritable ROM size is 4 KB | Retention: 3 years[Note 4] | 10000 | | | Times |

<R> **Notes 1.** Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP5, is used and the rewrite time during self programming, see **Tables 28-12** and **28-13**.

**2.** The prewrite time before erasure and the erase verify time (writeback time) are not included.

**3.** When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

<R> **4.** Data retention is guaranteed for three years after data has been written. If rewriting has been performed, data retention is guaranteed for another three years thereafter.

**Remark** $f_{XP}$: Main system clock oscillation frequency

# APPENDIX B REVISION HISTORY

## B.1 Major Revisions in This Edition

(1/3)

| Page | Description | Classification |
|---|---|---|
| Throughout | • Addition of PG-FP5 and FL-PR5<br>• Addition of explanation for segment key scan function | (b, c) |
| **CHAPTER 1 OUTLINE** | | |
| p. 17 | Addition of **Note 2** to Table of ROM, RAM capacities **in 1.1 Features** | (d) |
| pp. 20 to 22 | Addition of **Remark 2** to **1.4 Pin Configuration (Top View)** | (c) |
| pp. 25 to 27 | Addition of **Note** to table of function list in **1.5 78K0/Lx3 Microcontroller Series Lineup** | (c) |
| p. 30 | Addition of **Note 4** to **1.7 Outline of Functions (μPD78F047x)** | (c) |
| p. 33 | Addition of **Note 4** to **1.8 Outline of Functions (μPD78F048x)** | (c) |
| p. 36 | Addition of **Note 5** to **1.9 Outline of Functions (μPD78F049x)** | (c) |
| **CHAPTER 3 CPU ARCHITECTURE** | | |
| pp. 59, 61, 63, 65, 67 | Addition of **Note 3** to **Memory Map** of **Figure 3-2**, **Figure 3-4**, **Figure 3-6**, **Figure 3-8**, **and Figure 3-10** | (b) |
| pp. 73, 75, 77, 79, 81 | Addition of **Note** to **Correspondence Between Data Memory and Addressing** of **Figure 3-12**, **Figure 3-14**, **Figure 3-16**, **Figure 3-18**, **and Figure 3-20** | (b) |
| p. 95 | Change of Illustration in **3.3.3 Table indirect addressing** | (c) |
| **CHAPTER 4 PORT FUNCTIONS** | | |
| p. 116 | Change of **Figure 4-8. Block Diagram of P20 to P27** | (a) |
| p. 138 | Change of **Figure 4-28. Format of Port Register** and addition of **Notes 1, 2**, and **3** | (b, c) |
| p. 139 | Addition of **Note** to **Figure 4-29. Format of Pull-up Resistor Option Register** | (c) |
| **CHAPTER 5 CLOCK GENERATOR** | | |
| p. 160 | Change of **Figure 5-9. Format of Internal High-speed Oscillation Trimming Register (HIOTRM)** | (b) |
| p. 166 | Change of **Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On** | (b) |
| p. 167 | Change of **Caution 1** in **Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On** | (b) |
| **CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00** | | |
| p. 197 | Addition of **Note 2** to **Figure 6-10. Format of Input Switch Control Register (ISC)** | (c) |
| p. 232 | Modification of **Figure 6-42. (f) 16-bit capture/compare register 000 (CR000)** | (a) |
| p. 259 | Addition of **6.6 (12) Reading of 16-bit timer counter 00 (TM00)** | (c) |
| **CHAPTER 7 8-BIT TIMER/EVENT COUNTERS 50, 51, AND 52** | | |
| p. 270 | Addition of **Note 2** to **Figure 7-12. Format of Input Switch Control Register (ISC)** | (c) |
| p. 280 | Change of **7.5 (2) Cautions for 16-bit timer/event counter 00 count up during external 24-bit event counter operation** | (c) |
| p. 281 | Addition of **7.5 (3) Reading of 8-bit timer counter 5n (TM5n)** | (c) |
| **CHAPTER 8 8-BIT TIMERS H0, H1, AND H2** | | |
| p. 284 | Change of **Figure 8-2. Block Diagram of 8-Bit Timer H1** | (a) |
| p. 288 | Change of **Figure 8-6. Format of 8-Bit Timer H Mode Register 0 (TMHMD0)** | (c) |
| p. 310 | Addition of **8.4.4 Control of number of carrier clocks by timer 51 counter** | (b, c) |

**Remark** "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents