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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	77
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5605bk0cll6

2.2 Pin muxing

Table 2 defines the pin list and muxing for this device.

Each entry of Table 2 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 2. Functional port pins

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
Port A										
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][4]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKUP	I/O I/O O I/O I	M	Tristate	12	16	24
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[5] — WKUP[2][4]	SIUL eMIOS_0 WKUP — WKUP	I/O I/O I — I	S	Tristate	7	11	19
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKUP[3][4]	SIUL eMIOS_0 — ADC_0 WKUP	I/O I/O — O I	S	Tristate	5	9	17
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKUP[9][4]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKUP	I/O I/O — I/O I I	S	Tristate	29	43	51
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	118	146
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKUP[10][4]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKUP	I/O I/O I/O I/O I	M	Tristate	27	40	48
Port B										
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX E0UC[30] LIN0TX	SIUL FlexCAN_0 eMIOS_0 LINFlex_0	I/O O I/O O	M	Tristate	23	31	39
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — — —	GPIO[17] — E0UC[31] — WKUP[4][4] CAN0RX LIN0RX	SIUL — eMIOS_0 — WKUP FlexCAN_0 LINFlex_0	I/O — I/O — I I I	S	Tristate	24	32	40
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA E0UC[30]	SIUL LINFlex_0 I^2C_0 eMIOS_0	I/O O I/O I/O	M	Tristate	100	144	176
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] E0UC[31] SCL — WKUP[11][4] LIN0RX	SIUL eMIOS_0 I^2C_0 — WKUP LINFlex_0	I/O I/O I/O — I I	S	Tristate	1	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[0] ADC1_P[0] GPIO[20]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	50	72	88
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[1] ADC1_P[1] GPIO[21]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	53	75	91

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	76	92
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	55	77	93
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL[7] WKUP[25] ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKUP ADC_0 ADC_1	I — — — — I I I	I	—	39	53	61
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL[7] WKUP[26] ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKUP ADC_0 ADC_1	I — — — — I I I	I	—	38	52	60
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] — — — WKUP[8][4] ADC0_S[2] ADC1_S[6]	SIUL — — — WKUP ADC_0 ADC_1	I/O — — — I I I	J	Tristate	40	54	62
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	J	Tristate	—	—	97
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	61	83	101

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	4	4
Port D										
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPIO[48] — — — WKUP[27] ADC0_P[4] ADC1_P[4]	SIUL — — — WKUP ADC_0 ADC_1	I — — — I I I	I	Tristate	41	63	77
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPIO[49] — — — WKUP[28] ADC0_P[5] ADC1_P[5]	SIUL — — — WKUP ADC_0 ADC_1	I — — — I I I	I	Tristate	42	64	78
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 — —	GPIO[50] — — — ADC0_P[6] ADC1_P[6]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	43	65	79
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPIO[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	44	66	80
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPIO[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	45	67	81

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] E1UC[4] — — EIRQ[13] CAN1RX CAN4RX	SIUL eMIOS_1 — — SIUL FlexCAN_1 FlexCAN_4	I/O I/O — — I I I	S	Tristate	—	101	125
Port G										
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	122
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — EIRQ[14] CAN5RX	SIUL — eMIOS_1 — SIUL FlexCAN_5	I/O — I/O — I I	S	Tristate	—	97	121
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M	Tristate	—	8	16
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKUP[17][4]	SIUL eMIOS_1 DSPI_3 — WKUP	I/O I/O O — I	S	Tristate	—	7	15
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M	Tristate	—	6	14
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKUP[18][4] SIN_3	SIUL eMIOS_1 — — WKUP DSPI_3	I/O I/O — — I I	S	Tristate	—	5	13
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX —	SIUL eMIOS_1 LINFlex_6 —	I/O I/O O —	M	Tristate	—	30	38

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	J	Tristate	—	—	76
PI[15]	PCR[143]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 — — ADC0_S[23]	SIUL DSPI_4 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	75
Port J										
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 —	GPIO[144] CS1_4 — — ADC0_S[24]	SIUL DSPI_4 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	74
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — — — ADC0_S[25] SIN_5	SIUL — — —— ADC_0 DSPI_5	I/O — — — I I	J	Tristate	—	—	73
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 — — ADC0_S[26]	SIUL DSPI_5 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	72
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 — — ADC0_S[27]	SIUL DSPI_5 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	71
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O — —	M	Tristate	—	—	5

1 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 See Table 3.

3 The RESET configuration applies during and after reset.

Table 4. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the *MPC5606BK Microcontroller Reference Manual*.

3.2.1 NVUSRO[PAD3V5V] field description

Table 5 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 5. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 6 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 6. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs

Table 14. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PC[0]	6%	9%	7%	8%	7%	10%	8%	8%
			PH[9]	7%	—	8%	—	7%	—	9%	—
			PE[2]	7%	10%	8%	9%	8%	11%	9%	10%
			PE[3]	7%	10%	9%	9%	8%	12%	10%	10%
			PC[5]	7%	11%	9%	9%	8%	12%	10%	11%
			PC[4]	8%	11%	9%	10%	9%	13%	10%	11%
			PE[4]	8%	11%	9%	10%	9%	13%	11%	12%
			PE[5]	8%	11%	10%	10%	9%	14%	11%	12%
		—	PH[4]	8%	12%	10%	10%	10%	14%	12%	12%
		—	PH[5]	8%	—	10%	—	10%	—	12%	—
		—	PH[6]	8%	12%	10%	11%	10%	15%	12%	13%
		—	PH[7]	9%	12%	10%	11%	11%	15%	13%	13%
		—	PH[8]	9%	12%	10%	11%	11%	16%	13%	14%
		4	PE[6]	9%	12%	10%	11%	11%	16%	13%	14%
			PE[7]	9%	12%	10%	11%	11%	16%	14%	14%
	—	—	PI[3]	9%	—	10%	—	—	—	—	—
	—	—	PI[2]	9%	—	10%	—	—	—	—	—
	—	—	PI[1]	9%	—	10%	—	—	—	—	—
	—	—	PI[0]	9%	—	10%	—	—	—	—	—
	4	4	PC[12]	8%	12%	10%	11%	12%	18%	15%	16%
			PC[13]	8%	—	10%	—	13%	—	15%	—
			PC[8]	8%	—	10%	—	13%	—	15%	—
			PB[2]	8%	11%	9%	10%	13%	18%	15%	16%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 SRC is the Slew Rate Control bit in SIU_PCR*x*

3.7 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors VDD_BV to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

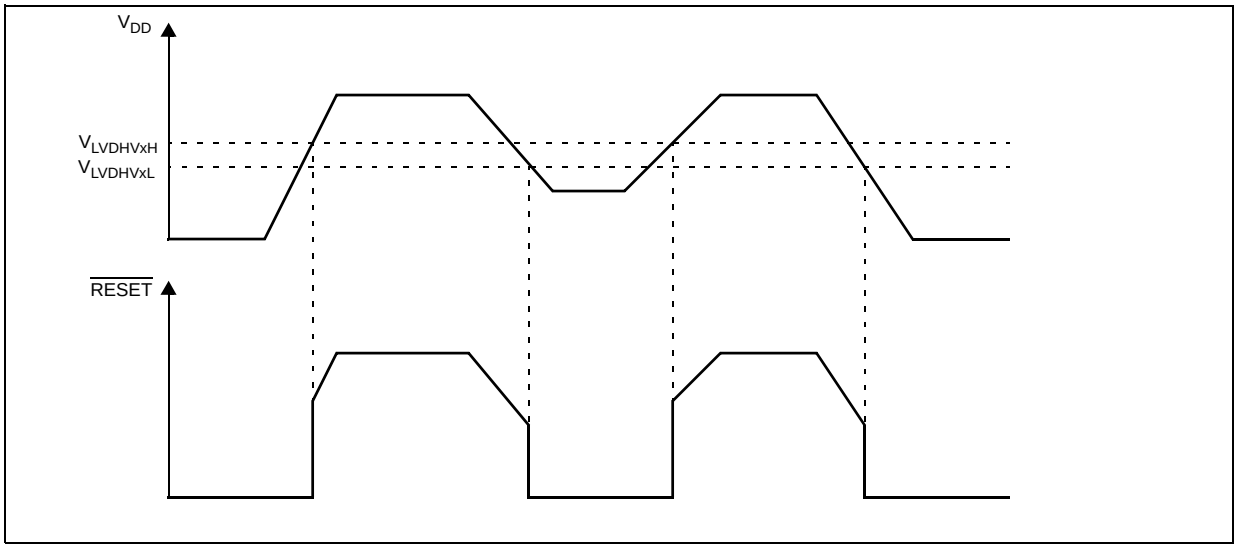

Figure 11. Low voltage monitor vs. reset

Table 23. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	D	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV3BH}$	CC	T	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3BL low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.14	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

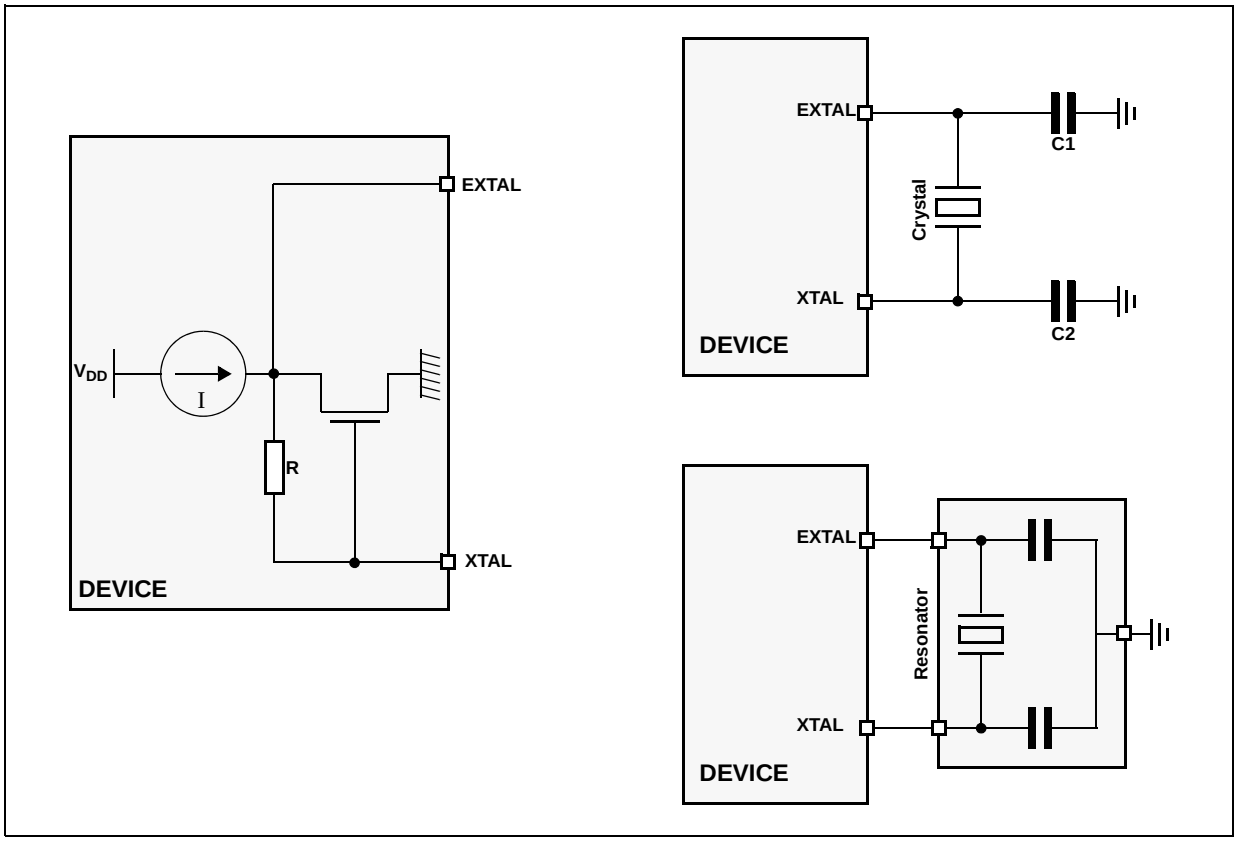

Figure 12. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 33. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Table 34. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

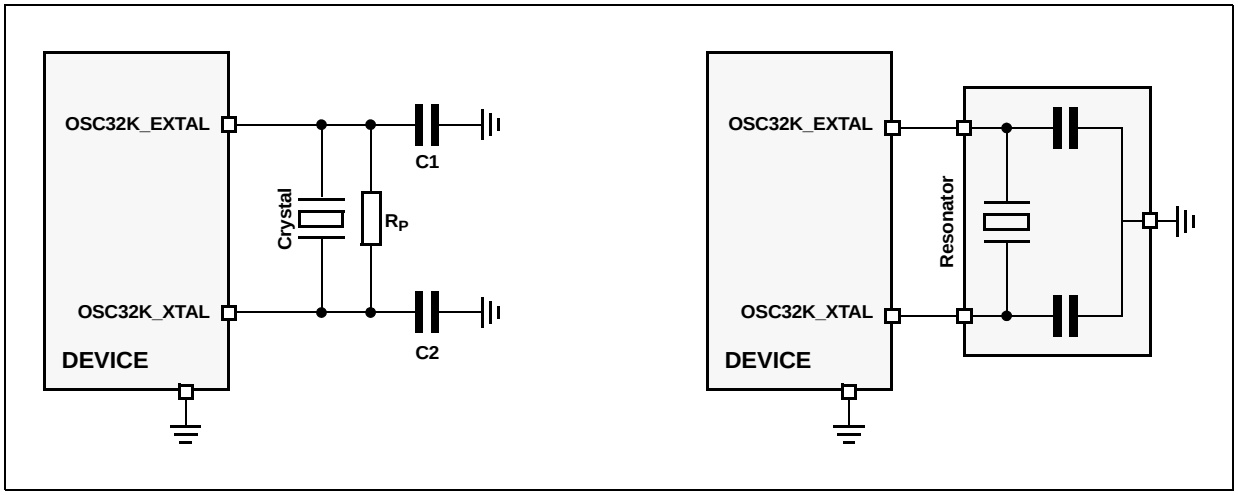

Figure 14. Crystal oscillator and resonator connection scheme

NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

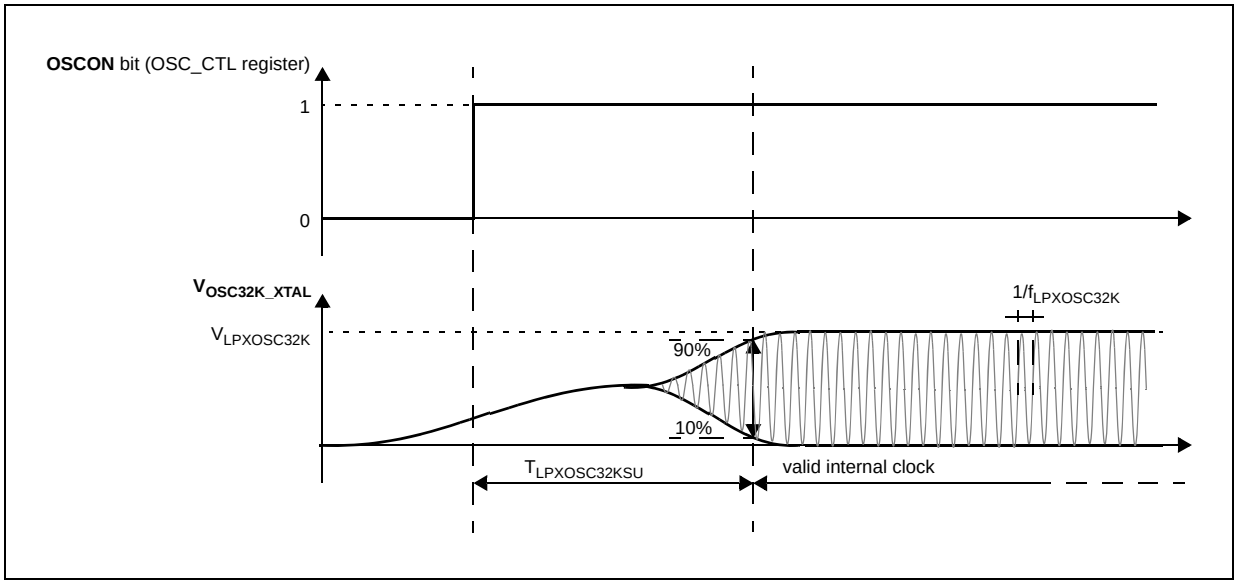

Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 36. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the FXOSC or FIRC sources.

Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

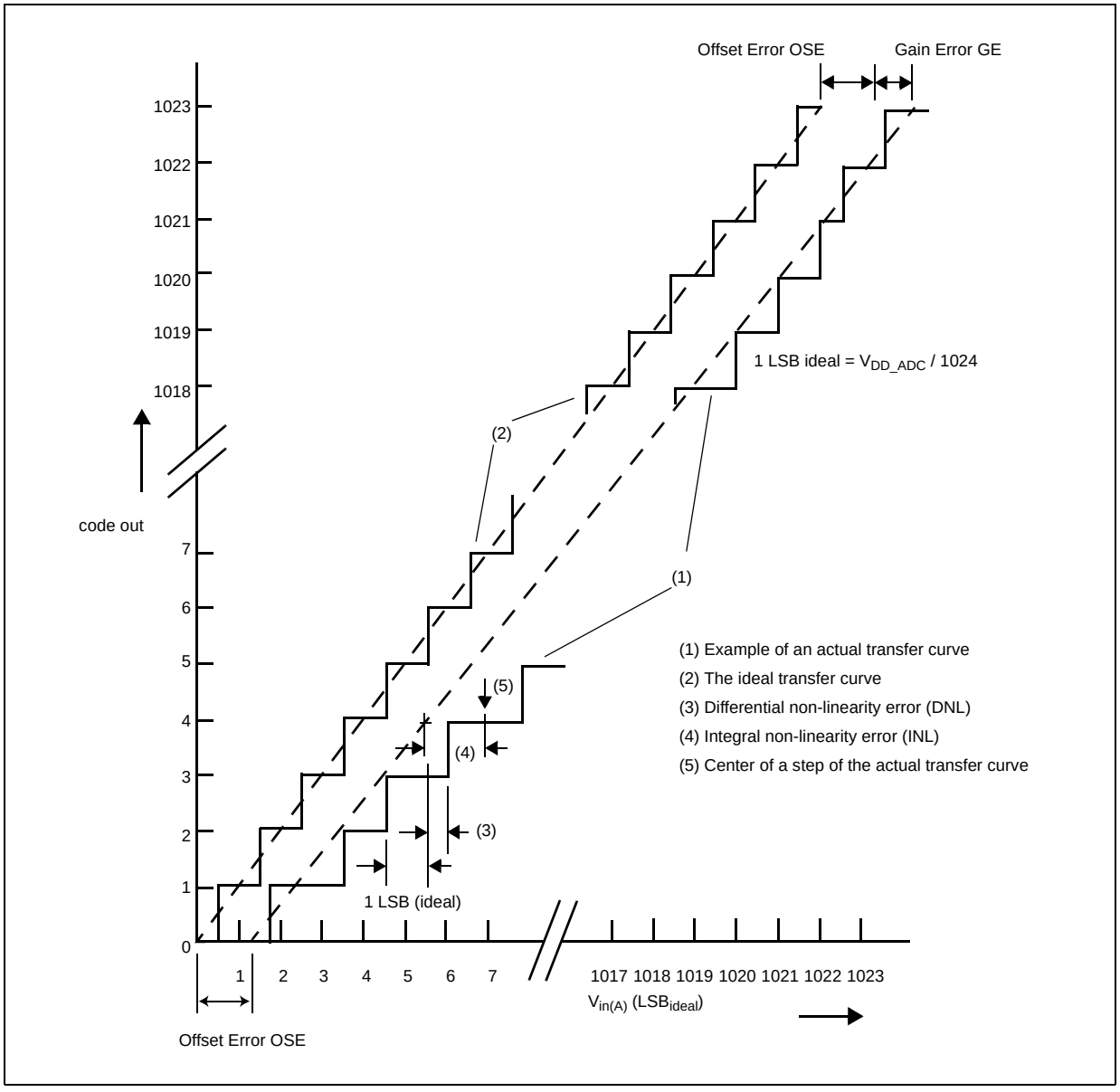

Figure 17. ADC_0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

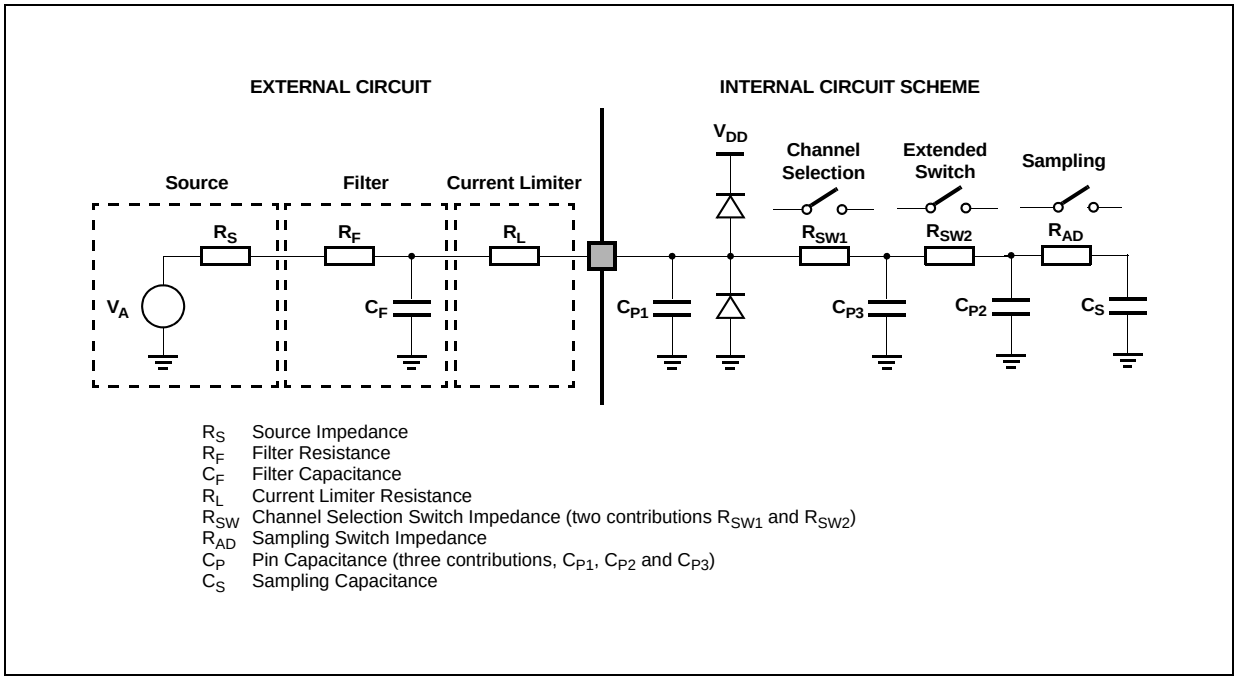

Figure 19. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

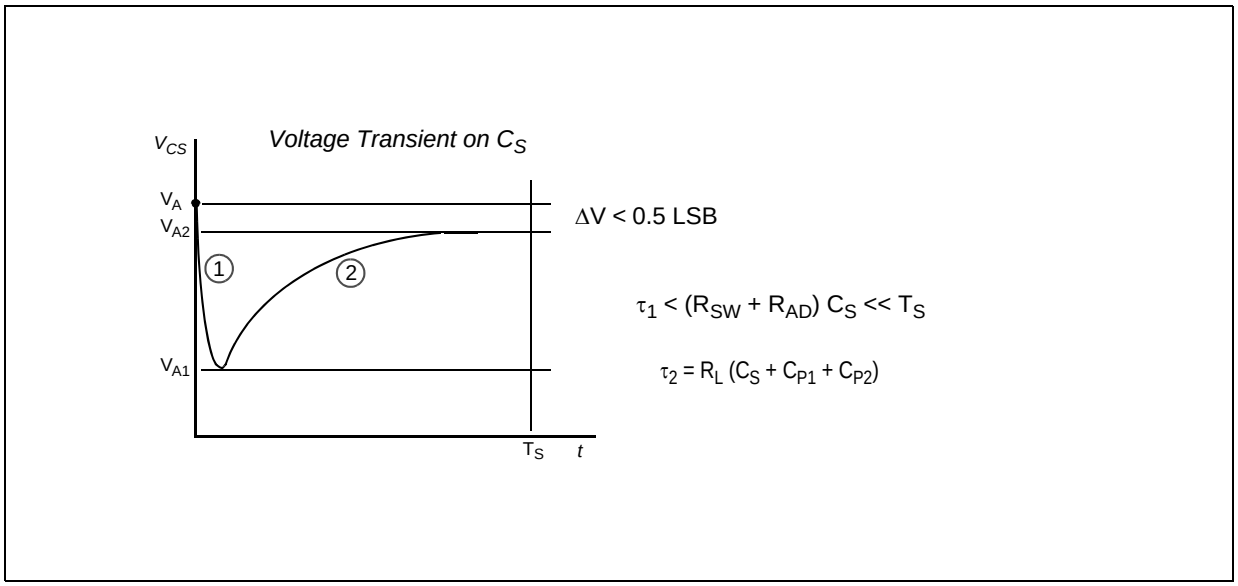

Figure 20. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

3.17.3 ADC electrical characteristics

Table 40. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		D		T_A = 85°C			3	100	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 41. ADC_0 conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
$I_{ADC0pwd}$	SR	—	ADC_0 consumption in power down mode	—	—	—	50	µA
$I_{ADC0run}$	SR	—	ADC_0 consumption in running mode	—	—	—	5	mA
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC0_SYS}	SR	—	ADC_0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[5]	f_{ADC} = 32 MHz, ADC0_conf_sample_input = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t_{ADC0_C}	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF

Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-Extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
OFS	CC	T	Absolute Offset error	—		—	2	—	LSB
GNE	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		–6	—	6	LSB
		T		With current injection		–8	—	8	
TUEX[7]	CC	T	Total Unadjusted Error for extended channel	Without current injection		–10	—	10	LSB
		T		With current injection		–12	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.

5 This parameter does not include the sample time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

6 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Table 44. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI5/DSPI6			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

1 Operating conditions: C_{out} = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

2 For DSPI4, if SOUT is mapped to a SLOW pad while SCK is mapped to a MEDIUM pad (or vice versa), the minimum cycle time for SCK should be calculated based on the rise and fall times of the SLOW pad. For MTFE=1, SOUT must not be mapped to a SLOW pad while SCK is mapped to a MEDIUM pad.

3 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTAR*x* registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

4 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTAR*x* registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

5 For DSPI*x*_CTAR*n*[PCSSCK] = 11.

6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

7 SCK and SOUT are configured as MEDIUM pad.

6 Revision history

Table 46. Revision history

Revision	Date	Description of changes
1	22 Apr 2011	Initial release.
2	15 May 2013	Changed device number to MPC5606BK. In Table 2 (Functional port pins), updated PA[11] AF2, PD[13] AF2, and PH[11] AF3 I/O direction to “I/O”. In Table 3 (Pad types), corrected “Fast” in the “S” row to “Slow.” In Table 5 (PAD3V5V field description), updated footnote 2. In Table 6 (OSCILLATOR_MARGIN field description), updated footnote 2. Inserted Section 3.2.3, NVUSRO[WATCHDOG_EN] field description. In Table 8 (Absolute maximum ratings), Table 9 (Recommended operating conditions (3.3 V)), and Table 10 (Recommended operating conditions (5.0 V)), corrected the parameter description for V_{DD_ADC} to “Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})” In Section 3.6.1, I/O pad types bullet item, removed Nexus reference. In Table 12 (I/O input DC electrical characteristics), added specifications for 85 °C. In Table 13 (I/O pull-up/pull-down DC electrical characteristics), Table 14 (SLOW configuration output buffer electrical characteristics), Table 15 (MEDIUM configuration output buffer electrical characteristics), and Table 16 (FAST configuration output buffer electrical characteristics), changed sentence in footnote 2 to “All pads but RESET are configured in input or in high impedance state.” In Table 15 (MEDIUM configuration output buffer electrical characteristics), for V_{OL}, changed I_{OH} to I_{OL}. Updated Table 20 (I/O weight). In Table 21 (Reset electrical characteristics) changed sentence in footnote 4 to “All pads but RESET are configured in input or in high impedance state.” in Table 22 (Voltage regulator electrical characteristics), corrected the maximum value for I_{DD_BV} in Table 22 (Voltage regulator electrical characteristics) to 300 mA. In Table 23 (Low voltage monitor electrical characteristics), changed V_{PORUP} classification tag from “P” (Production testing guaranteed) to “D” (Design simulation). Changed $V_{LVDHV3BH}$ classification tag from “P” (Production testing guaranteed) to “T” (Design characterization). In Table 23 (Low voltage monitor electrical characteristics), changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ minimums from 2.7 V to 2.6 V.