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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	77
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5605bk0mll6r

Figure 4 shows the MPC5606BK in the 100 LQFP package.

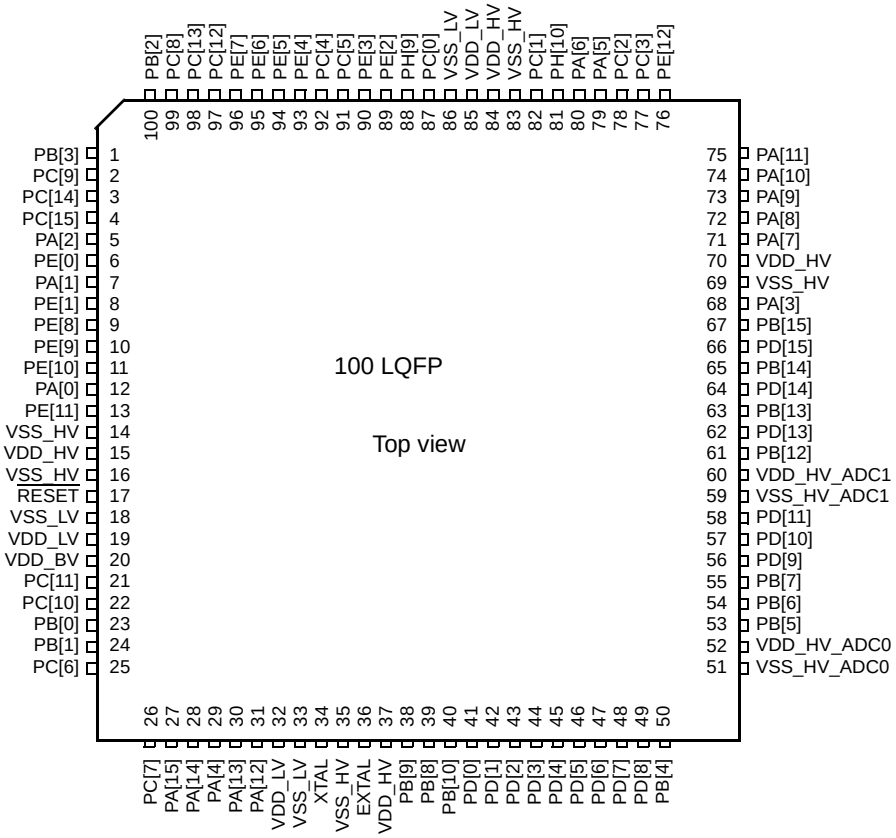


Figure 4. 100 LQFP pinout

2.2 Pin muxing

Table 2 defines the pin list and muxing for this device.

Each entry of Table 2 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 2. Functional port pins

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
Port A										
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][4]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKUP	I/O I/O O I/O I	M	Tristate	12	16	24
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[5] — WKUP[2][4]	SIUL eMIOS_0 WKUP — WKUP	I/O I/O I — I	S	Tristate	7	11	19
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKUP[3][4]	SIUL eMIOS_0 — ADC_0 WKUP	I/O I/O — O I	S	Tristate	5	9	17
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKUP[9][4]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKUP	I/O I/O — I/O I I	S	Tristate	29	43	51
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	118	146
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX DEBUG[3] EIRQ[7]	SIUL DSPI_1 FlexCAN_3 SSCM SIUL	I/O O O O I	M	Tristate	91	130	158
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] DEBUG[4]	SIUL LINFlex_1 eMIOS_1 SSCM	I/O O I/O O	S	Tristate	25	36	44
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] DEBUG[5] LIN1RX WKUP[12][4]	SIUL — eMIOS_1 SSCM LINFlex_1 WKUP	I/O — I/O O I I	S	Tristate	26	37	45
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] DEBUG[6]	SIUL LINFlex_2 eMIOS_0 SSCM	I/O O I/O O	S	Tristate	99	143	175
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] DEBUG[7] WKUP[13][4] LIN2RX	SIUL — eMIOS_0 SSCM WKUP LINFlex_2	I/O — I/O O I I	S	Tristate	2	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M	Tristate	22	28	36
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] WKUP[5][4] CAN1RX CAN4RX	SIUL — — ADC_0 WKUP FlexCAN_1 FlexCAN_4	I/O — — O I I I	S	Tristate	21	27	35
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	4	4
Port D										
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPIO[48] — — — WKUP[27] ADC0_P[4] ADC1_P[4]	SIUL — — — WKUP ADC_0 ADC_1	I — — — I I I	I	Tristate	41	63	77
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPIO[49] — — — WKUP[28] ADC0_P[5] ADC1_P[5]	SIUL — — — WKUP ADC_0 ADC_1	I — — — I I I	I	Tristate	42	64	78
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 — —	GPIO[50] — — — ADC0_P[6] ADC1_P[6]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	43	65	79
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 — —	GPIO[51] — — — ADC0_P[7] ADC1_P[7]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	44	66	80
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPIO[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	45	67	81

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	139	167
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	140	168
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	21
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKUP[7][4] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKUP FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	14	22
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlex_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	11	15	23
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKUP[14][4]	SIUL eMIOS_0 DSPI_1 — LINFlex_3 WKUP	I/O I/O O — I I	S	Tristate	13	17	25
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — —	GPIO[76] — E1UC[19][10] — EIRQ[11] SIN_2 ADC1_S[7]	SIUL — eMIOS_1 — SIUL DSPI_2 ADC_1	I/O — I/O — I I I	J	Tristate	76	109	133
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT_2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	103	127

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] E1UC[4] — — EIRQ[13] CAN1RX CAN4RX	SIUL eMIOS_1 — — SIUL FlexCAN_1 FlexCAN_4	I/O I/O — — I I I	S	Tristate	—	101	125
Port G										
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	122
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — EIRQ[14] CAN5RX	SIUL — eMIOS_1 — SIUL FlexCAN_5	I/O — I/O — I I	S	Tristate	—	97	121
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M	Tristate	—	8	16
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKUP[17][4]	SIUL eMIOS_1 DSPI_3 — WKUP	I/O I/O O — I	S	Tristate	—	7	15
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M	Tristate	—	6	14
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKUP[18][4] SIN_3	SIUL eMIOS_1 — — WKUP DSPI_3	I/O I/O — — I I	S	Tristate	—	5	13
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX —	SIUL eMIOS_1 LINFlex_6 —	I/O I/O O —	M	Tristate	—	30	38

Table 14. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	

Table 19. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 20 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below the 100%.

Table 20. I/O weight[1]

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PB[3]	5%	—	6%	—	13%	—	15%	—
			PC[9]	4%	—	5%	—	13%	—	15%	—
			PC[14]	4%	—	4%	—	13%	—	15%	—
			PC[15]	3%	4%	4%	4%	12%	18%	15%	16%
	—	—	PJ[4]	3%	4%	3%	3%	—	—	—	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	1	—	PG[9]	9%	—	10%	—	9%	—	10%	—
		—	PG[8]	9%	—	11%	—	9%	—	11%	—
		1	PC[11]	9%	—	11%	—	9%	—	11%	—
			PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
		—	PG[7]	9%	—	11%	—	9%	—	11%	—
		—	PG[6]	10%	14%	11%	12%	10%	14%	11%	12%
		1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
		—	PF[9]	10%	—	12%	—	10%	—	12%	—
		—	PF[8]	10%	14%	12%	13%	10%	14%	12%	13%
		—	PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
		1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
		—	PF[10]	10%	14%	11%	12%	10%	14%	11%	12%
		—	PF[11]	9%	—	11%	—	9%	—	11%	—
		1	PA[15]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PF[13]	8%	—	10%	—	8%	—	10%	—
		1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	7%	—	9%	—	7%	—	9%	—
			PA[13]	7%	10%	8%	9%	7%	10%	8%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

3.9 Power consumption in different application modes

Table 24 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 24. Electrical characteristics in different application modes[1]

Symbol		C	Parameter	Conditions[2]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[3]	CC	C	RUN mode maximum average current	—		—	81	130[4]	mA
I_{DDRUN}[5]	CC	T	RUN mode typical average current[6]	f_{CPU} = 8 MHz		—	12	—	mA
		T		f_{CPU} = 16 MHz		—	27	—	
		C		f_{CPU} = 32 MHz		—	40	—	
		P		f_{CPU} = 48 MHz		—	54	95	
		P		f_{CPU} = 64 MHz		—	67	120	
I_{DDHALT}	CC	C	HALT mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	10	15	mA
		P			T_A = 125 °C	—	15	28	
I_{DDSTOP}	CC	P	STOP mode current[8]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	130	500	µA
		D			T_A = 55 °C	—	180	—	
		D			T_A = 85 °C	—	1	5	mA
		D			T_A = 105 °C	—	3	9	
		P			T_A = 125 °C	—	5	14	
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	17	80	µA
		C			T_A = 55 °C	—	30	—	
		C			T_A = 85 °C	—	110	—	
		C			T_A = 105 °C	—	280	950	
		C			T_A = 125 °C	—	460	1700	
$I_{DDSTDBY1}$	CC	C	STANDBY1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	12	50	µA
		C			T_A = 55 °C	—	24	—	
		C			T_A = 85 °C	—	48	—	
		C			T_A = 105 °C	—	150	500	
		C			T_A = 125 °C	—	260	—	

1 Except for I_{DDMAX}, all consumptions in this table apply to V_{DD_BV} only and do not include V_{DD_HV}.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3 Running consumption is given on voltage regulator supply (V_{DDREG}). I_{DDMAX} is composed of three components: $I_{DDMAX} = I_{DD}(V_{DD\_BV}) + I_{DD}(V_{DD\_HV}) + I_{DD}(V_{DD\_HV\_ADC})$. It does not include a fourth component linked to I/Os toggling which is **highly** dependent on the application. The given value is thought to be a **worst case value** (64 MHz at 125 °C) with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. Note that this value can be significantly reduced by the application: switch off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 26. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 27. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash power supply DC characteristics

Table 28 shows the power supply DC characteristics on external supply.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 30. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

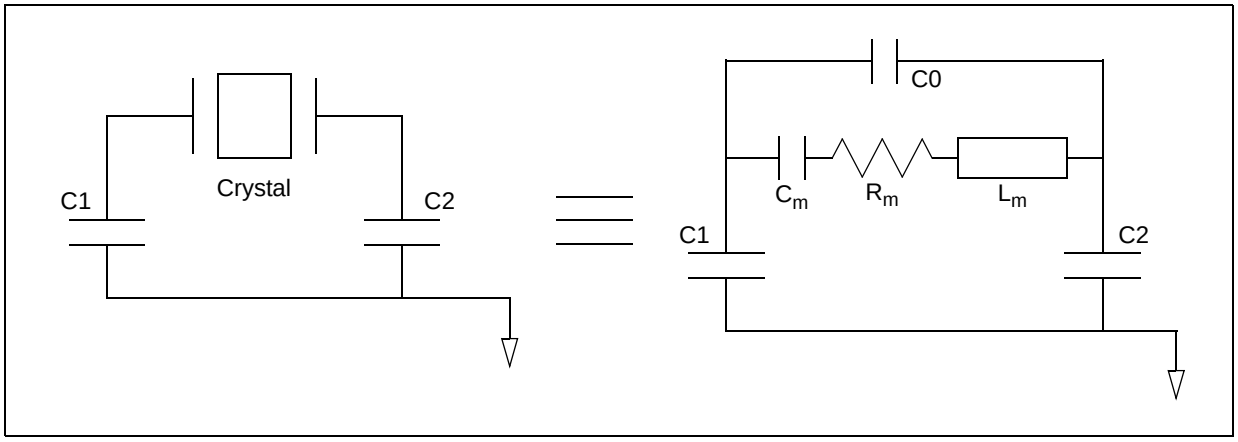


Figure 15. Equivalent circuit of a quartz crystal

Table 35. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled at C0 = 2.85 pF[4]	—	—	65	kΩ
		AC coupled at C0 = 4.9 pF[4]	—	—	50	
		AC coupled at C0 = 7.0 pF[4]	—	—	35	
		AC coupled at C0 = 9.0 pF[4]	—	—	30	

1 The crystal used is Epson Toyocom MC306.

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

Table 37. FMPLL electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	64	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
		P	VCO frequency with frequency modulation	—	245.76	—	532.48	
f_{CPU}	SR	—	System clock frequency	—	—	—	64[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{STJIT}	CC	—	FMPLL short term jitter[5]	f_{sys} maximum	–4	—	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLCLK} at 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 Frequency modulation is considered ± 4%.

4 f_{CPU} 64 MHz can be achieved only at up to 105 °C.

5 Short term jitter is measured on the clock rising edge at cycle *n* and *n* + 4.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed		—	16	—	MHz
	SR	—		—		12		20	
$I_{FIRCRUN}$[2],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	10	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

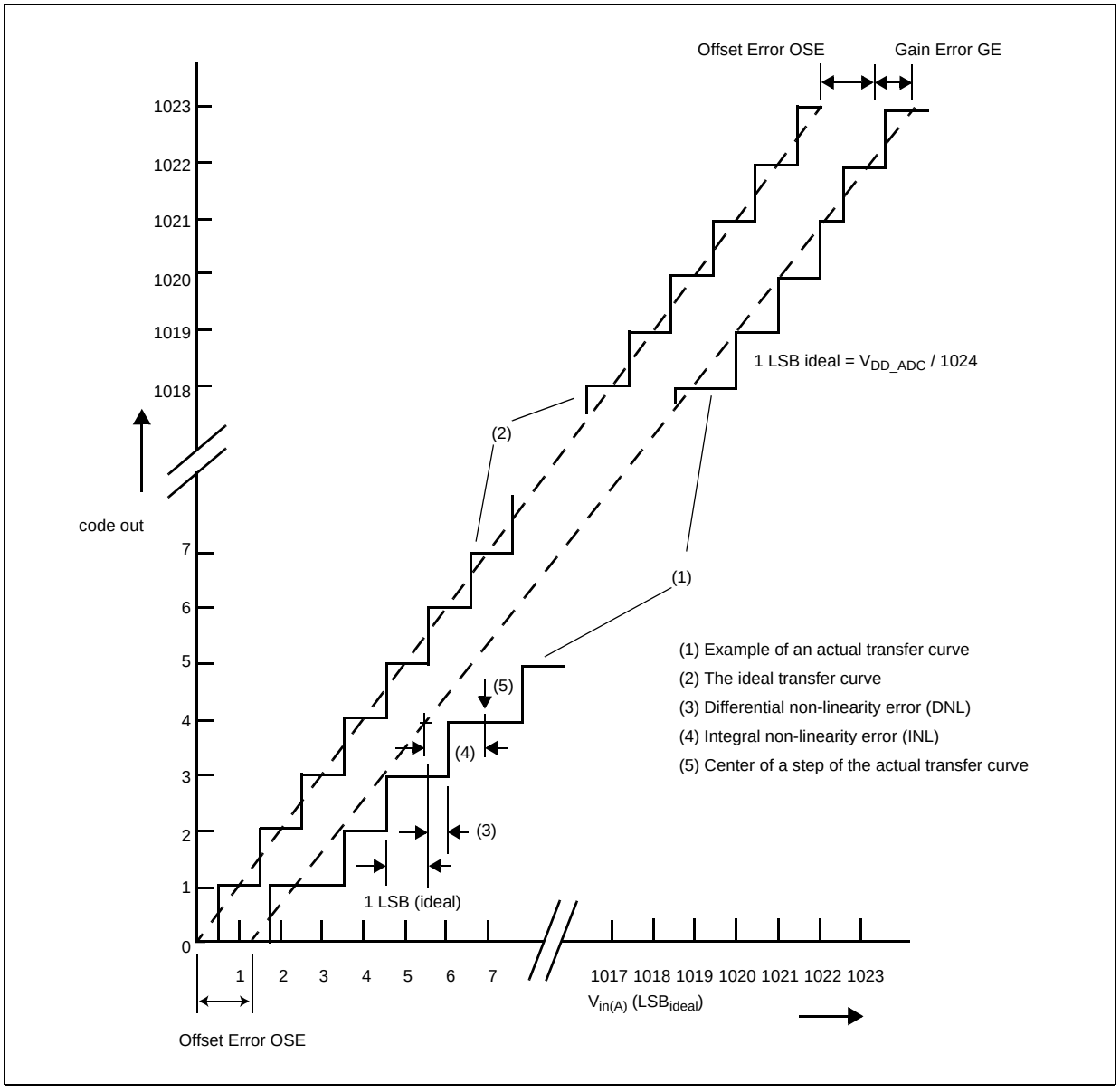


Figure 17. ADC_0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

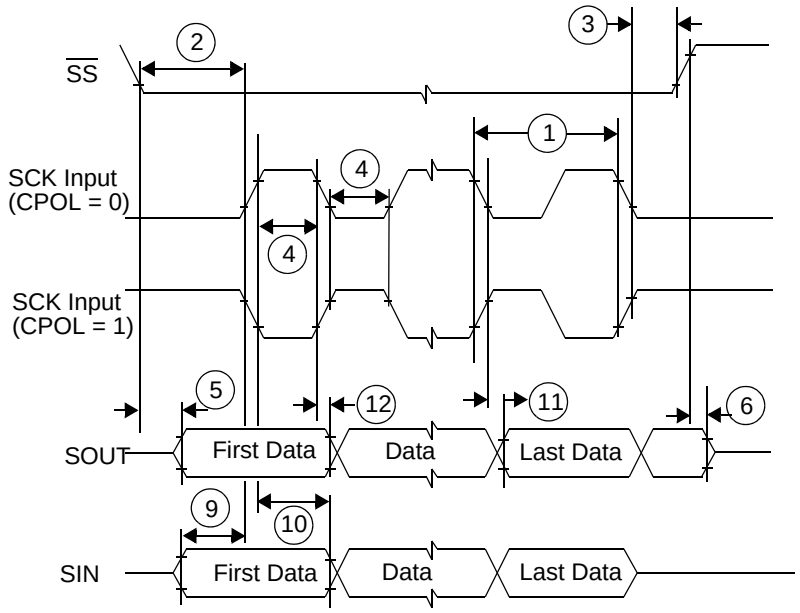
Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sample time[4] VDD = 3.3 V	f_{ADC1} = 20 MHz, ADC1_conf_sample_input = 12	600	—	—	ns
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 17	500	—	—	
			Sample time[4] VDD = 3.3 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	µs
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] VDD = 3.3 V	f_{ADC1} = 20MHz, ADC1_conf_comp = 0	2.4	—	—	µs
			Conversion time[5] VDD = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, ADC1_conf_comp = 0	1.5	—	—	µs
			Conversion time[5] VDD = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
			Conversion time[5] VDD = 5.0 V	f_{ADC1} = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Table 43. On-chip peripherals current consumption[1] (continued)

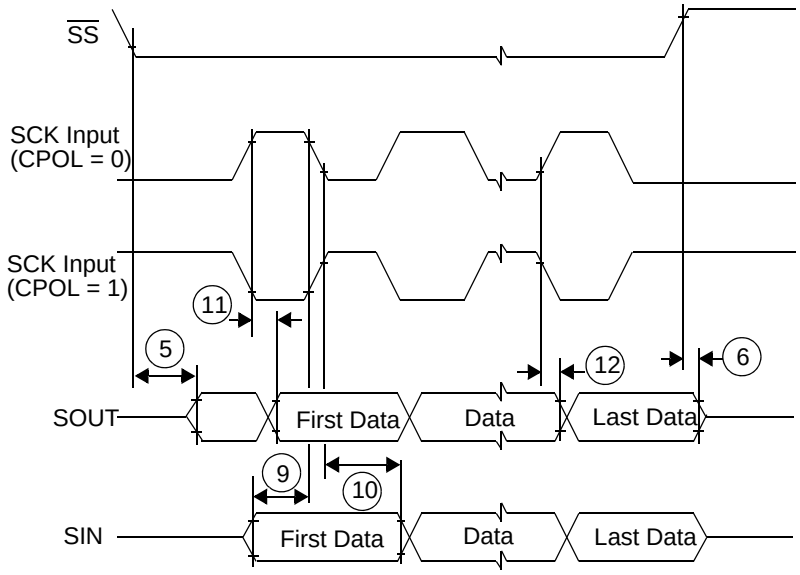
Symbol		C	Parameter	Conditions		Value	Unit
						Typ	
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_BV(PLL)}$	CC	T	PLL supply current on V_{DD_BV}	V_{DD} = 5.5 V	—	2.5	mA

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz



Note: Numbers shown reference Table 44.

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Numbers shown reference Table 44.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1

4 Package characteristics

4.1 Package mechanical data

4.1.1 176 LQFP

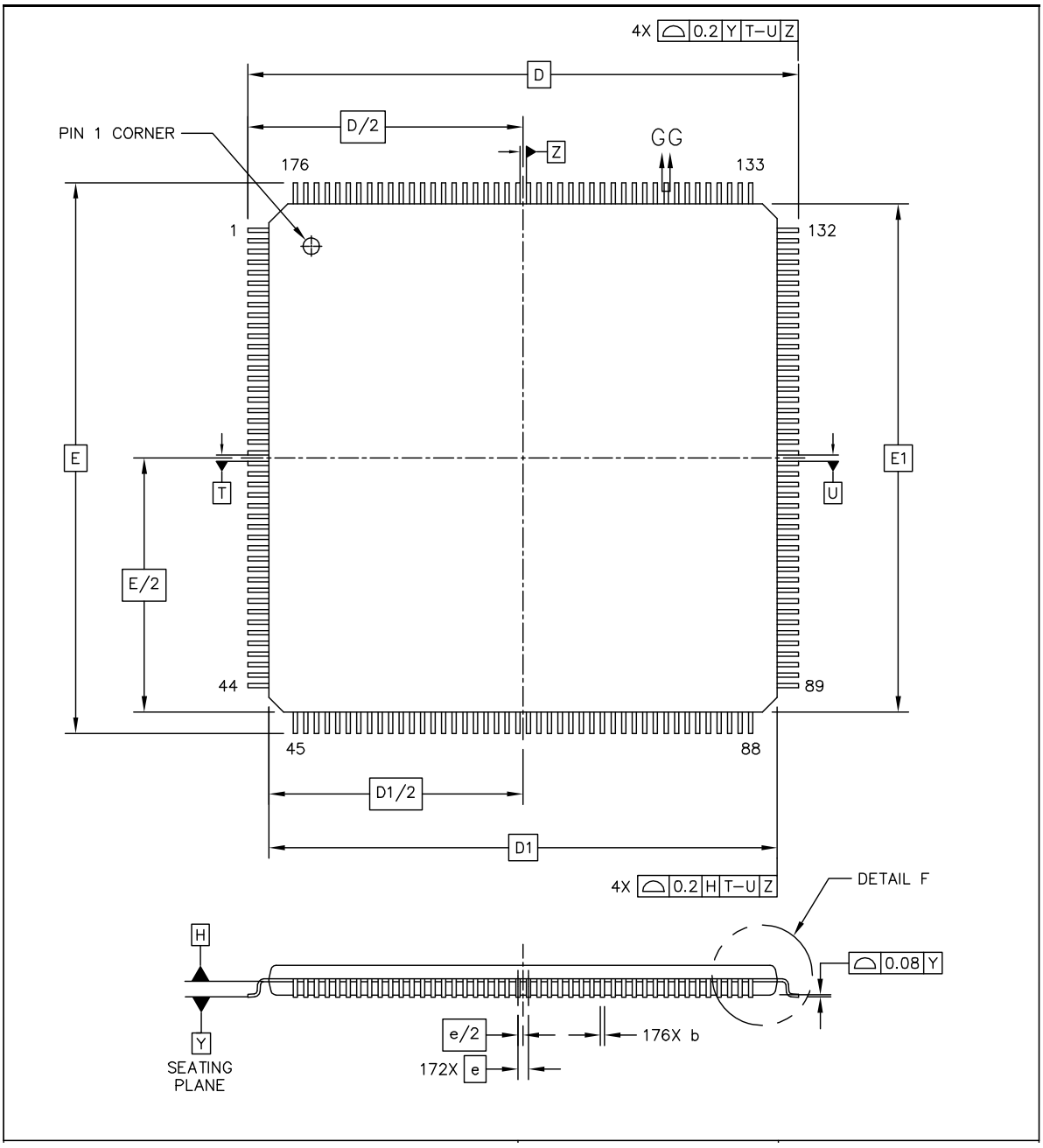


Figure 33. 176 LQFP package mechanical drawing (Part 1 of 3)

4.1.2 144 LQFP

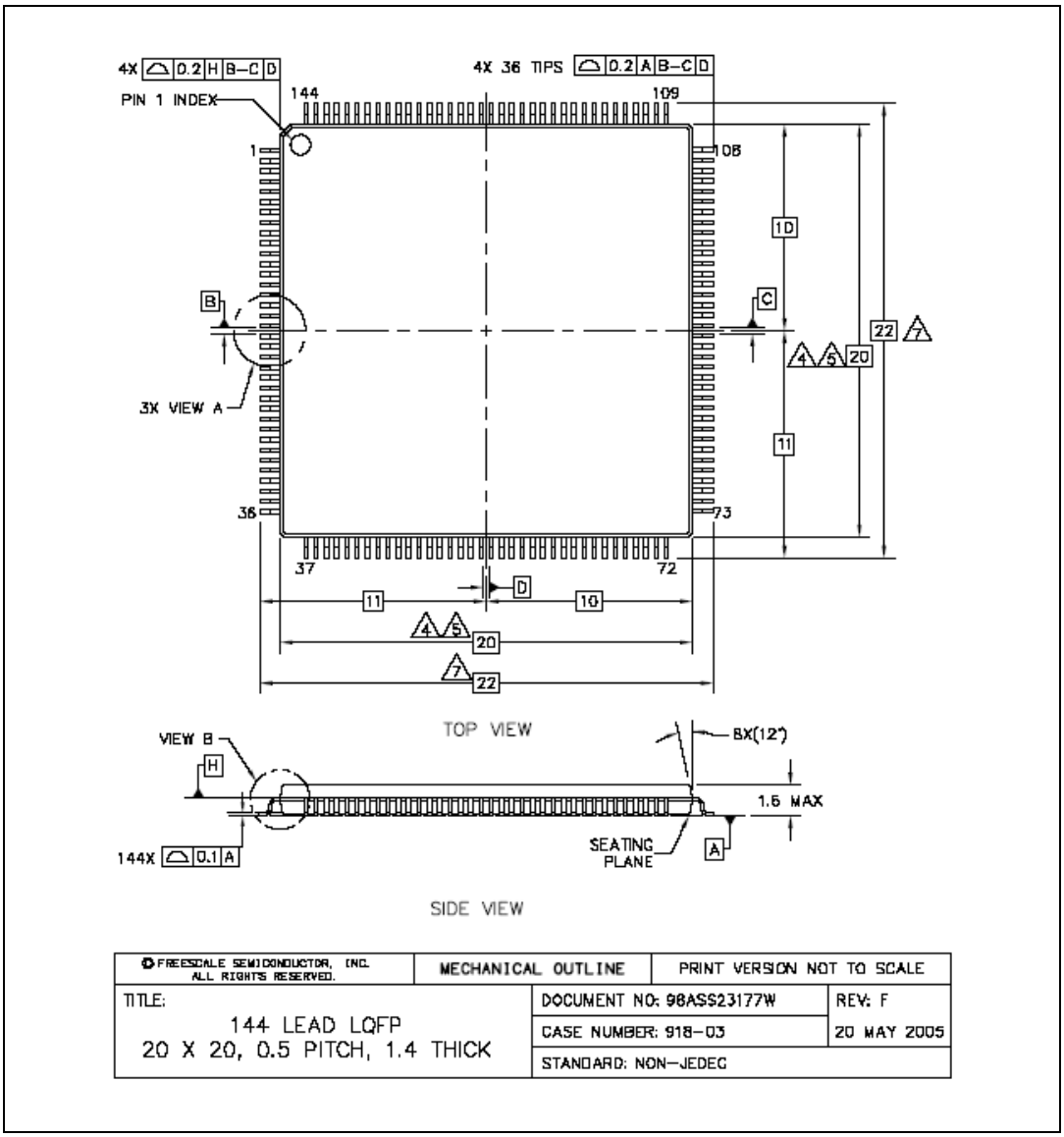


Figure 36. 144 LQFP package mechanical drawing (Part 1 of 2)