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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0mlq6

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	68	82
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	69	83
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	70	84
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	49	71	87
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	56	78	94
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	57	79	95
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	58	80	96
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	—	—	100

3.2.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 7 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 7. WATCHDOG_EN field description[1]

Value[2]	Description
0	Disable after reset
1	Enable after reset

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is '1'. This value can be programmed by the customer in Shadow Flash.

3.3 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

Table 11. LQFP thermal characteristics[1] (continued)

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JC}$	CC		Thermal resistance, junction-to-case[5]	Single-layer board — 1s	100	—	—	23	°C/W
					144	—	—	23	
					176	—	—	23	
				Four-layer board — 2s2p	100	—	—	19.8	
					144	—	—	19.2	
					176	—	—	18.8	

1 Thermal characteristics are targets based on simulation.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C.

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

4 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

5 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

3.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

Table 14. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	

Table 21. Reset electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100 pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to the MC_RGM chapter of the *MPC5606BK Microcontroller Reference Manual*).

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

4 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 3.4, Recommended operating conditions).

The internal voltage regulator requires controlled slew rate of V_{DD}/V_{DD_BV} as described in Figure 9.

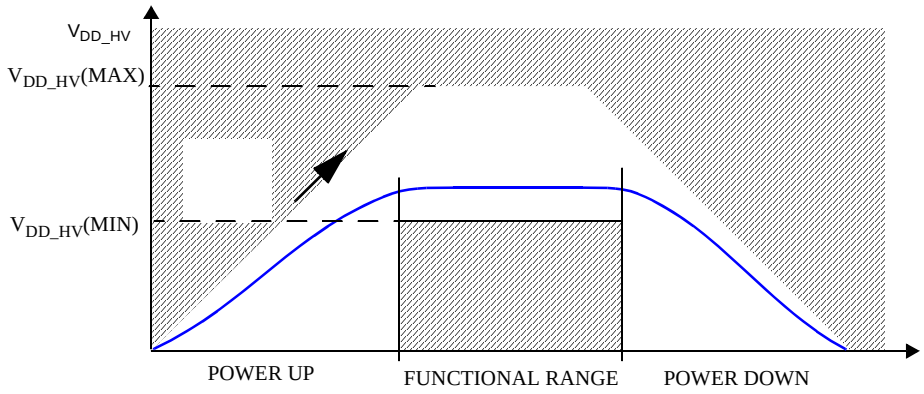


Figure 9. V_{DD} and V_{DD_BV} maximum slope

When STANDBY mode is used, further constraints apply to the V_{DD}/V_{DD_BV} in order to guarantee correct regulator functionality during STANDBY exit. This is described in Figure 10.

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of C_{STDBY} capacitance on application board (capacitance and ESR typical values), but would actually depend on the exact characteristics of the application's external regulator.

3.9 Power consumption in different application modes

Table 24 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 24. Electrical characteristics in different application modes[1]

Symbol		C	Parameter	Conditions[2]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[3]	CC	C	RUN mode maximum average current	—		—	81	130[4]	mA
I_{DDRUN}[5]	CC	T	RUN mode typical average current[6]	f_{CPU} = 8 MHz		—	12	—	mA
		T		f_{CPU} = 16 MHz		—	27	—	
		C		f_{CPU} = 32 MHz		—	40	—	
		P		f_{CPU} = 48 MHz		—	54	95	
		P		f_{CPU} = 64 MHz		—	67	120	
I_{DDHALT}	CC	C	HALT mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	10	15	mA
		P			T_A = 125 °C	—	15	28	
I_{DDSTOP}	CC	P	STOP mode current[8]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	130	500	µA
		D			T_A = 55 °C	—	180	—	
		D			T_A = 85 °C	—	1	5	mA
		D			T_A = 105 °C	—	3	9	
		P			T_A = 125 °C	—	5	14	
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	17	80	µA
		C			T_A = 55 °C	—	30	—	
		C			T_A = 85 °C	—	110	—	
		C			T_A = 105 °C	—	280	950	
		C			T_A = 125 °C	—	460	1700	
$I_{DDSTDBY1}$	CC	C	STANDBY1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	12	50	µA
		C			T_A = 55 °C	—	24	—	
		C			T_A = 85 °C	—	48	—	
		C			T_A = 105 °C	—	150	500	
		C			T_A = 125 °C	—	260	—	

1 Except for I_{DDMAX}, all consumptions in this table apply to V_{DD_BV} only and do not include V_{DD_HV}.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3 Running consumption is given on voltage regulator supply (V_{DDREG}). I_{DDMAX} is composed of three components: $I_{DDMAX} = I_{DD}(V_{DD\_BV}) + I_{DD}(V_{DD\_HV}) + I_{DD}(V_{DD\_HV\_ADC})$. It does not include a fourth component linked to I/Os toggling which is **highly** dependent on the application. The given value is thought to be a **worst case value** (64 MHz at 125 °C) with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. Note that this value can be significantly reduced by the application: switch off unused peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 26. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 27. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash power supply DC characteristics

Table 28 shows the power supply DC characteristics on external supply.

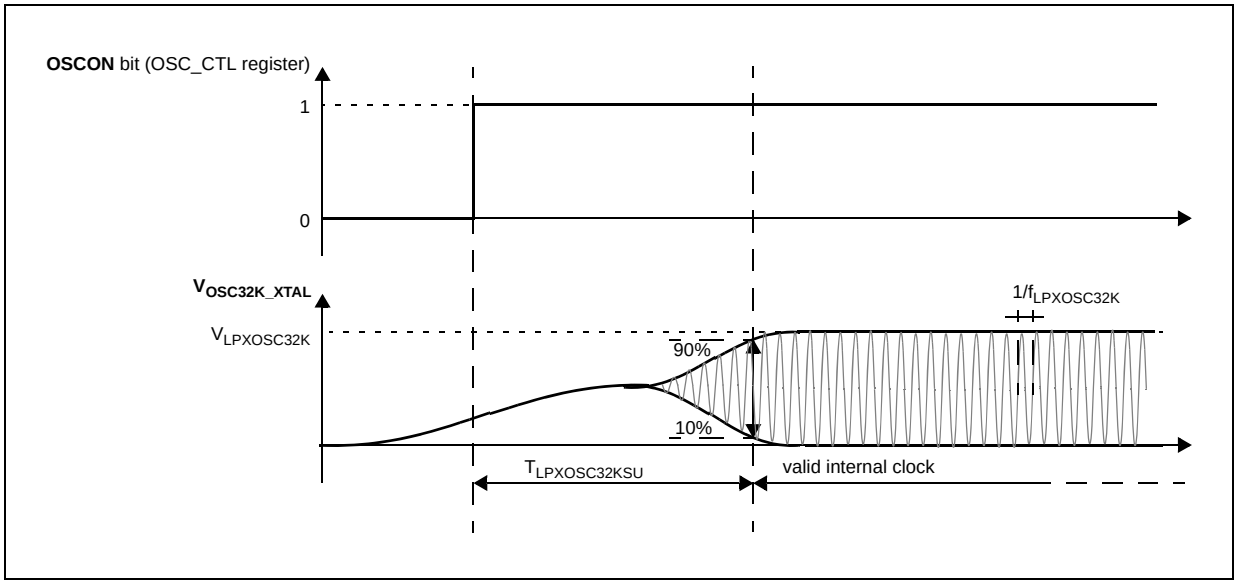


Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 36. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the FXOSC or FIRC sources.

Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%

Table 37. FMPLL electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	64	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
		P	VCO frequency with frequency modulation	—	245.76	—	532.48	
f_{CPU}	SR	—	System clock frequency	—	—	—	64[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{STJIT}	CC	—	FMPLL short term jitter[5]	f_{sys} maximum	–4	—	4	%
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLCLK} at 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 Frequency modulation is considered ± 4%.

4 f_{CPU} 64 MHz can be achieved only at up to 105 °C.

5 Short term jitter is measured on the clock rising edge at cycle *n* and *n* + 4.

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed		—	16	—	MHz
	SR	—		—		12		20	
$I_{FIRCRUN}$[2],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed		—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	10	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

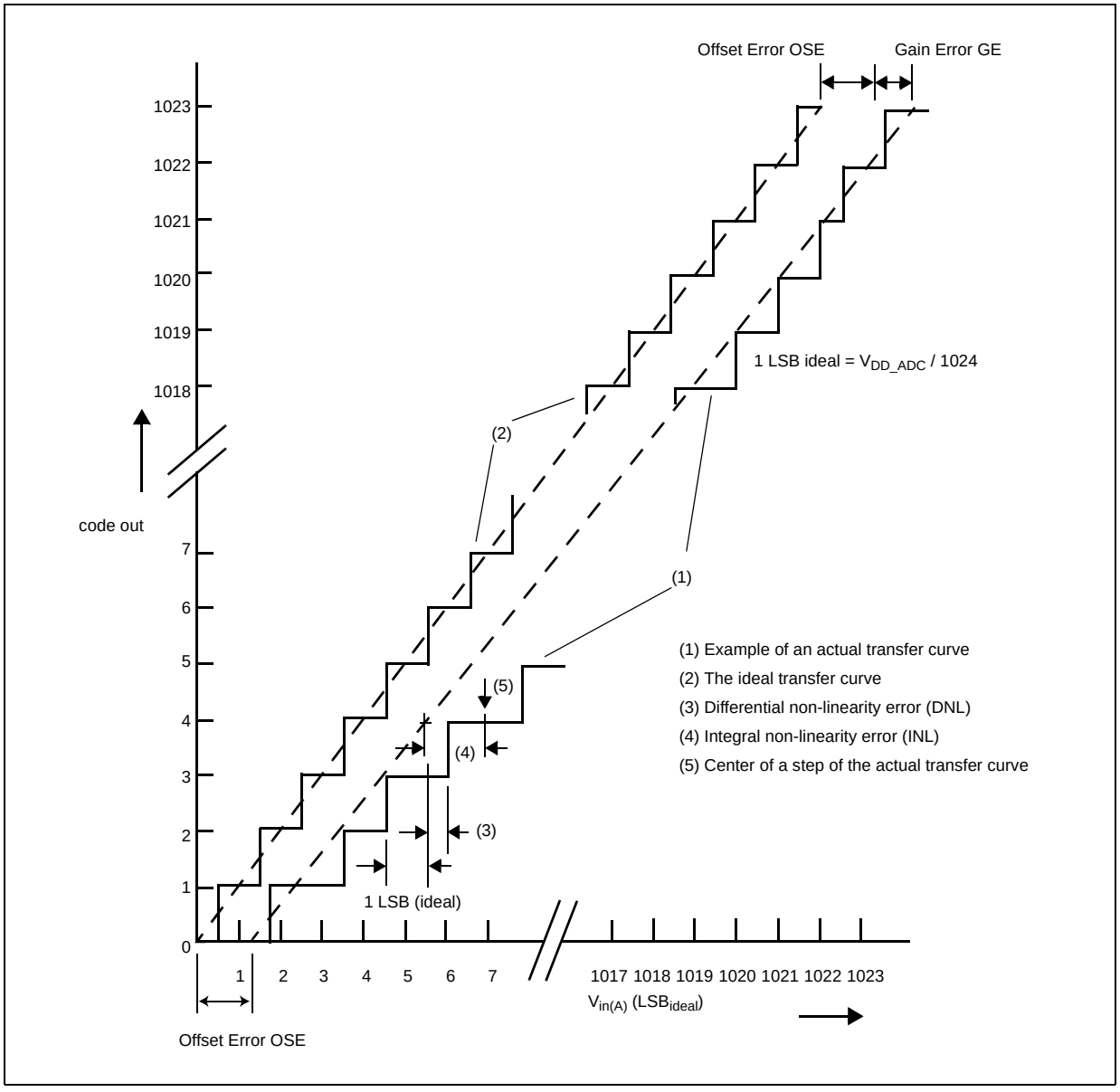


Figure 17. ADC_0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

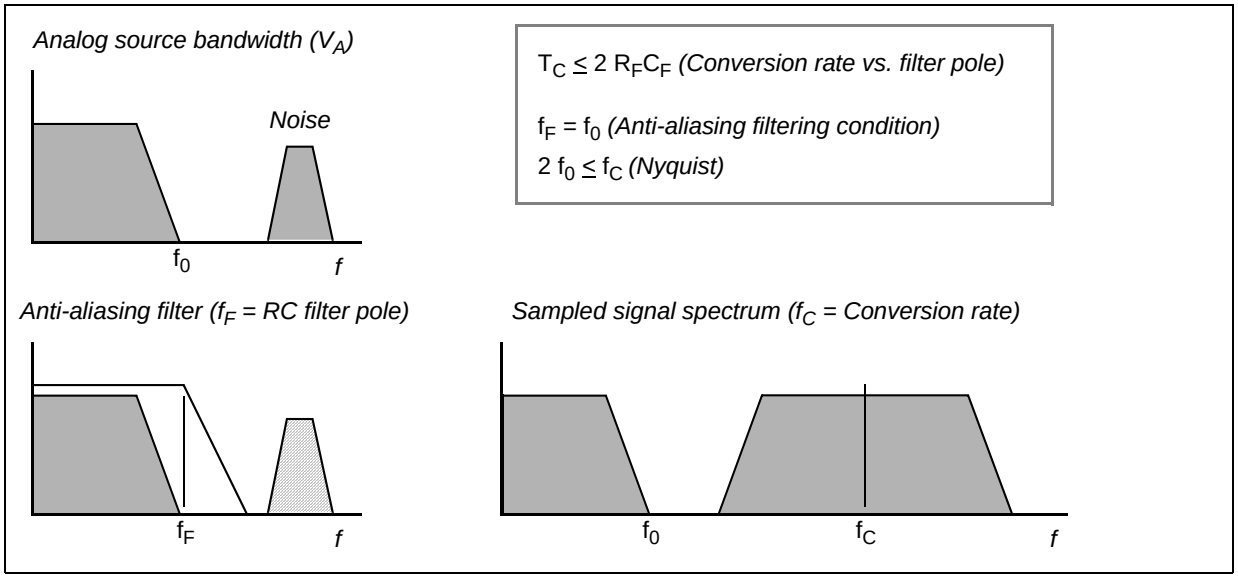


Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC_0 (10-bit) ***Eqn. 12***

$$C_F > 2048 \bullet C_S$$

ADC_1 (12-bit) ***Eqn. 13***

$$C_F > 8192 \bullet C_S$$

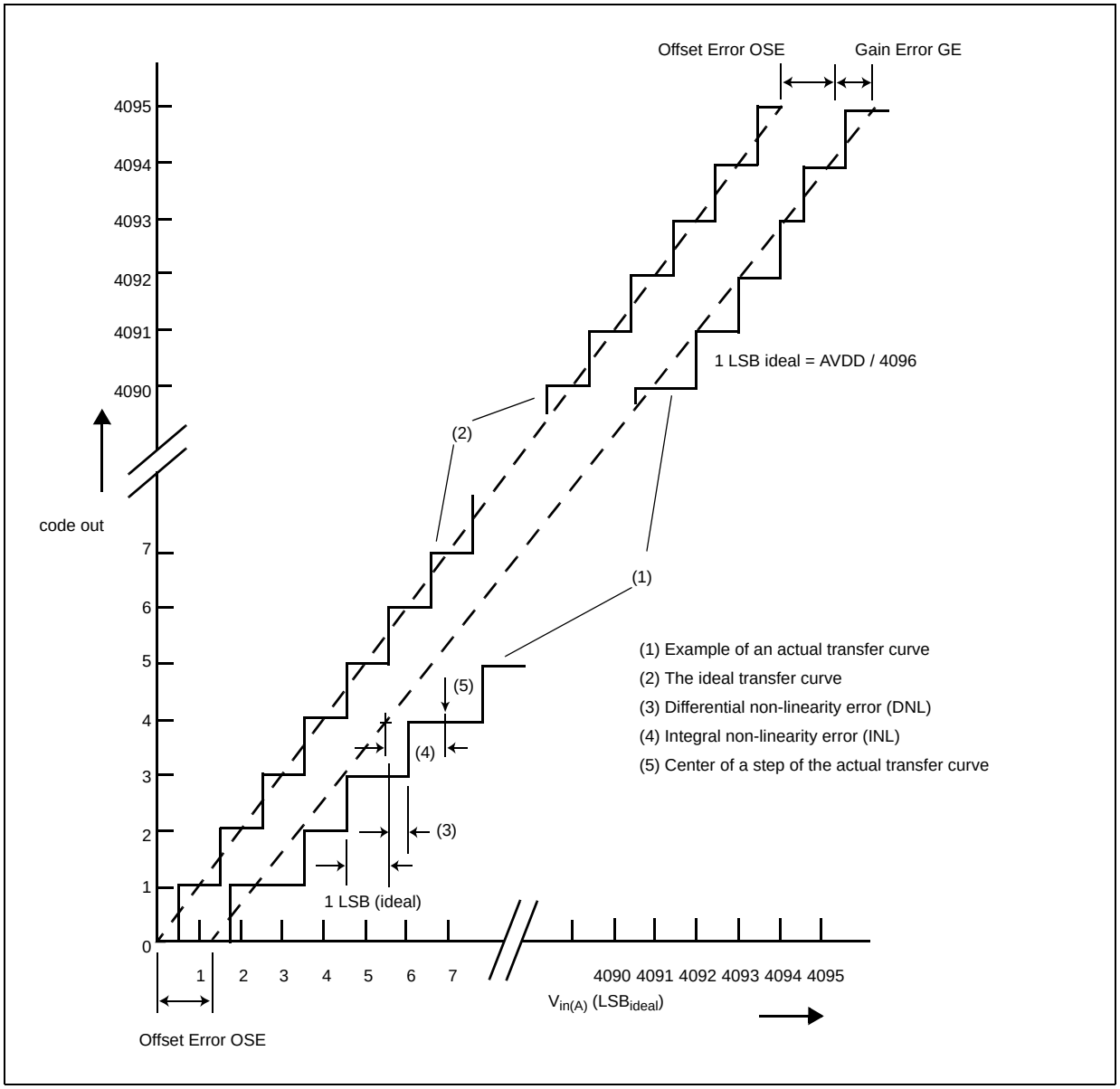


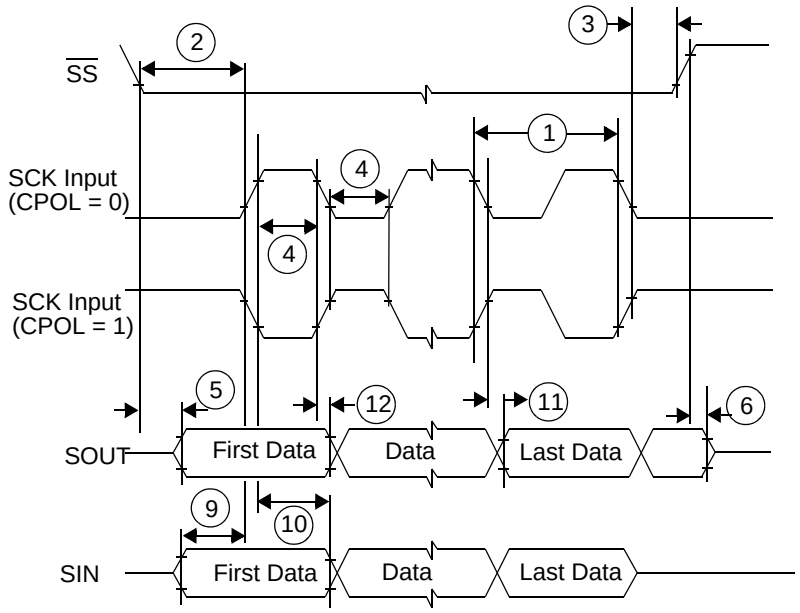
Figure 22. ADC_1 characteristic and error definitions

Table 42. ADC_1 conversion characteristics (12-bit ADC_1)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V

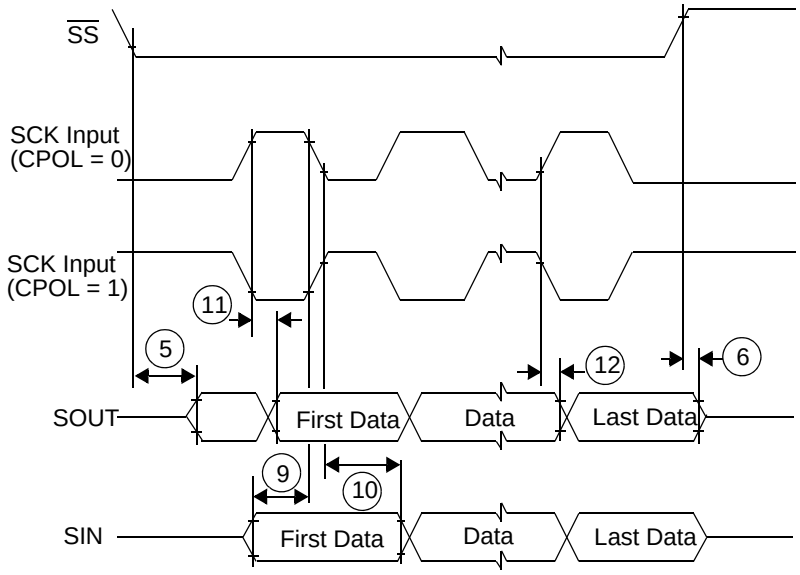
Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sample time[4] VDD = 3.3 V	f_{ADC1} = 20 MHz, ADC1_conf_sample_input = 12	600	—	—	ns
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 17	500	—	—	
			Sample time[4] VDD = 3.3 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	µs
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] VDD = 3.3 V	f_{ADC1} = 20MHz, ADC1_conf_comp = 0	2.4	—	—	µs
			Conversion time[5] VDD = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, ADC1_conf_comp = 0	1.5	—	—	µs
			Conversion time[5] VDD = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
			Conversion time[5] VDD = 5.0 V	f_{ADC1} = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ



Note: Numbers shown reference Table 44.

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Numbers shown reference Table 44.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1

4 Package characteristics

4.1 Package mechanical data

4.1.1 176 LQFP

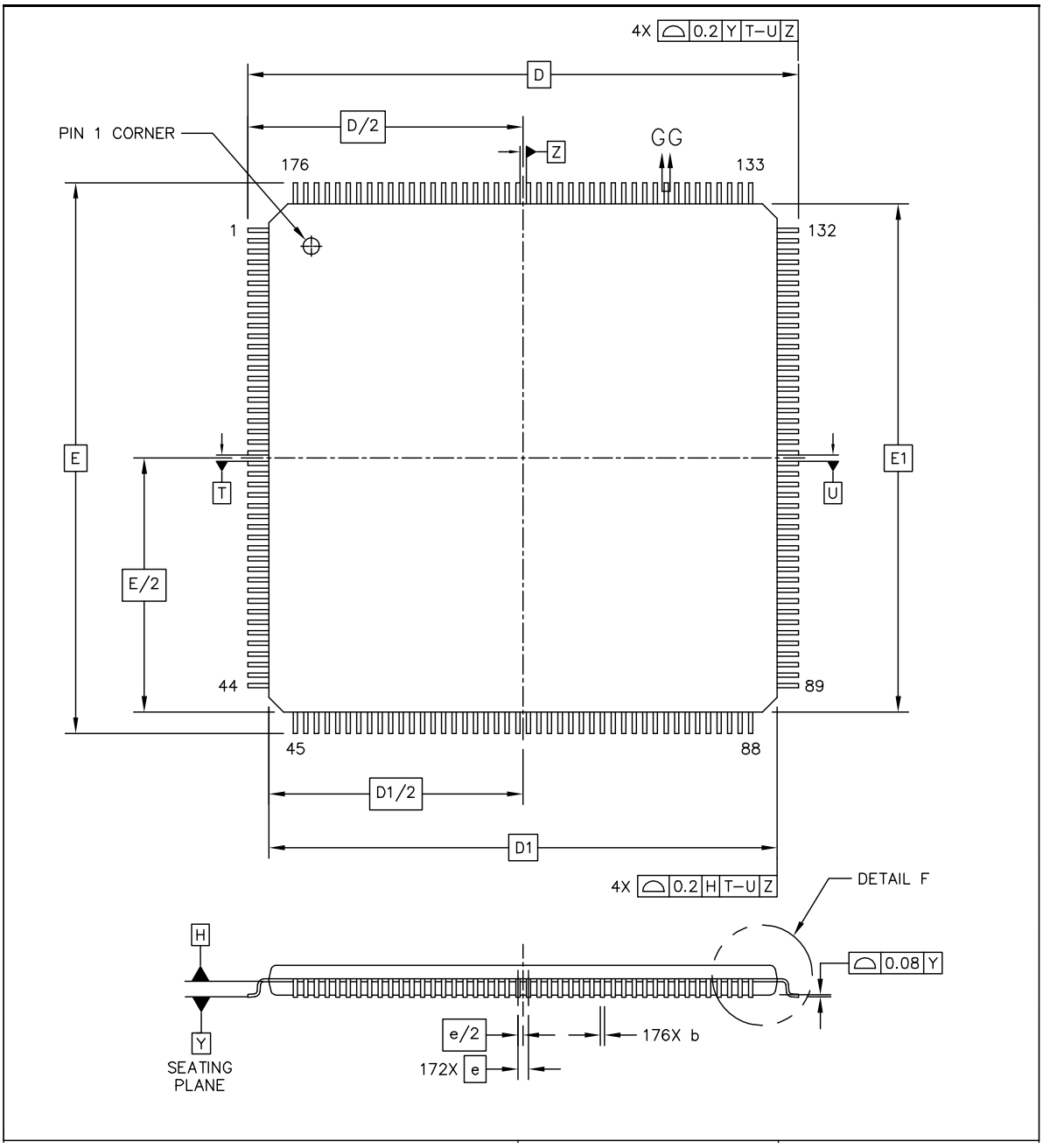


Figure 33. 176 LQFP package mechanical drawing (Part 1 of 3)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

Figure 35. 176 LQFP package mechanical drawing (Part 3 of 3)

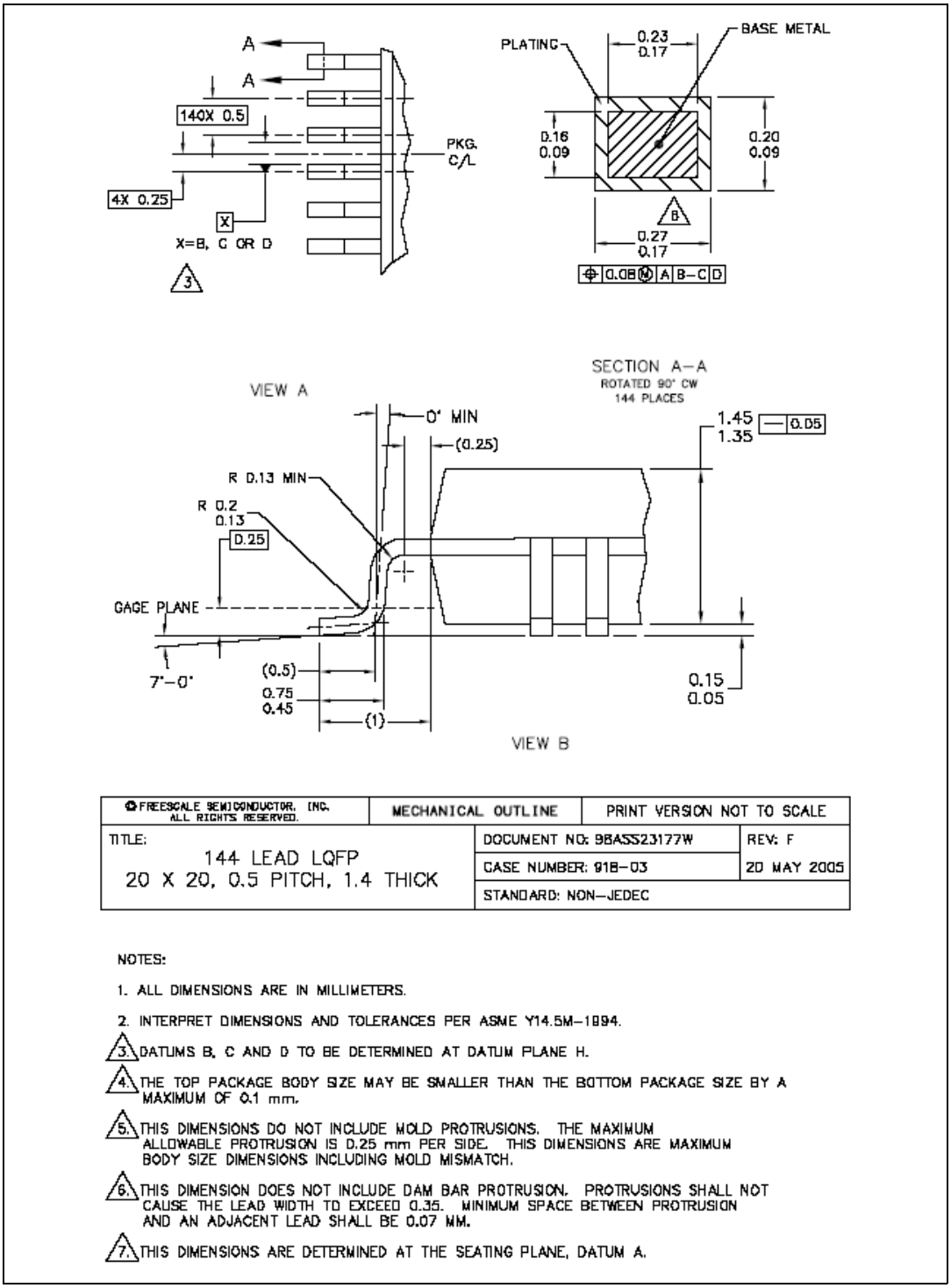
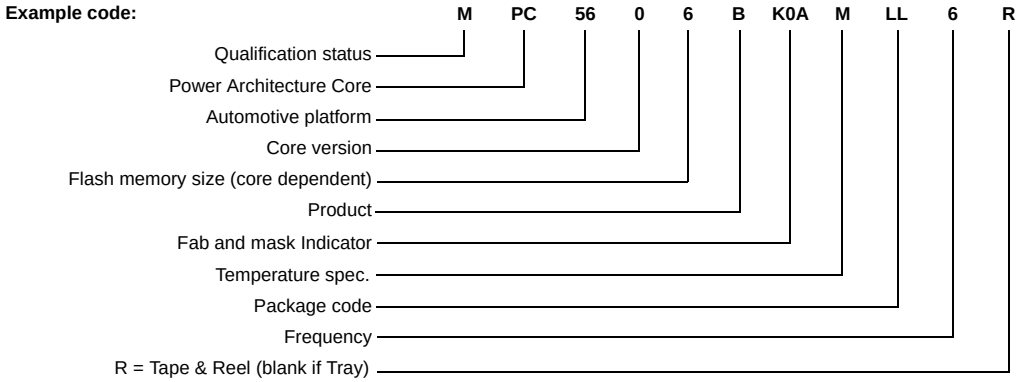


Figure 37. 144 LQFP package mechanical drawing (Part 2 of 2)

5 Ordering information



Qualification status
M = General market qualified
S = Automotive qualified
P = Engineering samples

Automotive Platform
56 = Power Architecture in 90nm

Core version
0 = e200z0

Flash memory size (for z0 core)
5 = 768 KB
6 = 1024 KB

Product
B = Body

Fab and mask Indicator
K = TSMC Fab
0 = Version of the maskset
A = Mask set indicator (Blank = 1st production maskset, A = 2nd, B = 3rd, etc)

Temperature spec.
C = –40 to 85 °C
V = –40 to 105 °C
M = –40 to 125 °C

Package code
LL = 100 LQFP
LQ = 144 LQFP
LU = 176 LQFP

Frequency
4 = Up to 48 MHz
6 = Up to 64 MHz

Note: Not all options are available on all devices.

Figure 41. Commercial product code structure

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