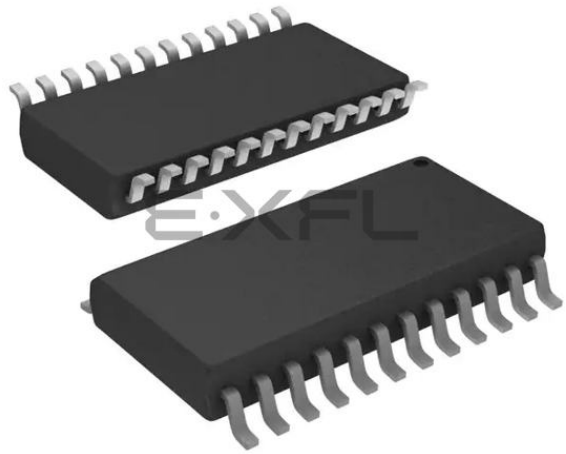


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63be2m1

Contents

1 Introduction

The ST7263B microcontrollers form a sub-family of the ST7 MCUs dedicated to USB applications. The devices are based on an industry-standard 8-bit core and feature an enhanced instruction set. They operate at a 24 MHz or 12 MHz oscillator frequency. Under software control, the ST7263B MCUs may be placed in either Wait or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST7263B MCUs feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The devices include an ST7 core, up to 32 Kbytes of program memory, up to 1024 bytes of RAM, 27 I/O lines and the following on-chip peripherals:

- USB low speed interface with 3 endpoints with programmable in/out configuration using the DMA architecture with embedded 3.3 V voltage regulator and transceivers (no external components are needed).
- 8-bit analog-to-digital converter (ADC) with 12 multiplexed analog inputs
- Industry standard asynchronous SCI serial interface
- Watchdog
- 16-bit Timer featuring an External clock input, 2 input Captures, 2 output Compares with Pulse Generator capabilities
- Fast I²C multimaster interface
- Low voltage reset (LVD) ensuring proper power-on or power-off of the device

The ST72F63B devices are Flash versions. They support programming in IAP mode (In-application programming) via the on-chip USB interface.

Table 2. Device overview

Features	ST7263BHx			ST7263BDx	ST7263BKx				ST7263BEx			
Program memory - Kbytes (Flash / ROM)	32	16	8	32	32	16	8	4	32	16	8	4
RAM (stack) - bytes	1024 (128)	512 (128)	384 (128)	1024 (128)	1024 (128	512 (128)	384 (128)	384 (128	1024 (128)	512 (128)	384 (128)	384 (128)
Standard Peripherals	Watchdog timer, 16-bit timer, USB											
Other Peripherals	SCI, I²C, ADC						SCI, AD	ADC	SCI, I²C			
I/Os (high current)	27 (10)				19 (10)				14 (6)			
Operating Supply	4.0 V to 5.5 V											
CPU frequency	8 MHz (with 24 MHz oscillator) or 4 MHz (with 12 MHz oscillator)											
Operating temp.	0 °C to +70 °C											
Packages	LQFP48 (7x7)			QFN40 (6x6)	SDIP32/ SO34		QFN40 (6x6)	SDIP32/ SO34	SO24			

Figure 12. Low voltage detector functional diagram

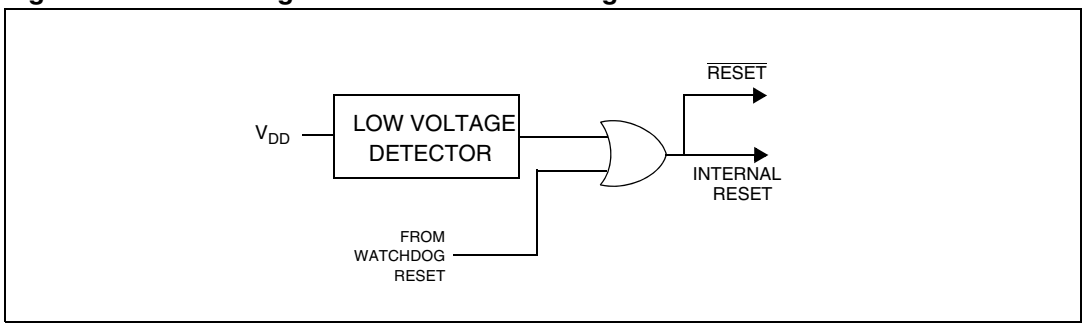
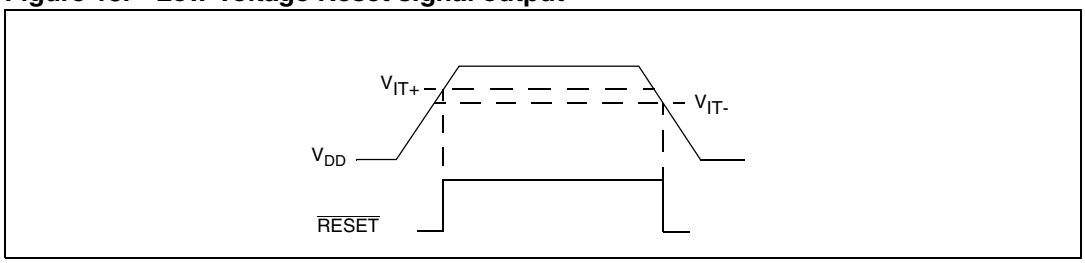


Figure 13. Low Voltage Reset signal output



1. Hysteresis (V_{IT+}-V_{IT-}) = V_{hys}

Figure 14. Temporization timing diagram after an internal Reset

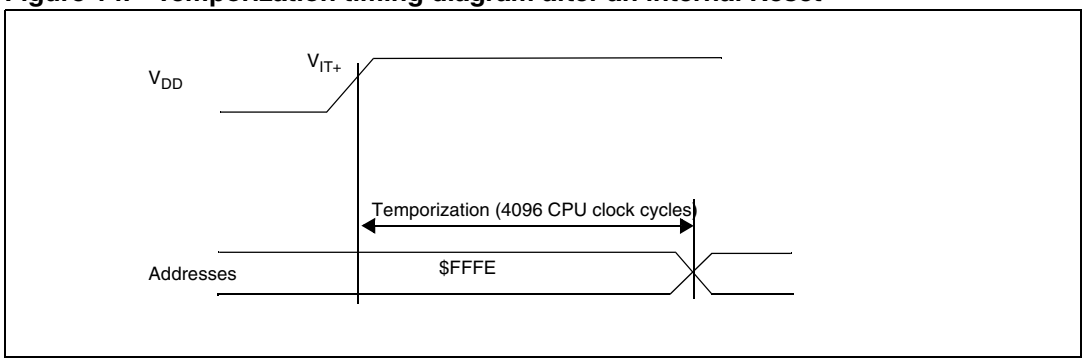


Figure 17. Crystal/ceramic resonator

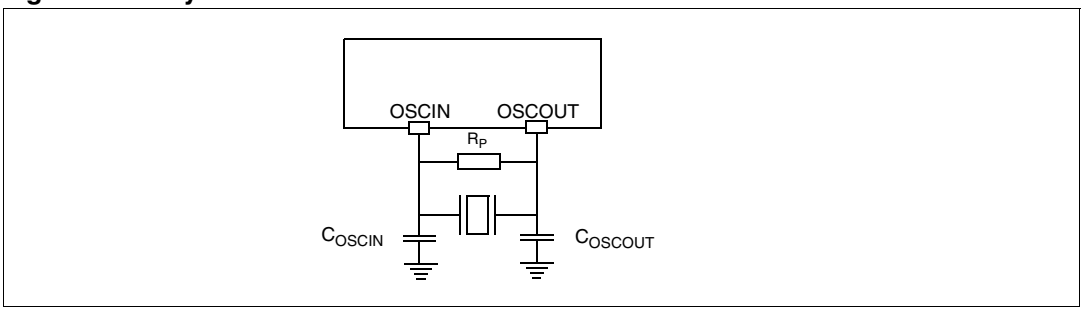
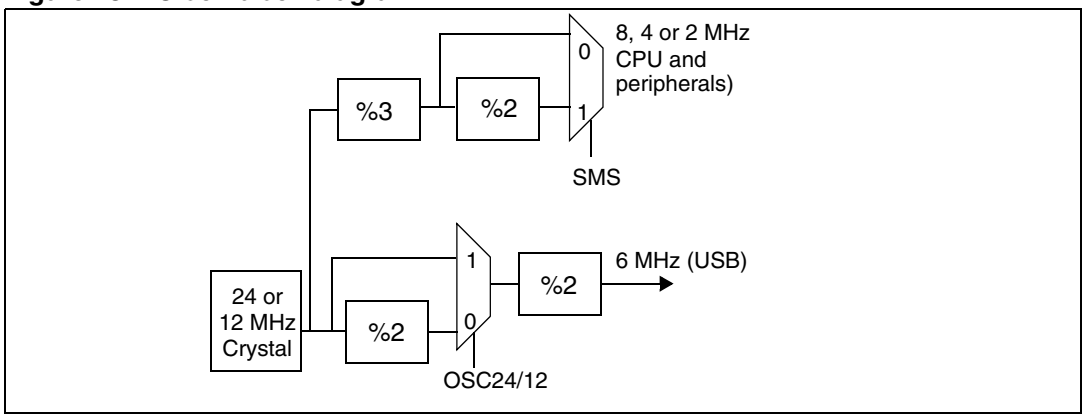


Figure 18. Clock block diagram



The MCU will remain in Wait mode until a Reset or an interrupt occurs, causing it to wake up. Refer to *Figure 21*.

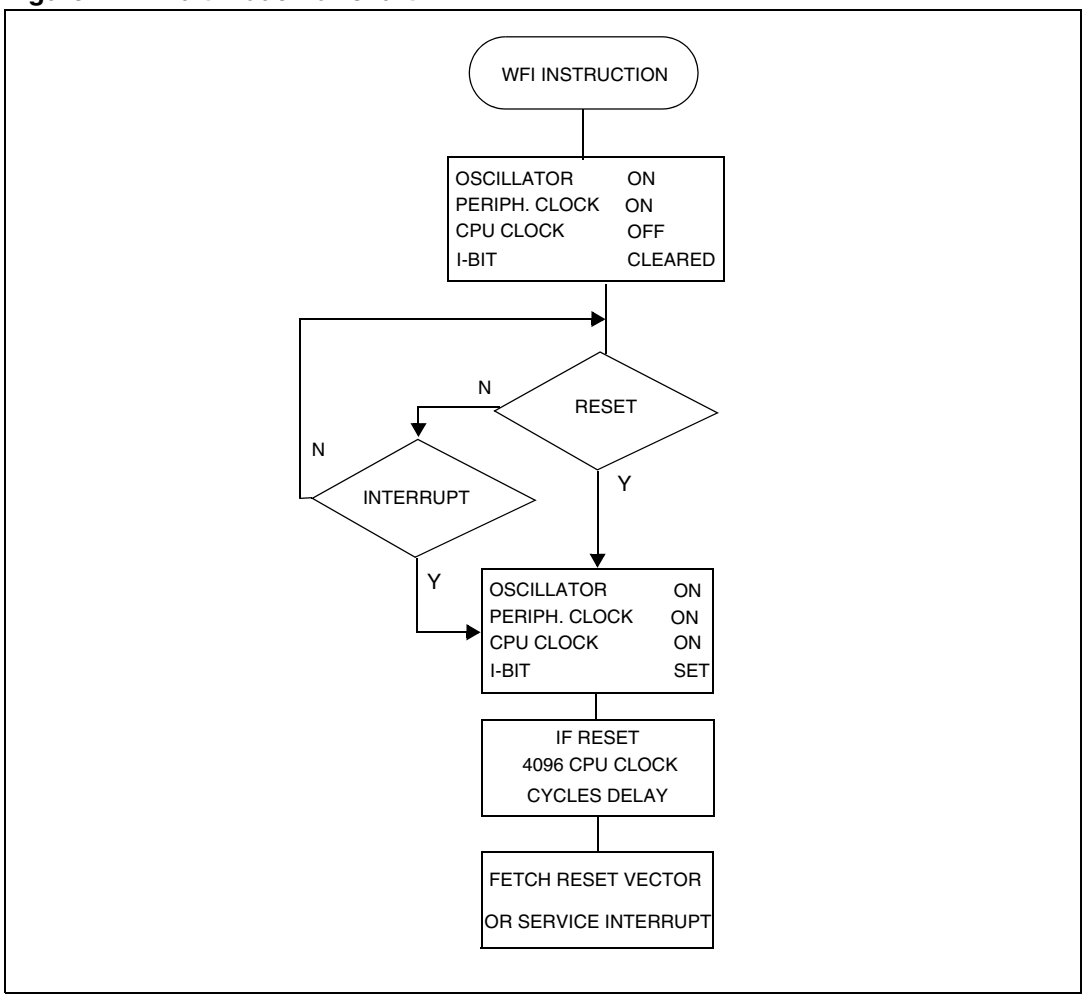
Related documentation

AN 980: ST7 Keypad Decoding Techniques, Implementing Wakeup on Keystroke

AN1014: How to Minimize the ST7 Power Consumption

AN1605: Using an active RC to wakeup the ST7LITE0 from power saving mode

Figure 21. Wait mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I-Bit is set during the interrupt routine and cleared when the CC register is popped.

9 I/O ports

9.1 Introduction

The I/O ports offer different functional modes:

- Transfer of data through digital inputs and outputs and for specific pins
- Analog signal input (ADC)
- Alternate signal input/output for the on-chip peripherals
- External interrupt generation

An I/O port consists of up to 8 pins. Each pin can be programmed independently as a digital input (with or without interrupt generation) or a digital output.

9.2 Functional description

Each port is associated to 2 main registers:

- Data register (DR)
- Data Direction register (DDR)

Each I/O pin may be programmed using the corresponding register bits in DDR register: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

Table 10. I/O pin functions

DDR	Mode
0	Input
1	Output

Input modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Note: 1 All the inputs are triggered by a Schmitt trigger.

2 When switching from input mode to output mode, the DR register should be written first to output the correct value as soon as the port is configured as an output.

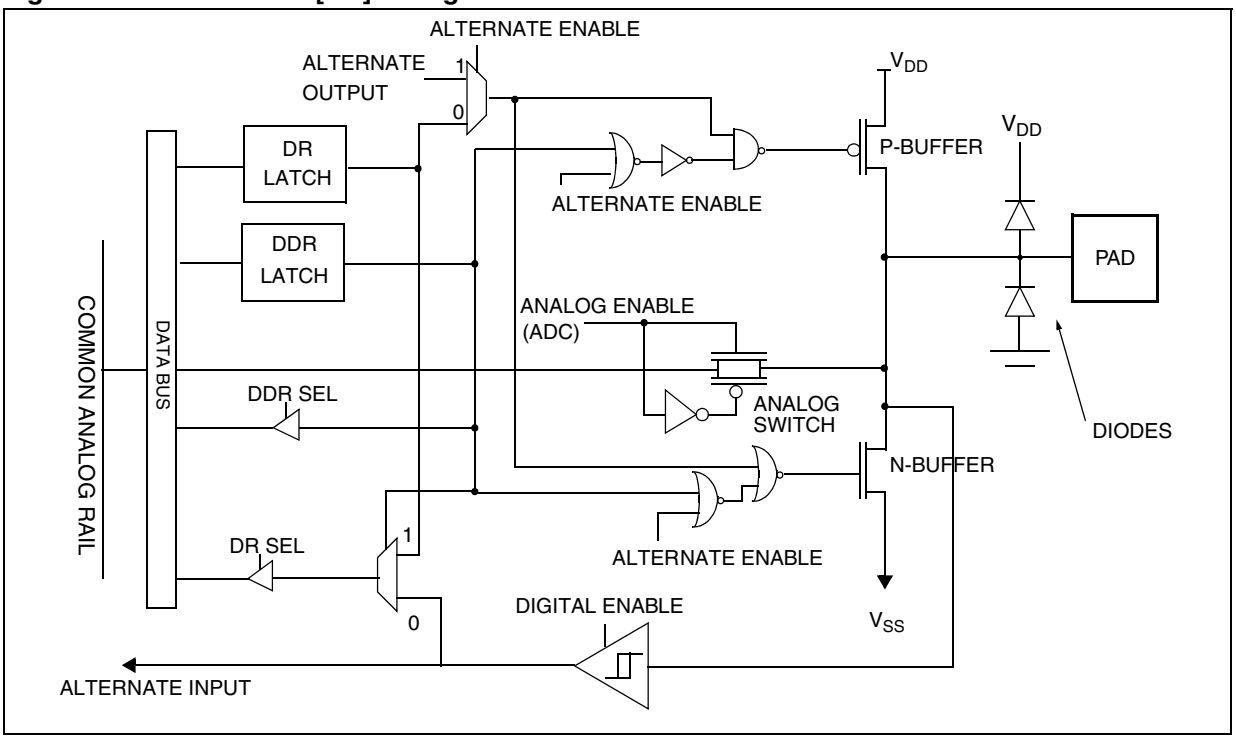
Interrupt function

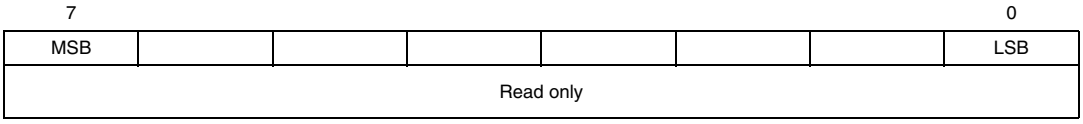
When an I/O is configured as an input with interrupt, an event on this I/O can generate an external interrupt request to the CPU. The interrupt sensitivity is given independently according to the description mentioned in the ITRFRE interrupt register.

Each pin can independently generate an interrupt request.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see interrupts section). If more than one input pin is selected simultaneously as an interrupt source, this is logically ORed. For this reason if one of the interrupt pins is tied low, the other ones are masked.

Figure 24. Port B and D[3:0] configuration

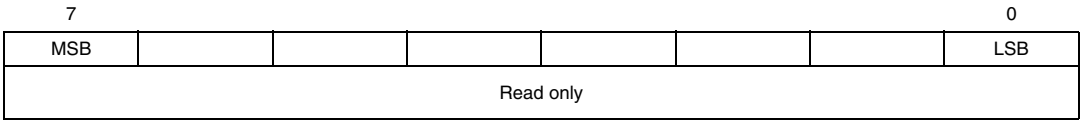




Alternate Counter Low register (ACLR)

Reset value: 1111 1100 (FCh)

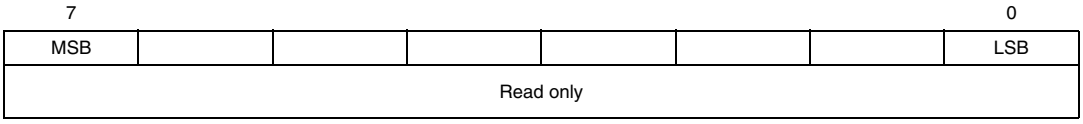
This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to CSR register does not clear the TOF bit in the CSR register.



Input Capture 2 High register (IC2HR)

Reset value: Undefined

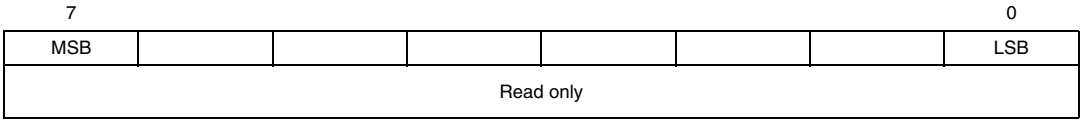
This is an 8-bit read only register that contains the high part of the counter value (transferred by the input Capture 2 event).



Input Capture 2 Low register (IC2LR)

Reset value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input Capture 2 event).



11.3 Serial communications interface (SCI)

11.3.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

11.3.2 Main features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Independently programmable transmit and receive baud rates up to 250K baud.
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- Two receiver Wakeup modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- Four error detection flags:
  - Overrun error
  - Noise error
  - Frame error
  - Parity error
- Six interrupt sources with flags:
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error detected
  - Parity error
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

11.3.3 General description

The interface is externally connected to another device by two pins (see *Figure 42*):

- TDO: Transmit Data output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive Data input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

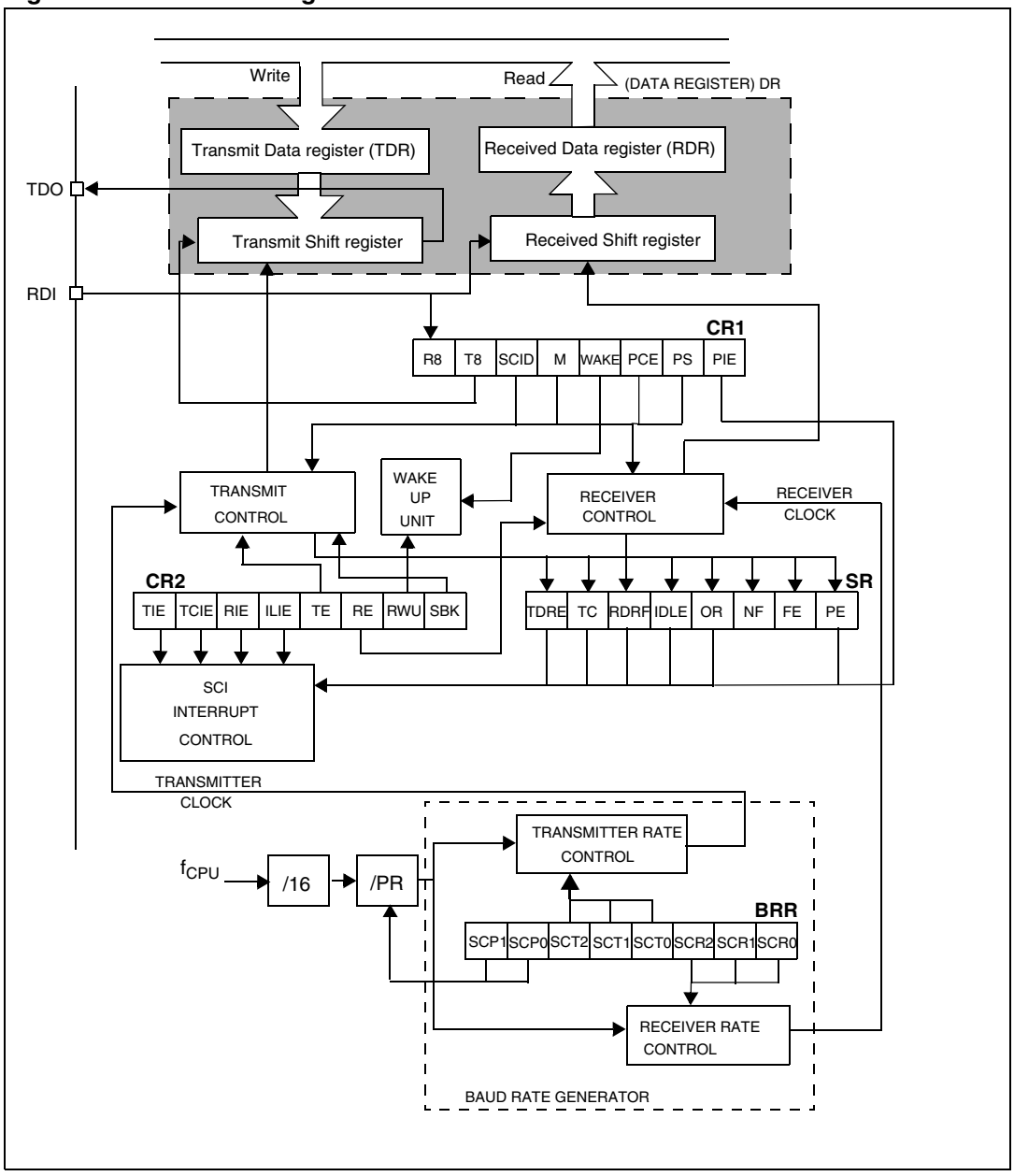
Through these pins, serial data is transmitted and received as frames comprising:

- An Idle Line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- A Stop bit indicating that the frame is complete.

This interface uses two types of baud rate generator:

- A conventional type for commonly-used baud rates.

Figure 41. SCI block diagram



Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see *Figure 41*).

Procedure

1. Select the M bit to define the word length.
2. Select the desired baud rate using the SCIBRR and the SCIETPR registers.
3. Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.
4. Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CC register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit or after the break frame) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CC register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see *Figure 42*).

Parity control

Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the frame length defined by the M bit, the possible SCI frame formats are as listed in *Table 26*.

Table 26. Frame formats(1)

M bit	PCE bit	SCI frame
0	0	ǀ SB ǀ 8 bit data ǀ STB ǀ
0	1	ǀ SB ǀ 7-bit data ǀ PB ǀ STB ǀ
1	0	ǀ SB ǀ 9-bit data ǀ STB ǀ
1	1	ǀ SB ǀ 8-bit data PB ǀ STB ǀ

1. SB = Start Bit, STB = Stop Bit, PB = Parity Bit

Note: In case of wakeup by an address mark, the MSB bit of the data is taken into account and not the parity bit

Even parity: the parity bit is calculated to obtain an even number of “1s” inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Ex: data=00110101; 4 bits set => parity bit will be 0 if even parity is selected (PS bit = 0).

Odd parity: the parity bit is calculated to obtain an odd number of “1s” inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Ex: data=00110101; 4 bits set => parity bit will be 1 if odd parity is selected (PS bit = 1).

Transmission mode: If the PCE bit is set then the MSB bit of the data written in the data register is not transmitted but is changed by the parity bit.

Reception mode: If the PCE bit is set then the interface checks if the received data byte has an even number of “1s” if even parity is selected (PS=0) or an odd number of “1s” if odd parity is selected (PS=1). If the parity check fails, the PE flag is set in the SCISR register and an interrupt is generated if PIE is set in the SCICR1 register.

SCI clock tolerance

During reception, each bit is sampled 16 times. The majority of the 8th, 9th and 10th samples is considered as the bit value. For a valid bit detection, all the three samples should have the same value otherwise the noise flag (NF) is set. For example: if the 8th, 9th and 10th samples are 0, 1 and 1 respectively, then the bit value will be “1”, but the Noise Flag bit is be set because the three samples values are not the same.

Consequently, the bit length must be long enough so that the 8th, 9th and 10th samples have the desired bit value. This means the clock frequency should not vary more than 6/16 (37.5%) within one bit. The sampling clock is resynchronized at each start bit, so that when receiving 10 bits (one start bit, 1 data byte, 1 stop bit), the clock deviation must not exceed 3.75%.

Note: The internal sampling clock of the microcontroller samples the pin value on every falling edge. Therefore, the internal sampling clock and the time the application expects the sampling to take place may be out of sync. For example: If the baud rate is 15.625 kbaud (bit length is 64µs), then the 8th, 9th and 10th samples will be at 28µs, 32 µs & 36 µs respectively (the first sample starting ideally at 0 µs). But if the falling edge of the internal

Interrupt Status register (ISTR)

Reset value: 0000 0000 (00h)

7							0
SUSP	DOVR	CTR	ERR	IOVR	ESUSP	RESET	SOF
Read.write							

When an interrupt occurs these bits are set by hardware. Software must read them to determine the interrupt type and clear them after servicing.

Note: These bits cannot be set by software.

7 **SUSP** *Suspend mode request*.
This bit is set by hardware when a constant idle state is present on the bus line for more than 3 ms, indicating a suspend mode request from the USB bus. The suspend request check is active immediately after each USB reset event and its disabled by hardware when suspend mode is forced (FSUSP bit of CTLR register) until the end of resume sequence.

6 **DOVR** *DMA over/underrun*.
This bit is set by hardware if the ST7 processor can't answer a DMA request in time.
0: No over/underrun detected
1: Over/underrun detected

5 **CTR** *Correct Transfer.* This bit is set by hardware when a correct transfer operation is performed. The type of transfer can be determined by looking at bits TP3-TP2 in register PIDR. The Endpoint on which the transfer was made is identified by bits EP1-EP0 in register IDR.
0: No Correct Transfer detected
1: Correct Transfer detected
Note: A transfer where the device sent a NAK or STALL handshake is considered not correct (the host only sends ACK handshakes). A transfer is considered correct if there are no errors in the PID and CRC fields, if the DATA0/DATA1 PID is sent as expected, if there were no data overruns, bit stuffing or framing errors.

4 **ERR** *Error.*
This bit is set by hardware whenever one of the errors listed below has occurred:
0: No error detected
1: Timeout, CRC, bit stuffing or nonstandard framing error detected

3 **IOVR** *Interrupt overrun.*
This bit is set when hardware tries to set ERR, or SOF before they have been cleared by software.
0: No overrun detected
1: Overrun detected

Figure 48. Transfer sequencing

Table 37. Slave receiver

S	Address	A		Data1	A		Data2	A		DataN	A		P	
			EV 1			EV 2			EV 2			EV 2		EV 4

.....

Table 38. Slave Transmitter

S	Address	A			Data1	A		Data2	A		DataN	NA		P	
			EV 1	EV 3			EV 3			EV 3			EV3 -1		EV 4

.....

Table 39. Master receiver

S		Address	A		Data1	A		Data2	A		DataN	NA		P
	EV 5			EV 6			EV 7			EV 7			EV 7	

.....

Table 40. Master Transmitter

S		Address	A			Data1	A		Data2	A		DataN	A		P
	EV 5			EV 6	EV 8			EV 8			EV 8			EV 8	

.....

1. Legend:
   S=Start, P=Stop, A=Acknowledge, NA=Non-acknowledge
   EVx=Event (with interrupt if ITE=1)**EV1:** EVF=1, ADSL=1, cleared by reading the SR1 register.

EV2: EVF=1, BTF=1, cleared by reading the SR1 register followed by reading the DR register.

EV3: EVF=1, BTF=1, cleared by reading the SR1 register followed by writing the DR register.

EV3-1: EVF=1, AF=1, BTF=1; AF is cleared by reading the SR1 register. The BTF is cleared by releasing the lines (STOP=1, STOP=0) or by writing the DR register (DR=FFh).
Note: If lines are released by STOP=1, STOP=0, the subsequent EV4 is not seen.

EV4: EVF=1, STOPF=1, cleared by reading the SR2 register.

EV5: EVF=1, SB=1, cleared by reading the SR1 register followed by writing the DR register.

EV6: EVF=1, cleared by reading the SR1 register followed by writing the CR register (for example PE=1).

EV7: EVF=1, BTF=1, cleared by reading the SR1 register followed by reading the DR register.

EV8: EVF=1, BTF=1, cleared by reading the SR1 register followed by writing the DR register.

Table 48. ST7 addressing mode overview (continued)

Mode			Syntax	Destination/ source	Pointer address	Pointer size (Hex.)	Length (bytes)
Long	Indirect		ld A,[$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC-128/PC+127(1)			+ 1
Relative	Indirect		jrne [$10]	PC-128/PC+127(1)	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

1. At the time the instruction is executed, the Program Counter (PC) points to the instruction following JRxx.

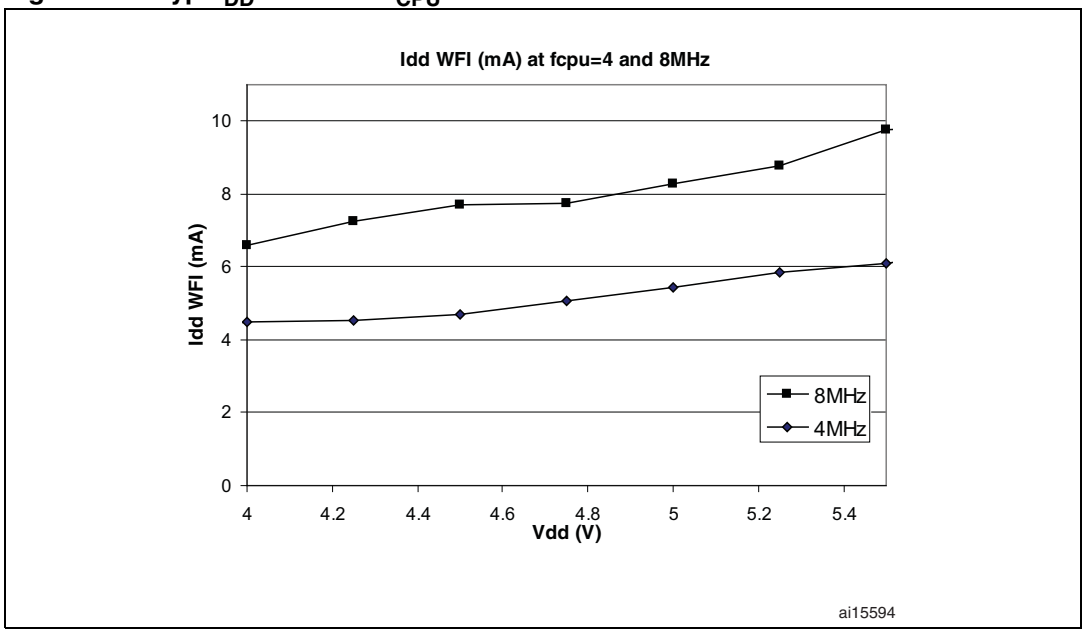
12.1.1 Inherent

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Table 49. Inherent instructions

Inherent instruction	Function
NOP	No operation
TRAP	S/W interrupt
WFI	Wait For Interrupt (Low Power mode)
HALT	Halt Oscillator (Lowest Power mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero

Figure 56. Typ. I_{DD} in Wait at f_{CPU}= 4 and 8 MHz



13.5 Clock and timing characteristics

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A.

Table 61. General timings

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
$t_{c(INST)}$	Instruction cycle time	f_{CPU}=8 MHz	2	3	12	t_{CPU}
			250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time(2) $t_{v(IT)} = \Delta t_{c(INST)} + 10\ t_{CPU}$	f_{CPU}=8 MHz	10	-	22	t_{CPU}
			1.25	-	2.75	µs

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

Table 62. Control timing characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ.	Max	
f_{OSC}	Oscillator frequency		-	-	24	MHz
f_{CPU}	Operating frequency		-	-	8	MHz
t_{RL}	External reset input pulse width		2520	-	-	ns
t_{PORL}	Internal power reset duration		4096	-	-	t_{CPU}
t_{WDGL}	Watchdog or low voltage reset output pulse width		200	300	-	ns

Figure 70. $|V_{DD}-V_{OH}|$ @ V_{DD}=5 V (high current)

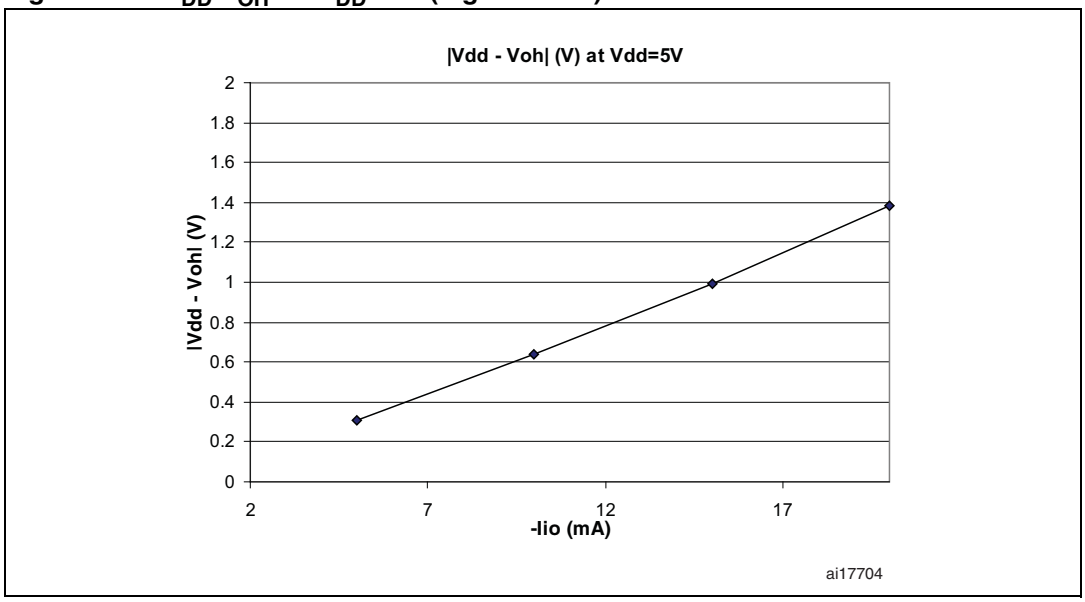


Figure 71. $|V_{DD}-V_{OH}|$ @ I_{IO}=2 mA (low current)

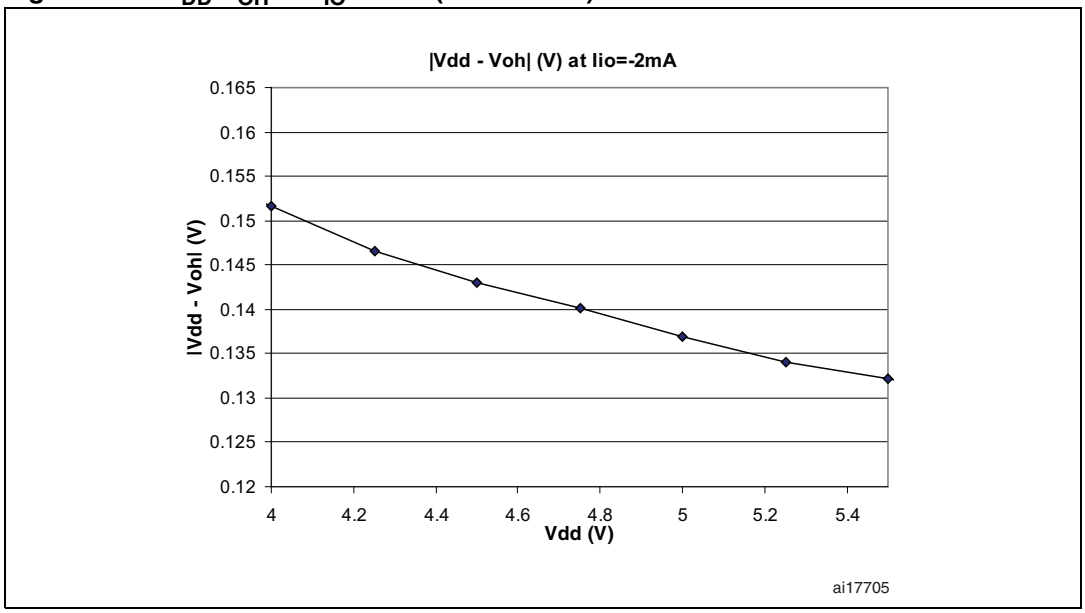
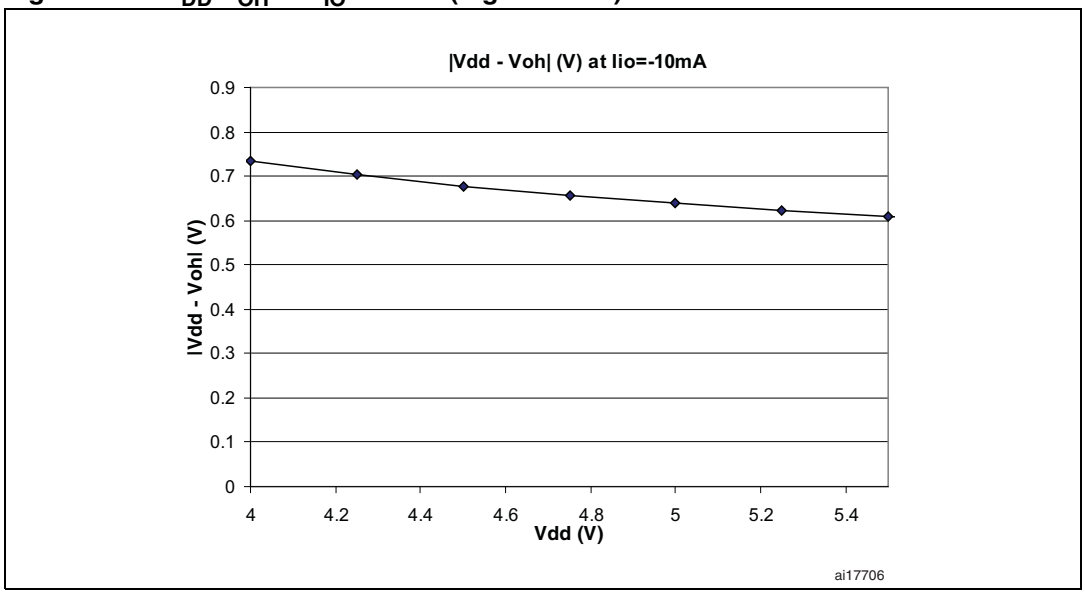


Figure 72. $|V_{DD}-V_{OH}|$ @ I_{IO}=10 mA (high current)



13.9 Control pin characteristics

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 72. Asynchronous $\overline{\text{RESET}}$ pin

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	Input high level voltage			0.7xV_{DD}	-	V_{DD}	V
V_{IL}	Input low voltage			V_{SS}	-	0.3xV_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis(1)			-	400	-	mV
V_{OL}	Output low level voltage(2)	V_{DD}=5 V	I_{IO}=5 mA	-	-	0.8	V
			I_{IO}=7.5 mA	-	-	1.3	
R_{ON}	Weak pull-up equivalent resistor (3)	V_{IN}=V_{SS}	V_{DD}=5 V	50	80	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources		-	6 30	-	1/f_{SFOSC} µs
$t_{h(RSTL)in}$	External reset pulse hold time(4)			5	-	-	µs

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
2. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 13.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.
4. To guarantee the reset of the device, a minimum pulse has to be applied to $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

Table 77 gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Table 77. SCL frequency(1)(2)(3)(4)

f_{SCL} (kHz)	I2CCCR Value							
	f_{CPU}=4 MHz				f_{CPU}=8 MHz			
	V_{DD} = 4.1 V		V_{DD} = 5 V		V_{DD} = 4.1 V		V_{DD} = 5 V	
	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ
400	NA	NA	NA	NA	83h	83	83h	83h
300	NA	NA	NA	NA	85h	85h	85h	85h
200	83h	83h	83h	83h	8Ah	89h	8Ah	8Ah
100	10h	10h	10h	10h	24h	23h	24h	23h
50	24h	24h	24h	24h	4Ch	4Ch	4Ch	4Ch
20	5Fh	5Fh	5Fh	5Fh	FFh	FFh	FFh	FFh

1. Legend: R_P = External pull-up resistance; f_{SCL} = I^2C speed; NA = not achievable.
2. The above variations depend on the accuracy of the external components used.
3. For speeds around 200 kHz, achieved speed can have ±5% tolerance.
4. For other speed ranges, achieved speed can have ±2% tolerance.

13.11 8-bit ADC

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 78. 8-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		-	-	4	MHz
V_{AIN}	Conversion range voltage(2)		V_{SSA}	-	V_{DDA}	V
R_{AIN}	External input resistor		-	-	10(3)	κΩ
C_{ADC}	Internal sample and hold capacitor		-	6	-	pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8 MHz, f_{ADC}=2 MHz	0(4)			µs
t_{ADC}	Conversion time (Sample+Hold)		6			
	- Sample capacitor loading time - Hold conversion time		4 8			$1/f_{ADC}$

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V.
2. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refer to V_{DD} and V_{SS}.
3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
4. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.