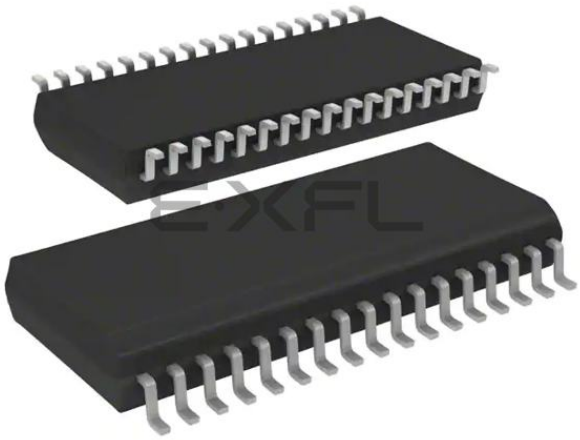


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

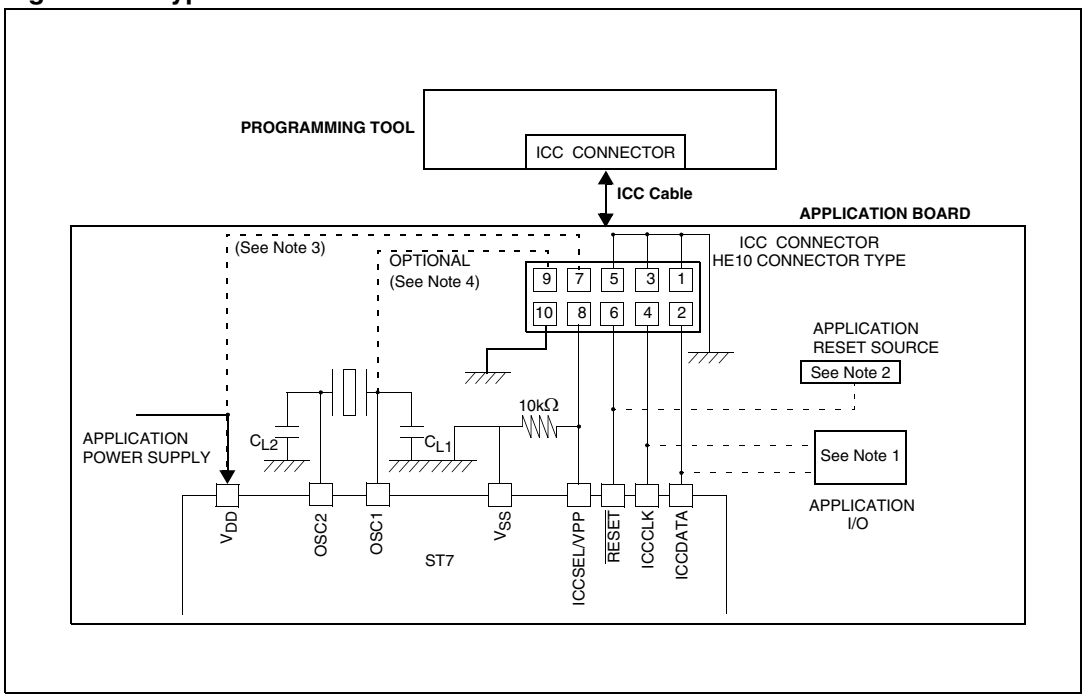
Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	34-BSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63bk1m1

11.2.1 Introduction . . . 58
11.2.2 Main features . . . 58
11.2.3 Functional description . . . 59
11.2.4 Low power modes . . . 72
11.2.5 Interrupts . . . 72
11.2.6 Summary of timer modes . . . 72
11.2.7 Register description . . . 73
11.3 Serial communications interface (SCI) . . . 80
11.3.1 Introduction . . . 80
11.3.2 Main features . . . 80
11.3.3 General description . . . 80
11.3.4 Functional description . . . 82
11.3.5 Low power modes . . . 89
11.3.6 Interrupts . . . 89
11.3.7 Register description . . . 90
11.4 USB interface (USB) . . . 97
11.4.1 Introduction . . . 97
11.4.2 Main features . . . 97
11.4.3 Functional description . . . 97
11.4.4 Register description . . . 98
11.4.5 Programming considerations . . . 106
11.5 I²C bus interface . . . 109
11.5.1 Introduction . . . 109
11.5.2 Main features . . . 109
11.5.3 General description . . . 109
11.5.4 Functional description . . . 111
11.5.5 Low power modes . . . 116
11.5.6 Interrupts . . . 116
11.5.7 Register description . . . 117
11.6 8-bit A/D converter (ADC) . . . 125
11.6.1 Introduction . . . 125
11.6.2 Main features . . . 125
11.6.3 Functional description . . . 125
11.6.4 Low power modes . . . 127
11.6.5 Interrupts . . . 128
11.6.6 Register description . . . 128

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32) (continued)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
15	16	23	29	PB2/AIN2	I/O	CT	10mA	X			X		X	Port B2	ADC analog input 2
16	17	24	30	PB1/AIN1	I/O	CT	10mA	X			X		X	Port B1	ADC analog input 1
17	18	25	31	PB0/AIN0	I/O	CT	10mA	X			X		X	Port B0	ADC analog input 0
18	19	26	32	PA7/OCMP2/IT4	I/O	CT			X	X			X	Port A7	Timer output Compare 2
19	20	27	33	PA6/OCMP1/IT3	I/O	CT			X	X			X	Port A6	Timer output Compare 1
20	21	28	34	PA5/ICAP2/IT2	I/O	CT			X	X			X	Port A5	Timer input Capture 2
21	22	29	35	PA4/ICAP1/IT1	I/O	CT			X	X			X	Port A4	Timer input Capture 1
22	23	30	36	PA3/EXTCLK	I/O	CT			X				X	Port A3	Timer External clock
23	24	31	38	PA2/SCL/ICCCLK	I/O	C_T	25mA	X				T		Port A2	I²C serial clock, ICC clock
-	-	32	39	PD0(1)/AIN8	I/O	C_T		X			X		X	Port D0	ADC analog input 8
-	-	33	40	PD1(1)/AIN9	I/O	C_T		X			X		X	Port D1	ADC analog input 9
-	-	34	41	PD2(1)/AIN10	I/O	C_T		X			X		X	Port D2	ADC analog input 10
-	-	35	42	PD3(1)/AIN11	I/O	C_T		X			X		X	Port D3	ADC analog input 11
-	-	36	43	PD4(1)	I/O	C_T			X				X	Port D4	
-	-	37	44	PD5(1)	I/O	C_T			X				X	Port D5	
-	-	38	45	PD6(1)	I/O	C_T			X				X	Port D6	
-	-	39	46	PD7(1)	I/O	C_T			X				X	Port D7	
-	25	-	-	NC	--									Not connected	
24	26	-	-	NC	--									Not connected	
25	27	-	-	NC	--									Not connected	
26	28	40	47	PA1/SDA/ICCDATA	I/O	CT	25mA	X				T		Port A1	I²C serial data, ICC data
27	29	1	48	PA0/MCO	I/O	CT				X			X	Port A0	Main clock output
28	30	2	1	V_{SSA}	S									Analog ground	
29	31	3	2	USBDP	I/O									USB bidirectional data (data +)	
30	32	4	3	USBDM	I/O									USB bidirectional data (data -)	

Figure 9. Typical ICC interface



1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.
2. During the ICC session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R > 1K or a reset management IC with open drain output and pull-up resistor > 1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.
3. The use of Pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.
4. Pin 9 has to be connected to the OSC1 or OSCIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

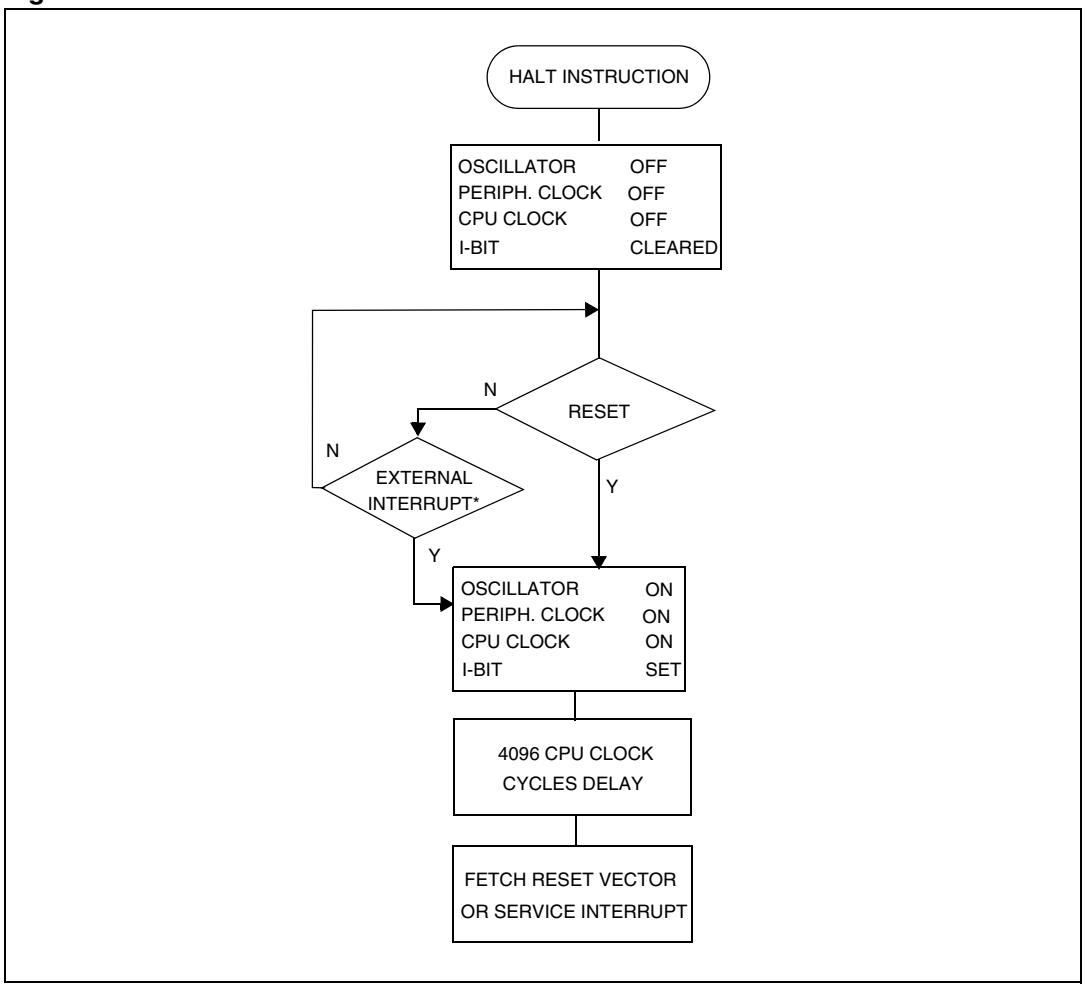
4.5 ICP (in-circuit programming)

To perform ICP the microcontroller must be switched to ICC (in-circuit communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see *Figure 9*). For more details on the pin locations, refer to the device pinout description.

Figure 20. Halt mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I-Bit is set during the interrupt routine and cleared when the CC register is popped.

8.3 Slow mode

In Slow mode, the oscillator frequency can be divided by 2 as selected by the SMS bit in the Miscellaneous register. The CPU and peripherals are clocked at this lower frequency. Slow mode is used to reduce power consumption, and enables the user to adapt the clock frequency to the available supply voltage.

8.4 Wait mode

Wait mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the “WFI” ST7 software instruction.

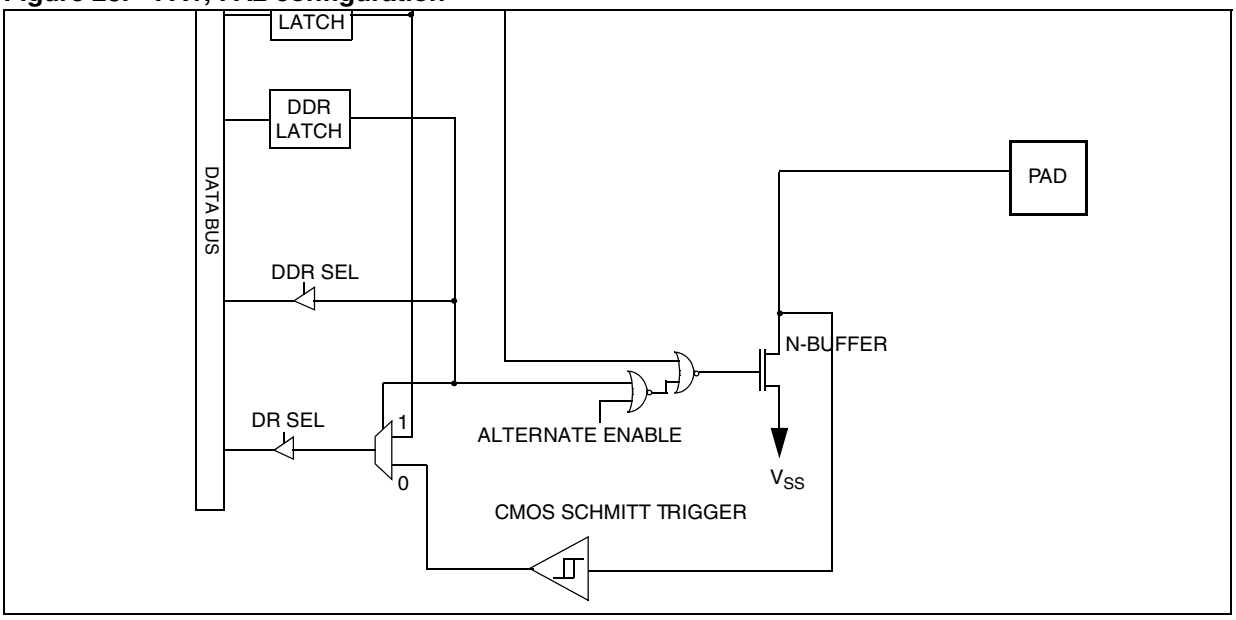
All peripherals remain active. During Wait mode, the I bit of the CC register is forced to 0 to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in Wait mode until an interrupt or Reset occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.

Table 12. PA1, PA2 description(1)

Port A	I / O		Alternate function	
	Input[1]	Output	Signal	Condition
PA1	without pull-up	Very high current open drain	SDA (I²C data)	I²C enable
PA2	without pull-up	Very high current open drain	SCL (I²C clock)	I²C enable

1. Reset state.

Figure 23. PA1, PA2 configuration



11.1.8 Register description

Control register (CR)

Reset value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0
Read/write							

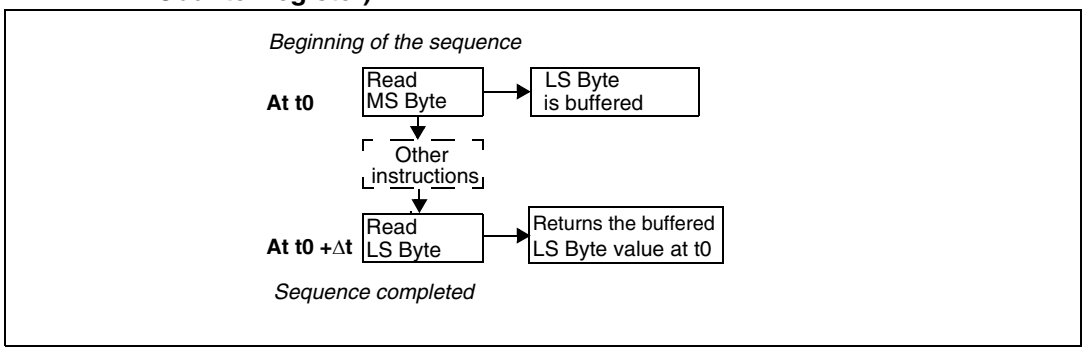
7 **WDGA** *Activation bit.*
This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.
0: Watchdog disabled
1: Watchdog enabled

[6:0] **T[6:0]** *7-bit timer (MSB to LSB).*
These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared).

Table 18. Watchdog timer register map and reset values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0Ch	WDGCR	WDGA	T6	T5	T4	T3	T2	T1	T0
	Reset value	0	1	1	1	1	1	1	1

Figure 28. 16-bit read sequence (from either the Counter register or the Alternate Counter register)



The user must read the MS Byte first, then the LS Byte value is buffered automatically.

This buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MS Byte several times.

After a complete reading sequence, if only the CLR register or ACLR register are read, they return the LS Byte of the count value at the time of the read.

Whatever the timer mode used (input capture, output compare, One Pulse mode or PWM mode) an overflow occurs when the counter rolls over from FFFFh to 0000h then:

- The TOF bit of the SR register is set.
- A timer interrupt is generated if:
  - TOIE bit of the CR1 register is set and
  - I bit of the CC register is cleared.

If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true.

Clearing the overflow interrupt request is done in two steps:

1. Reading the SR register while the TOF bit is set.
2. An access (read or write) to the CLR register.

Note: The TOF bit is not cleared by accesses to ACLR register. The advantage of accessing the ACLR register rather than the CLR register is that it allows simultaneous use of the overflow function and reading the free running counter at random times (for example, to measure elapsed time) without the risk of clearing the TOF bit erroneously.

The timer is not affected by Wait mode.

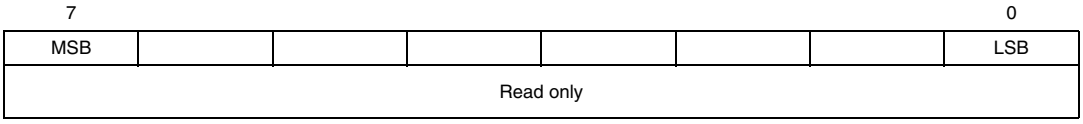
In Halt mode, the counter stops counting until the mode is exited. Counting then resumes from the previous count (MCU awakened by an interrupt) or from the reset count (MCU awakened by a Reset).

External clock

The external clock (where available) is selected if CC0 = 1 and CC1 = 1 in the CR2 register.

The status of the EXEDG bit in the CR2 register determines the type of level transition on the external clock pin EXTCLK that will trigger the free running counter.

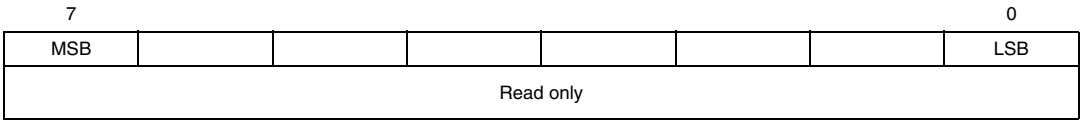
The counter is synchronized with the falling edge of the internal CPU clock.



Alternate Counter Low register (ACLR)

Reset value: 1111 1100 (FCh)

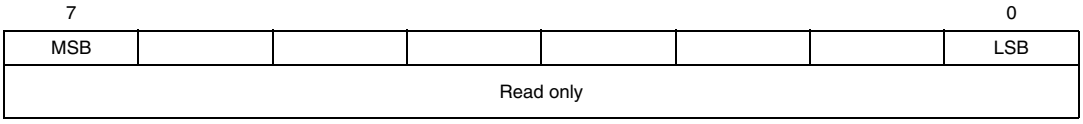
This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to CSR register does not clear the TOF bit in the CSR register.



Input Capture 2 High register (IC2HR)

Reset value: Undefined

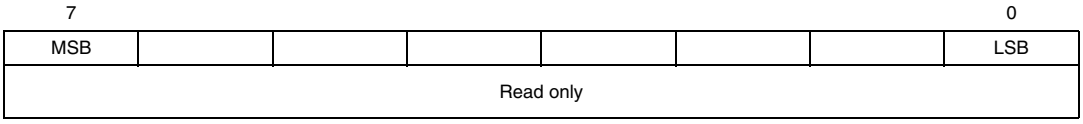
This is an 8-bit read only register that contains the high part of the counter value (transferred by the input Capture 2 event).



Input Capture 2 Low register (IC2LR)

Reset value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input Capture 2 event).



11.3.4 Functional description

The block diagram of the Serial Control Interface, is shown in *Figure 41* It contains 6 dedicated registers:

- Two control registers (SCICR1 & SCICR2)
- A status register (SCISR)
- A baud rate register (SCIBRR)

Refer to the register descriptions in *Section 11.3.7* for the definitions of each bit.

Serial data format

Word length may be selected as being either 8 or 9 bits by programming the M bit in the SCICR1 register (see *Figure 41*).

The TDO pin is in low state during the start bit.

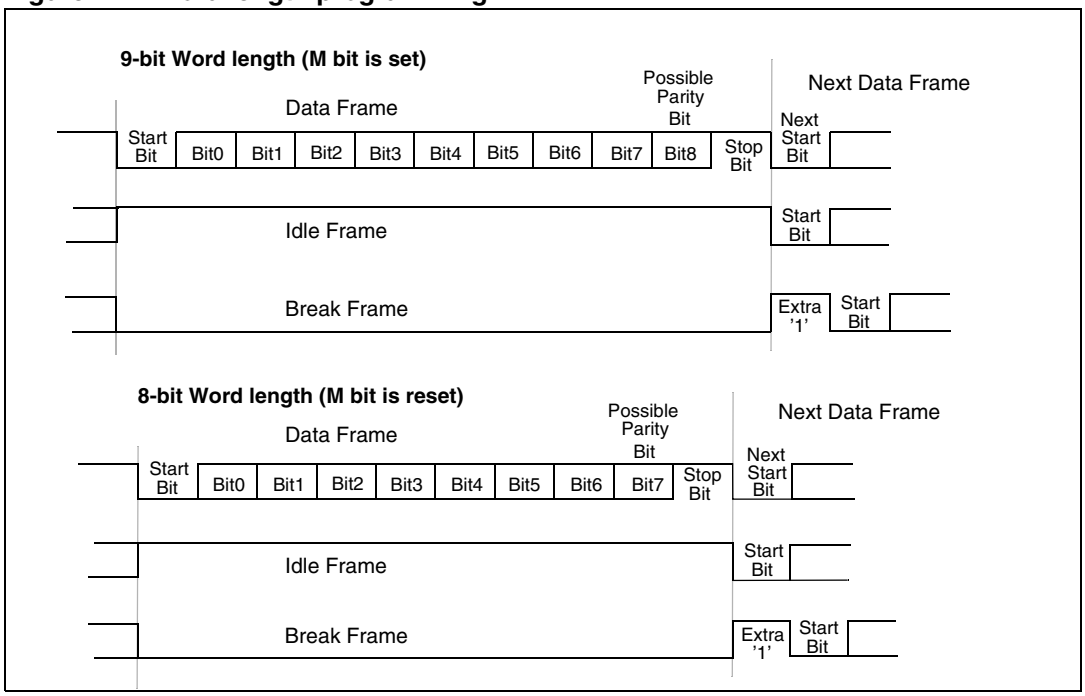
The TDO pin is in high state during the stop bit.

An Idle character is interpreted as an entire frame of “1”s followed by the start bit of the next frame which contains data.

A Break character is interpreted on receiving “0”s for some multiple of the frame period. At the end of the last break frame the transmitter inserts an extra “1” bit to acknowledge the start bit.

Transmission and reception are driven by their own baud rate generator.

Figure 42. Word length programming



As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set i.e. before writing the next byte in the SCIDR.

Receiver

The SCI can receive data words of either 8 or 9 bits. When the M bit is set, word length is 9 bits and the MSB is stored in the R8 bit in the SCICR1 register.

Character reception

During a SCI reception, data shifts in least significant bit first through the RDI pin. In this mode, the SCIDR register consists or a buffer (RDR) between the internal bus and the received shift register (see *Figure 41*).

Procedure

1. Select the M bit to define the word length.
2. Select the desired baud rate using the SCIBRR and the SCIERPR registers.
3. Set the RE bit, this enables the receiver which begins searching for a start bit.

When a character is received:

- The RDRF bit is set. It indicates that the content of the shift register is transferred to the RDR.
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CC register.
- The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

Clearing the RDRF bit is performed by the following software sequence done by:

1. An access to the SCISR register
2. A read to the SCIDR register.

The RDRF bit must be cleared before the end of the reception of the next character to avoid an overrun error.

Break character

When a break character is received, the SCI handles it as a framing error.

Idle character

When a idle frame is detected, there is the same procedure as a data received character plus an interrupt if the ILIE bit is set and the I bit is cleared in the CC register.

Overrun error

An overrun error occurs when a character is received when RDRF has not been reset. Data can not be transferred from the shift register to the RDR register as long as the RDRF bit is not cleared.

Baud rate generation

The baud rate for the receiver and transmitter (Rx and Tx) are set independently and calculated as follows:

$$Tx = \frac{f_{CPU}}{(16*PR)*TR} \qquad Rx = \frac{f_{CPU}}{(16*PR)*RR}$$

with:

PR = 1, 3, 4 or 13 (see SCP[1:0] bits)

TR = 1, 2, 4, 8, 16, 32, 64,128

(see SCT[2:0] bits)

RR = 1, 2, 4, 8, 16, 32, 64,128

(see SCR[2:0] bits)

All these bits are in the SCIBRR register.

Example: If f_{CPU} is 8 MHz (normal mode) and if PR=13 and TR=RR=1, the transmit and receive baud rates are 38400 baud.

Note: The baud rate registers MUST NOT be changed while the transmitter or the receiver is enabled.

Receiver muting and Wakeup feature

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non addressed receivers.

The non addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

All the reception status bits can not be set.

All the receive interrupts are inhibited.

A muted receiver may be awakened by one of the following two ways:

- By Idle Line detection if the WAKE bit is reset,
- By Address Mark detection if the WAKE bit is set.

Receiver wakes-up by Idle Line detection when the Receive line has recognized an Idle Frame. Then the RWU bit is reset by hardware but the IDLE bit is not set.

Receiver wakes-up by Address Mark detection when it received a “1” as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

Caution: In Mute mode, do not write to the SCICR2 register. If the SCI is in Mute mode during the read operation (RWU=1) and a address mark wake up event occurs (RWU is reset) before the write operation, the RWU bit will be set again by this write operation. Consequently the address byte is lost and the SCI is not woken up from Mute mode.

Endpoint n register A (EPnRA)

These registers (EP0RA, EP1RA and EP2RA) are used for controlling data transmission. They are also reset by the USB bus reset.

Note: Endpoint 2 and the EP2RA register are not available on some devices (see device feature list and register map).

Reset value: 0000 xxxx (0xh)

7							0
ST_ OUT	DTOG _TX	STAT _TX1	STAT _TX0	TBC3	TBC2	TBC1	TBC0
Read.write							

7 **ST_OUT** *Status out.*
This bit is set by software to indicate that a status out packet is expected: in this case, all nonzero OUT data transfers on the endpoint are STALLed instead of being ACKed. When ST_OUT is reset, OUT transactions can have any number of bytes, as needed.

6 **DTOG_TX** *Data Toggle, for transmission transfers.*
It contains the required value of the toggle bit (0=DATA0, 1=DATA1) for the next transmitted data packet. This bit is set by hardware at the reception of a SETUP PID. DTOG_TX toggles only when the transmitter has received the ACK signal from the USB host. DTOG_TX and also DTOG_RX (see EPnRB) are normally updated by hardware, at the receipt of a relevant PID. They can be also written by software.

[5:4] **STAT_TX[1:0]** *Status bits, for transmission transfers.*
These bits contain the information about the endpoint status, which are listed in *Table 34*.

These bits are written by software. Hardware sets the STAT_TX bits to NAK when a correct transfer has occurred (CTR=1) related to a IN or SETUP transaction addressed to this endpoint; this allows the software to prepare the next set of data to be transmitted.

[3:0] **TBC[3:0]** *Transmit byte count for Endpoint n.*
Before transmission, after filling the transmit buffer, software must write in the TBC field the transmit packet size expressed in bytes (in the range 0-8).

Caution: Any value outside the range 0-8 willinduce undesired effects (such as continuous data transmission).

Table 34. STAT_TX bit definition

STAT_TX1	STAT_TX0	Meaning
0	0	**DISABLED:** transmission transfers cannot be executed.
0	1	**STALL**: the endpoint is stalled and all transmission requests result in a STALL handshake.
1	0	**NAK**: the endpoint is naked and all transmission requests result in a NAK handshake.
1	1	**VALID**: this endpoint is enabled for transmission.

11.5 I²C bus interface

11.5.1 Introduction

The I²C bus interface serves as an interface between the microcontroller and the serial I²C bus. It provides both multimaster and slave functions, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It supports fast I²C mode (400 kHz).

11.5.2 Main features

- Parallel-bus/I²C protocol converter
- Multimaster capability
- 7-bit addressing
- Transmitter/receiver flag
- End-of-byte transmission flag
- Transfer problem detection

I²C master features

- Clock generation
- I²C bus busy flag
- Arbitration Lost Flag
- End of byte transmission flag
- Transmitter/Receiver Flag
- Start bit detection flag
- Start and Stop generation

I²C slave features

- Stop bit detection
- I²C bus busy flag
- Detection of misplaced start or stop condition
- Programmable I²C Address detection
- Transfer problem detection
- End-of-byte transmission flag
- Transmitter/Receiver flag

11.5.3 General description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa, using either an interrupt or polled handshake. The interrupts are enabled or disabled by software. The interface is connected to the I²C bus by a data pin (SDAI) and by a clock pin (SCLI). It can be connected both with a standard I²C bus and a Fast I²C bus. This selection is made by software.

Following the address reception and after SR1 register has been read, the slave receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set
- EVF and BTF bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see *Figure 48* Transfer sequencing EV2).

Slave transmitter

Following the address reception and after the SR1 register has been read, the slave sends bytes from the DR register to the SDA line via the internal shift register.

The slave waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see *Figure 48* Transfer sequencing EV3).

When the acknowledge pulse is received, the EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

Closing Slave communication

After the last data byte is transferred a Stop Condition is generated by the master. The interface detects this condition and sets EVF and STOPF bits with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR2 register (see *Figure 48* Transfer sequencing EV4).

Error cases

- **BERR**: Detection of a Stop or a Start condition during a byte transfer. In this case, the EVF and the BERR bits are set with an interrupt if the ITE bit is set.
  If it is a Stop, then the interface discards the data, released the lines and waits for another Start condition.
  If it is a Start, then the interface discards the data and waits for the next slave address on the bus.
- **AF**: Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set with an interrupt if the ITE bit is set.
  The AF bit is cleared by reading the I2CSR2 register. However, if read before the completion of the transmission, the AF flag will be set again, thus possibly generating a new interrupt. Software must ensure either that the SCL line is back at 0 before reading the SR2 register, or be able to correctly handle a second interrupt during the 9th pulse of a transmitted byte.

Note: In case of errors, SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. While AF=1, the SCL line may be held low due to SB or BTF flags that are set at the same time. It is then necessary to release both lines by software.

How to Release the SDA / SCL lines

Set and subsequently clear the STOP bit while BTF is set. The SDA/SCL lines are released after the transfer of the current byte.

Master mode

To switch from default Slave mode to Master mode, a Start condition generation is needed.

Start condition

Table 43. I²C register map

Address (Hex.)	Register name	7	6	5	4	3	2	1	0
39	DR	DR7 .. DR0							
3B	OAR	ADD7 .. ADD0							
3C	CCR	FM/SM	CC6 .. CC0						
3D	SR2				AF	STOPF	ARLO	BERR	GCAL
3E	SR1	EVF		TRA	BUSY	BTF	ADSL	M/SL	SB
3F	CR			PE	ENGC	START	ACK	STOP	ITE

Note: Refer to Section 16: Known limitations for information regarding a limitation on the alternate function on pin PA2 (SCL).

Table 62. Control timing characteristics

t_{WDG}	Watchdog timeout	f_{CPU} = 8MHz	49152	-	3145728	t_{CPU}
			6.144	-	393.216	ms
t_{OXOV}	Crystal oscillator startup time		20(1)	30	40(1)	ms
t_{DDR}	Power up rise time	from V_{DD} = 0 to 4 V	-	-	100(1)	ms

1. Not tested in production, guaranteed by characterization.

Table 63. External clock source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSCINH}	OSCIN input pin high level voltage	see *Figure 57*	0.7xV_{DD}	-	V_{DD}	V
V_{OSCINL}	OSCIN input pin low level voltage		V_{SS}	-	0.3xV_{DD}	
$t_{w(OSCINH)}$ $t_{w(OSCINL)}$	OSCIN high or low time(1)		15	-	-	ns
$t_{r(OSCIN)}$ $t_{f(OSCIN)}$	OSCIN rise or fall time(1)		-	-	15	
I_L	OSCx input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 57. Typical application with an external clock source

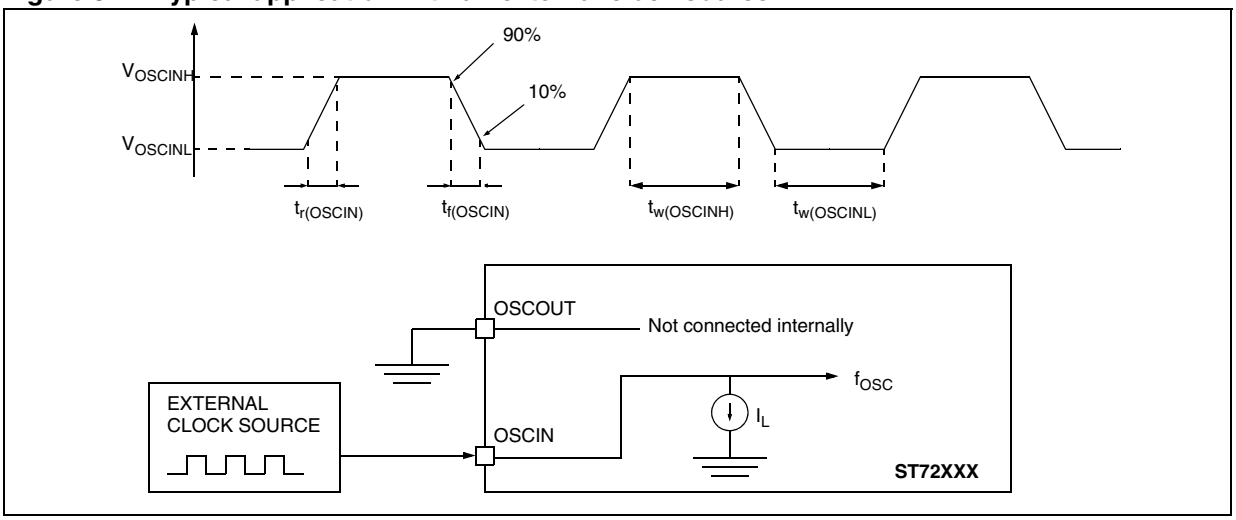


Table 69. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latchup class	T_A=+25 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

13.8 I/O port pin characteristics

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 70. General characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage			-	-	0.3xV_{DD}	V
V_{IH}	Input high level voltage			0.7xV_{DD}	-	-	
V_{IN}	Input voltage	True open drain I/O pins		V_{SS}	-	6.0	V
		Other I/O pins			-	V_{DD}	
V_{hys}	Schmitt trigger voltage hysteresis			-	400	-	mV
I_L	Input leakage current	V_{SS}≤V_{IN}≤V_{DD}		-	-	±1	µA
I_S	Static current consumption induced by each floating input pin(1)	Floating input mode		-	400	-	
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN}=V_{SS}	V_{DD}=5 V	50	90	120	kΩ
C_{IO}	I/O pin capacitance			-	5	-	pF
$t_{f(IO)out}$	Output high to low level fall time	C_L=50pF Between 10% and 90%		-	25	-	ns
$t_{r(IO)out}$	Output low to high level rise time			-	25	-	
$t_{w(IT)in}$	External interrupt pulse time(3)			1	-	-	t_{CPU}

1. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 60*). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 61*).
3. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 60. Two typical applications with unused I/O pin

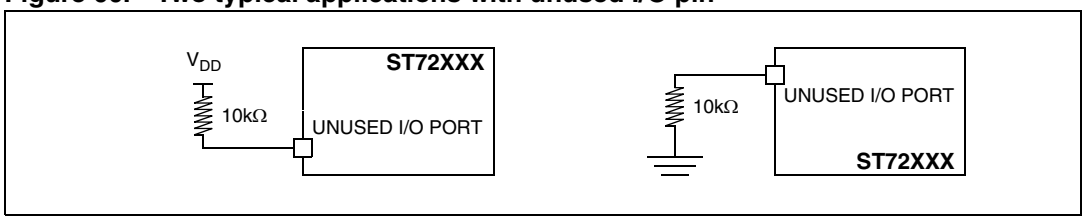


Figure 77. Typical application with ADC

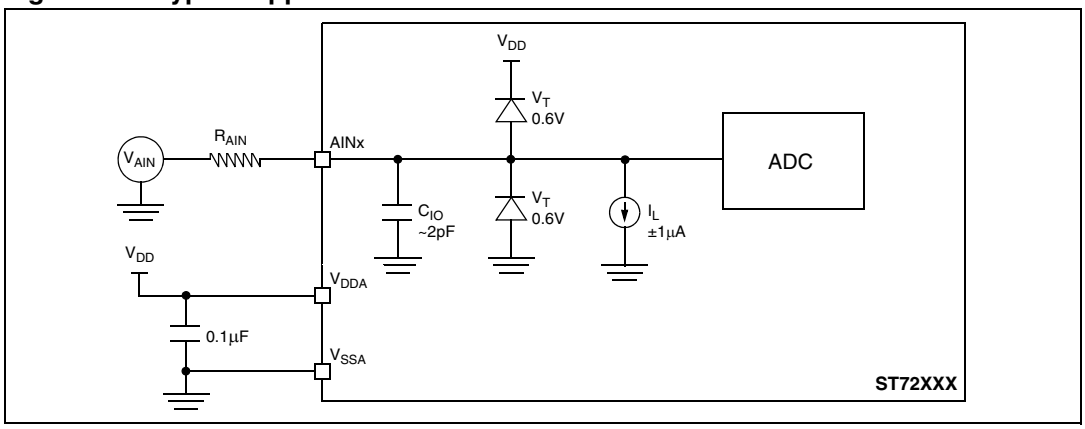


Table 79. ADC accuracy with V_{DD}=5 V, f_{CPU}= 8 MHz, f_{ADC}=4 MHz, R_{AIN}< 10 kΩ

Symbol	Parameter	Typ	Max(1)(2)
$\|E_T\|$	Total unadjusted error(3)	1.5	2
$\|E_{OI}\|$	Offset error(3)	0.5	1
$\|E_{GI}\|$	Gain Error(3)	0.5	1.5
$\|E_D\|$	Differential linearity error(3)	1	1.5
$\|E_L\|$	Integral linearity error(3)	1	1.5

1. Data based on characterization results over the whole temperature range, not tested in production.
2. Data based on characterization results, to guarantee 99.73% within ± max value from 0 to 70 °C (± 3s distribution limits).
3. ADC Accuracy vs. Negative Injection Current:
For I_{INJ-}=0.8mA, the typical leakage induced inside the die is 1.6µA and the effect on the ADC accuracy is a loss of 1 LSB for each 10KΩ increase of the external analog source impedance. This effect on the ADC accuracy has been observed under worst-case conditions for injection:
- negative injection
- injection to an input with analog capability, adjacent to the enabled Analog input
- at 5V V_{DD} supply, and worst case temperature.

Figure 82. 48-pin low profile quad flat package outline

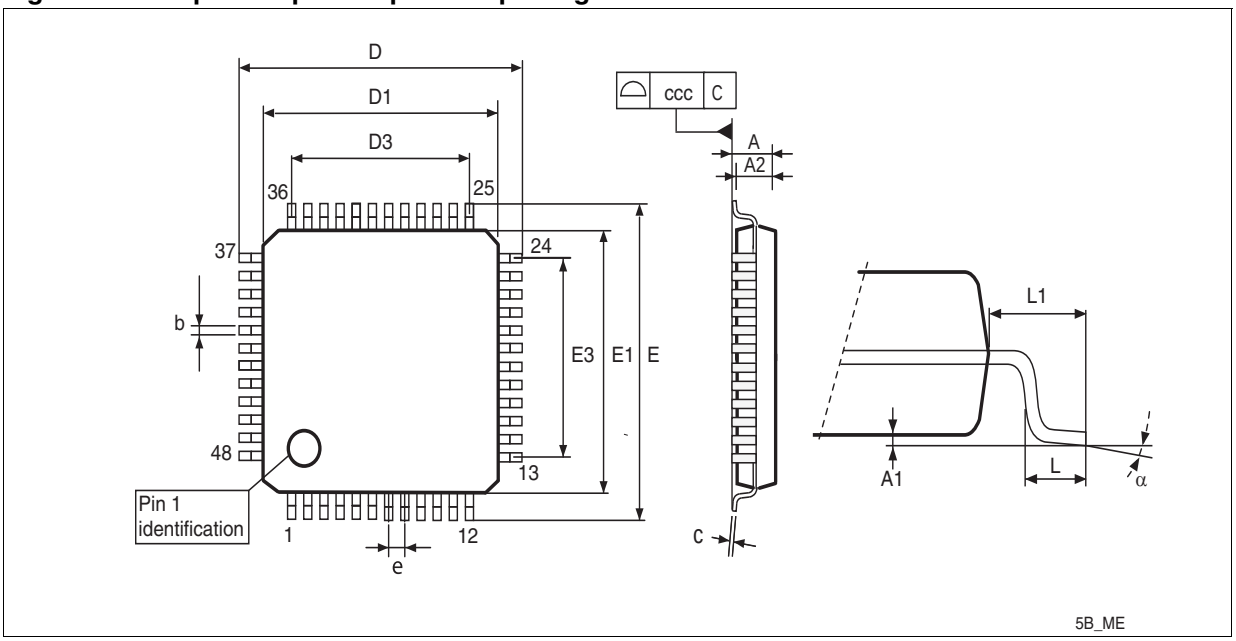


Table 83. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0060
A2	1.350	1.400	1.450	0.0530	0.0551	0.0570
b	0.170	0.220	0.270	0.0070	0.0087	0.0110
c	0.090		0.200	0.0040		0.0080
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
θ	0°	3.5°	7°	0°	3.5°	7°
ccc	0.080			0.0031		
	Number of pins					
N	48					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

17 Revision history

Table 89. Document revision history

Date	Revision	Changes
27-May-05	3	New revision created by merging 32K Flash and non-32K Flash datasheets together. Memory Map, *Figure 7*, expanded to handle all devices and memory sizes. Operating conditions with LVD values modified, *Section 13.3.1: Operating conditions with low voltage detector (LVD)*. Supply current characteristics values and notes updated, *Section 13.4: Supply current characteristics*. IDD Run and Wait graphs replaced, *Figure 55* and *Figure 56 on page 143*. Control timing characteristics modified, *Section Table 62.: Control timing characteristics*. Flash memory table notes and t_{PROG} typical value updated, *Section 13.6.1: Flash memory*. Notes added for I/O Port Pin Characteristics table, *Section Table 70.: General characteristics*. Note for R_{PU} modified, removing reference to data characterization, *Section Table 70*. I_{PU} and R_{PU} graphs added, *Figure 61* and *Figure 62 on page 150*. Notes updated for USB low speed electrical characteristics. Output voltage/current graphs added, Figures *Figure 63.*-*Figure 72.*Thermal Characteristics added for SO24 and TQFP48 packages, *Section 14.2: Thermal characteristics*. Important note added for OPT 3 Option Byte (LVD), *Section 15.1: Option byte*. Supported Part Numbers table updated with full sales type codes, *Table 86*. Option List updated with all device options. Important notes updated with 'USB behavior with LVD disabled', *Section 16.3: USB behavior with LVD disabled*. Clock block diagram redrawn, *Figure 18 on page 36*. DFU added to title and features list. Removed unnecessary notes related to Typical Values (already mentioned in *Section 13.1.2: Typical values*) in electrical characteristic tables sections: *Section 13.3.1*, *Section 13.4*, *Section 13.6.1*, *Section Table 70.*, *Section Table 72*. and *Section 13.11*. Added note for max values in ADC Accuracy, *Section 13.11*. Static Latch Up (LU) class tested only for T_A=25°C, *Section : Static latchup (LU)*
19-Sep-05	4	Flash memory minimum data retention increased to 40 years, *Section 13.6.1: Flash memory* AF bit text modified concerning SCL, I^2C chapter *Section 11.5.7: Register description* Reference made to the Flash Programming Reference Manual for Flash timing values Reset pulse generated by WDG changed to 30 µs, *Section 11.1: Watchdog timer (WDG)* Modified text in *Section 11.3: Serial communications interface (SCI)*, adding Parity error as an interrupt Added ECOPACK information in *Section 14: Package characteristics* Modified I_S value and corresponding note in *Section Table 70.: General characteristics*
06-Apr-06	5	32K and 8K QFN40 Packages added 4K SO24 Package added TQFP package renamed to LQFP