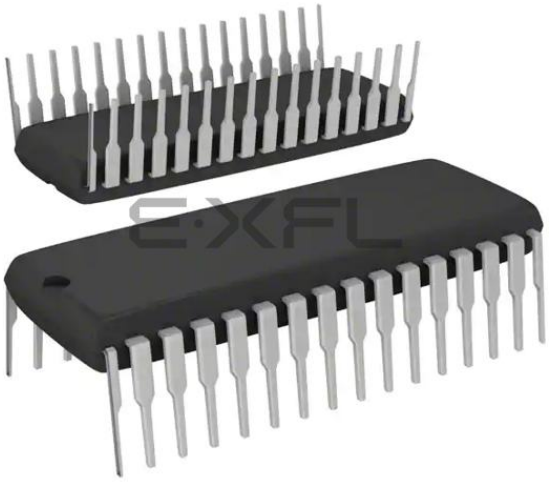

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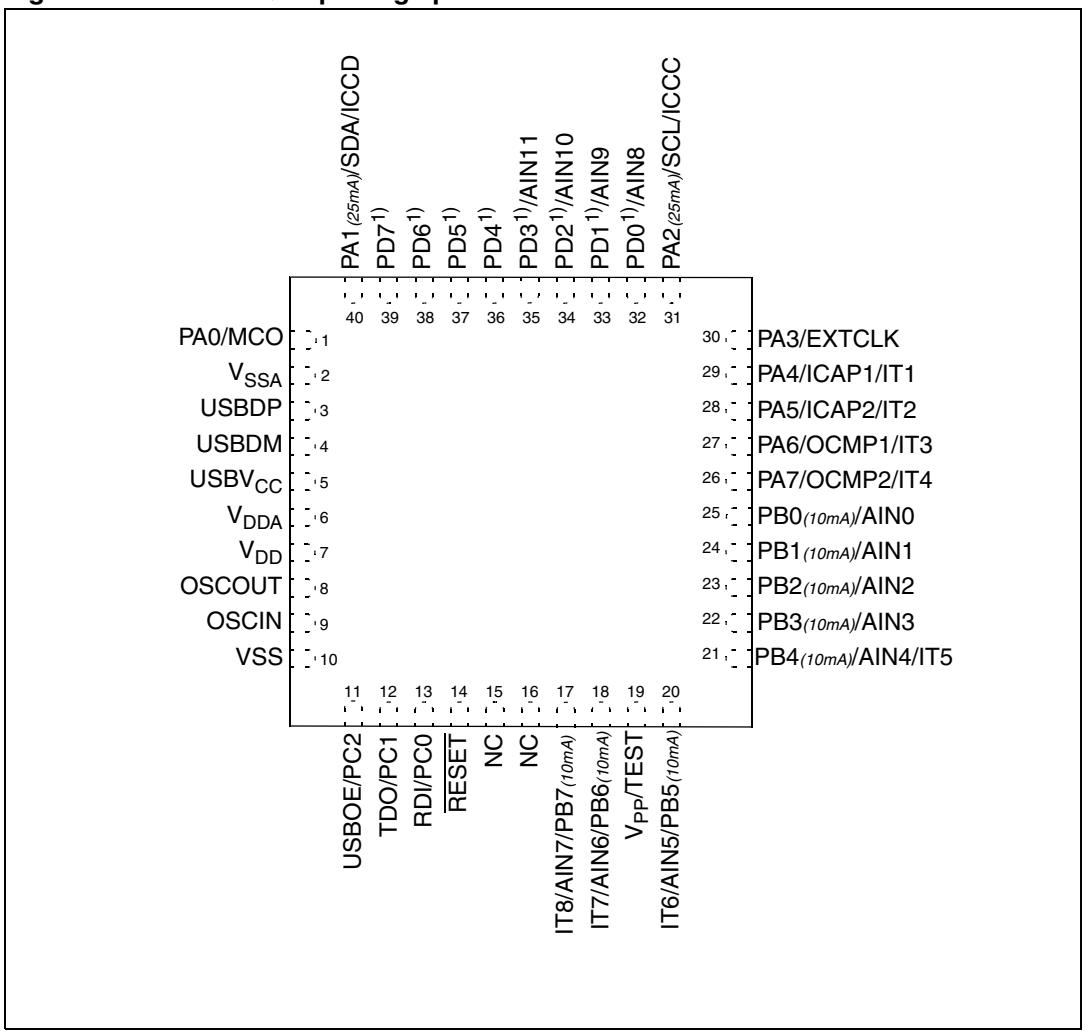
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63bk2b1

Figure 3. 40-lead QFN package pinout



1. Port D functions are not available on the 8 Kbyte version of the QFN40 package (ST7263BK2) and should not be connected.

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming). In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register access security system (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

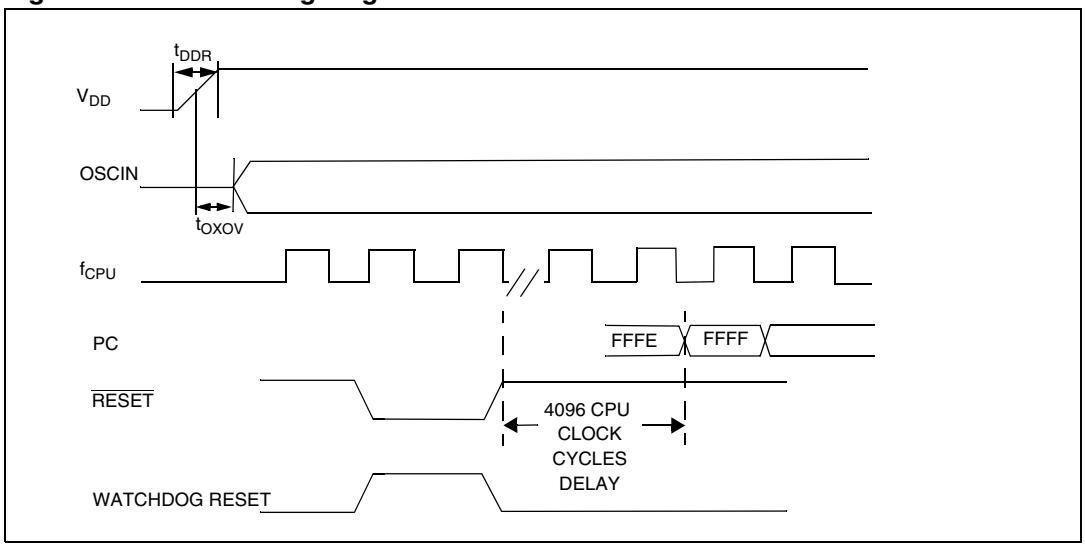
Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 7*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see *Figure 8*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 7. Sectors available in Flash devices

Flash size (Kbytes)	Available sectors
4	Sector 0
8	Sectors 0,1
> 8	Sectors 0,1, 2

Figure 15. Reset timing diagram



1. Refer to Electrical Characteristics for values of t_{DDR}, t_{OXOV}, V_{IT+}, V_{IT-} and V_{hys}

7 Interrupts

The ST7 core may be interrupted by one of two different methods: maskable hardware interrupts as listed in *Table 9* and a non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in *Figure 19*.

The maskable interrupts must be enabled clearing the I bit in order to be serviced. However, disabled interrupts may be latched and processed when they are enabled (see external interrupts subsection).

When an interrupt has to be serviced:

- Normal processing is suspended at the end of the current instruction execution.
- The PC, X, A and CC registers are saved onto the stack.
- The I bit of the CC register is set to prevent additional interrupts.
- The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to *Table 9* for vector addresses).

The interrupt service routine should finish with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

Note: As a consequence of the IRET instruction, the I bit will be cleared and the main program will resume.

Priority management

By default, a servicing interrupt cannot be interrupted because the I bit is set by hardware entering in interrupt routine.

In the case several interrupts are simultaneously pending, a hardware priority defines which one will be serviced first (see *Table 9*).

Non-maskable software interrupts

This interrupt is entered when the TRAP instruction is executed regardless of the state of the I bit. It will be serviced according to the flowchart on *Figure 19*.

Interrupts and low power mode

All interrupts allow the processor to leave the Wait low power mode. Only external and specific mentioned interrupts allow the processor to leave the Halt low power mode (refer to the “Exit from HALT“ column in *Table 9*).

External interrupts

The pins ITi/PAk and ITj/PBk (i=1,2; j= 5,6; k=4,5) can generate an interrupt when a rising edge occurs on this pin. Conversely, the ITl/PAn and ITm/PBn pins (l=3,4; m= 7,8; n=6,7) can generate an interrupt when a falling edge occurs on this pin.

Interrupt generation will occur if it is enabled with the ITiE bit (i=1 to 8) in the ITRFRE register and if the I bit of the CC is reset.

11.2.3 Functional description

Counter

The main block of the Programmable Timer is a 16-bit free running upcounter and its associated 16-bit registers. The 16-bit registers are made up of two 8-bit registers called high and low.

- Counter register (CR)

  Counter High register (CHR) is the most significant byte (MSB).

  Counter Low register (CLR) is the least significant byte (LSB).

- Alternate Counter register (ACR)

  Alternate Counter High register (ACHR) is the most significant byte (MSB).

  Alternate Counter Low register (ACLR) is the least significant byte (LSB).

These two read-only 16-bit registers contain the same value but with the difference that reading the ACLR register does not clear the TOF bit (Timer overflow flag), located in the Status register, (SR), (see note at the end of paragraph titled 16-bit read sequence).

Writing in the CLR register or ACLR register resets the free running counter to the FFFCh value.

Both counters have a reset value of FFFCh (this is the only value which is reloaded in the 16-bit timer). The reset value of both counters is also FFFCh in One Pulse mode and PWM mode.

The timer clock depends on the clock control bits of the CR2 register, as illustrated in *Table 24*. The value in the counter register repeats every 131072, 262144 or 524288 CPU clock cycles depending on the CC[1:0] bits.

The timer frequency can be $f_{CPU}/2$, $f_{CPU}/4$, $f_{CPU}/8$ or an external frequency.

Table 24. Clock Control bits

Timer clock	CC1	CC0
f_{CPU} / 4	0	0
f_{CPU} / 2		1
f_{CPU} / 8	1	0
External Clock (where available)		1

Control/status register (CSR)

Reset value: xxxx x0xx (xxh)

7	6	5	4	3			0
ICF1	OCF1	TOF	ICF2	OCF2	TIMD	0	0
Read only					Read/write		

7 **ICF1** *input Capture Flag 1.*

0: No input capture (reset value).

1: An input capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.

6 **OCF1** output *Compare Flag 1.*

0: No match (reset value).

1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.

5 **TOF** *Timer Overflow Flag.*

0: No timer overflow (reset value).

1:The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register.

Note: Reading or writing the ACLR register does not clear TOF.

4 **ICF2** *input Capture Flag 2.*

0: No input capture (reset value).

1: An input capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.

Table 25. 16-bit timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
11	CR2 Reset value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
12	CR1 Reset value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
13	CSR Reset value	ICF1 0	OCF1 0	TOF 0	ICF2 0	OCF2 0	TIMD 0	0 0	0 0
14	IC1HR Reset value	MSB							LSB
15	IC1LR Reset value	MSB							LSB
16	OC1HR Reset value	MSB 1	- 0	- 0	- 0	- 0	- 0	- 0	LSB 0
17	OC1LR Reset value	MSB 0	- 0	- 0	- 0	- 0	- 0	- 0	LSB 0
18	CHR Reset value	MSB 1	- 1	- 1	- 1	- 1	- 1	- 1	LSB 1
19	CLR Reset value	MSB 1	- 1	- 1	- 1	- 1	- 1	- 0	LSB 0
1A	ACHR Reset value	MSB 1	- 1	- 1	- 1	- 1	- 1	- 1	LSB 1
1B	ACLR Reset value	MSB 1	- 1	- 1	- 1	- 1	- 1	- 0	LSB 0
1C	IC2HR Reset value	MSB							LSB
1D	IC2LR Reset value	MSB							LSB
1E	OC2HR Reset value	MSB 1	- 0	- 0	- 0	- 0	- 0	- 0	LSB 0
1F	OC2LR Reset value	MSB 0	- 0	- 0	- 0	- 0	- 0	- 0	LSB 0

Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see *Figure 41*).

Procedure

1. Select the M bit to define the word length.
2. Select the desired baud rate using the SCIBRR and the SCIETPR registers.
3. Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.
4. Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CC register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit or after the break frame) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CC register.

Clearing the TC bit is performed by the following software sequence:

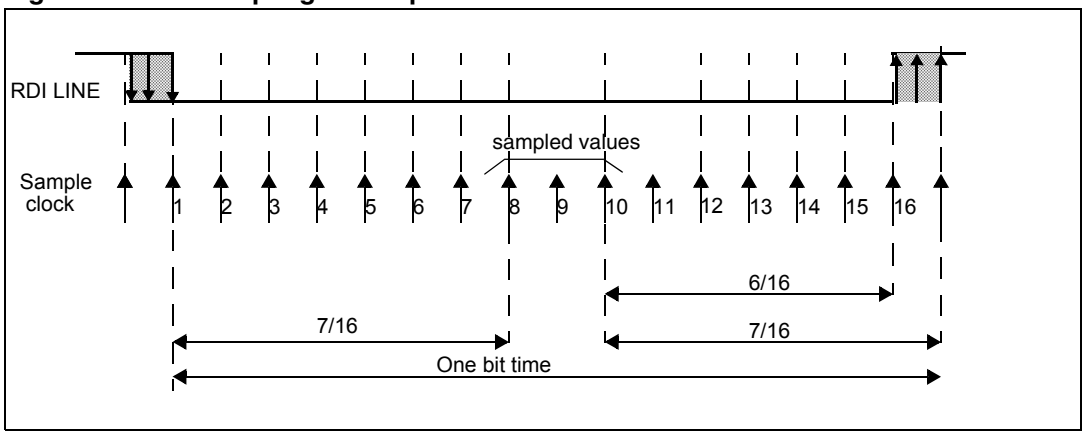
1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see *Figure 42*).

Figure 43. Bit sampling in reception mode



11.3.5 Low power modes

Table 27. Low power modes

Mode	Description
WAIT	No effect on SCI. SCI interrupts cause the device to exit from Wait mode.
HALT	SCI registers are frozen. In Halt mode, the SCI stops transmitting/receiving until Halt mode is exited.

11.3.6 Interrupts

Table 28. Interrupts

Interrupt event	Event flag	Enable Control bit	Exit from Wait	Exit from Halt
Transmit Data register Empty	TDRE	TIE	Yes	No
Transmission Complete	TC	TCIE	Yes	No
Received Data Ready to be Read	RDRF	RIE	Yes	No
Overrun Error Detected	OR		Yes	No
Idle Line Detected	IDLE	ILIE	Yes	No
Parity Error	PE	PIE	Yes	No

The SCI interrupt events are connected to the same interrupt vector.

These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

11.5.7 Register description

I²C Control register (CR)

Reset value: 0000 0000 (00h)

7							0
0	0	PE	ENGC	START	ACK	STOP	ITE
Read/write							

[7:6] Reserved. Forced to 0 by hardware.

5 **PE** *Peripheral enable.*
This bit is set and cleared by software.
0: Peripheral disabled
1: Master/Slave capability

Note: When PE=0, all the bits of the CR register and the SR register except the Stop bit are reset. All outputs are released while PE=0.
When PE=1, the corresponding I/O pins are selected by hardware as alternate functions.
*To enable the I²C interface, write the CR register **TWICE** with PE=1 as the first write only activates the interface (only PE is set).*

4 **ENGC** *Enable General Call.*
This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0). The 00h General Call address is acknowledged (01h ignored).
0: General Call disabled
1: General Call enabled

Note: In accordance with the I^2C standard, when GCAL addressing is enabled, an I^2C slave can only receive data. It will not transmit data to the master.

3 **START** *Generation of a Start condition*. This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0) or when the Start condition is sent (with interrupt generation if ITE=1).
In master mode:
0: No start generation
1: Repeated start generation
In slave mode:
0: No start generation
1: Start generation when the bus is free

Table 43. I²C register map

Address (Hex.)	Register name	7	6	5	4	3	2	1	0
39	DR	DR7 .. DR0							
3B	OAR	ADD7 .. ADD0							
3C	CCR	FM/SM	CC6 .. CC0						
3D	SR2				AF	STOPF	ARLO	BERR	GCAL
3E	SR1	EVF		TRA	BUSY	BTF	ADSL	M/SL	SB
3F	CR			PE	ENGC	START	ACK	STOP	ITE

Note: Refer to Section 16: Known limitations for information regarding a limitation on the alternate function on pin PA2 (SCL).

12 Instruction set

12.1 ST7 addressing modes

The ST7 Core features 17 different addressing modes which can be classified in 7 main groups:

Table 47. Addressing modes

Addressing mode	Example
Inherent	nop
Immediate	ld A,#$55
Direct	ld A,$55
Indexed	ld A,($55,X)
Indirect	ld A,([$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two sub-modes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimizes the use of long and short addressing modes.

Table 48. ST7 addressing mode overview

Mode			Syntax	Destination/ source	Pointer address	Pointer size (Hex.)	Length (bytes)
Inherent			nop				+ 0
Immediate			ld A,#$55				+ 1
Short	Direct		ld A,$10	00..FF			+ 1
Long	Direct		ld A,$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0 (with X register) + 1 (with Y register)
Short	Direct	Indexed	ld A,($10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,($1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[$10]	00..FF	00..FF	byte	+ 2

13 Electrical characteristics

13.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

13.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25 °C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

13.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25 °C, V_{DD}=5 V. They are given only as design guidelines and are not tested.

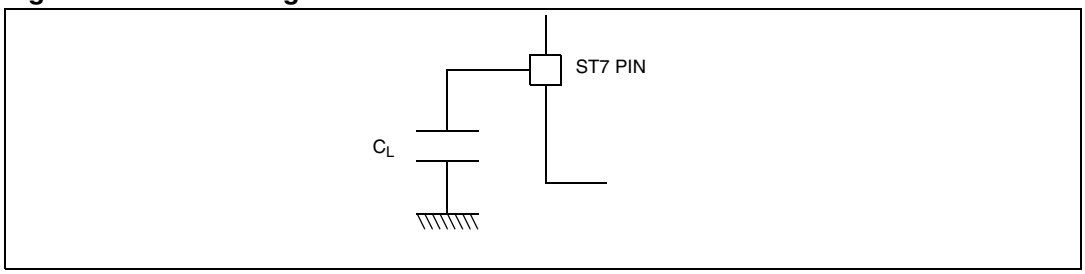
13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 52*.

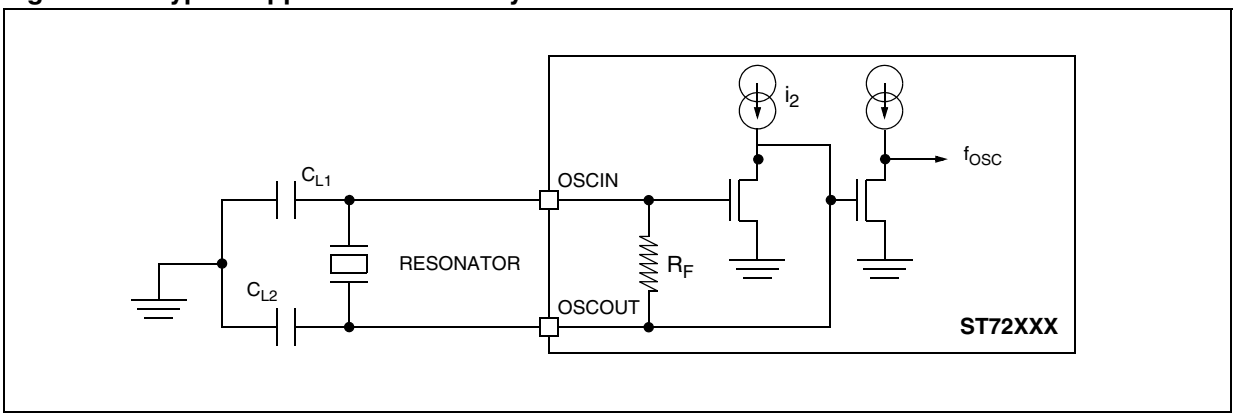
Figure 52. Pin loading conditions



13.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 53*.

Figure 58. Typical application with a crystal resonator



13.6 Memory characteristics

Subject to general operating conditions for f_{CPU}, and T_A unless otherwise specified.

Table 64. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or RESET)	2.0	-	-	V

1. Guaranteed by design. Not tested in production.

13.6.1 Flash memory

Operating Conditions: f_{CPU} = 8 MHz.

Table 65. Dual voltage Flash memory(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CPU}	Operating frequency	Read mode	-	-	8	MHz
		Write / Erase mode, T_A=25 °C	-	-	8	
V_{PP}	Programming voltage	4.0 V ≤V_{DD} ≤ 5.5 V	11.4	-	12.6	V
I_{PP}	V_{PP} current	Write / Erase	-	30	-	mA
t_{VPP}	Internal V_{PP} stabilization time		-	10	-	µs
t_{RET}	Data retention	T_A ≤ 5 5°C	40	-	-	years
N_{RW}	Write/erase cycles	T_A=25 °C	100	-	-	cycles

1. Refer to the Flash programming reference manual for the typical HDFlash programming and erase timing values.

Figure 73 and *Figure 74* show the reset circuit which protects the device against parasitic resets:

- The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
- Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in *Section Table 72.: Asynchronous RESET pin*. Otherwise the reset will not be taken into account internally.
- Because the reset circuit is designed to allow the internal reset to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in *Section Table 56.: Current characteristics*.

When the LVD is enabled:

- It is recommended not to connect a pull-up resistor or capacitor. A 10 nF pull-down capacitor is required to filter noise on the reset line.
- In case a capacitive power supply is used, it is recommended to connect a 1 MΩ pull-down resistor to the $\overline{\text{RESET}}$ pin to discharge any residual voltage induced by the capacitive effect of the power supply (this will add 5 µA to the power consumption of the MCU).
- Tips when using the LVD:
  a) Check that all recommendations related to ICCCLK and reset circuit have been applied (see notes above).
  b) Check that the power supply is properly decoupled (100 nF + 10 µF close to the MCU). Refer to AN1709 and AN2017. If this cannot be done, it is recommended to put a 100 nF + 1 MΩ pull-down on the $\overline{\text{RESET}}$ pin.
  c) The capacitors connected on the $\overline{\text{RESET}}$ pin and also the power supply are key to avoid any start-up marginality. In most cases, steps a) and b) above are sufficient for a robust solution. Otherwise: replace 10 nF pull-down on the $\overline{\text{RESET}}$ pin with a 5 µF to 20 µF capacitor.

Figure 73. $\overline{\text{RESET}}$ pin protection when LVD is enabled

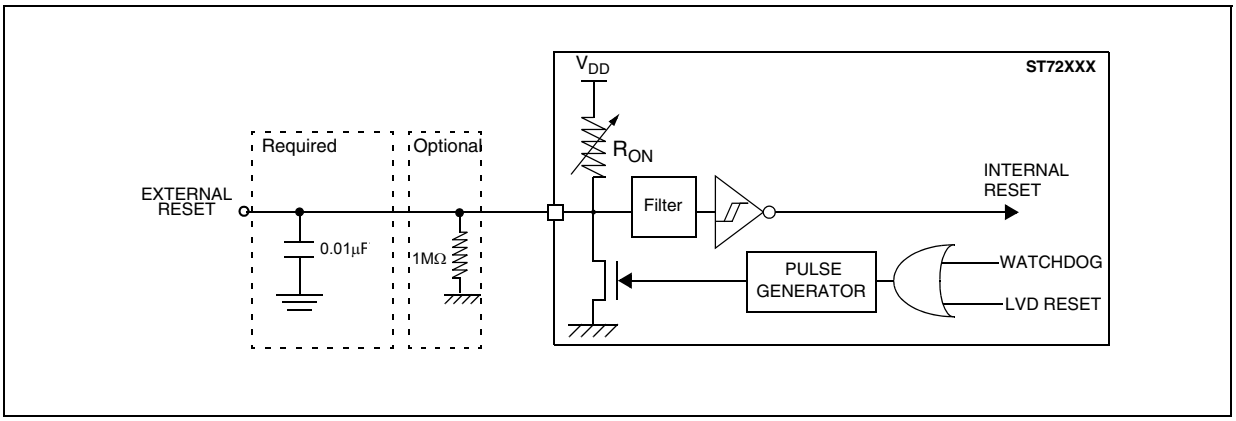
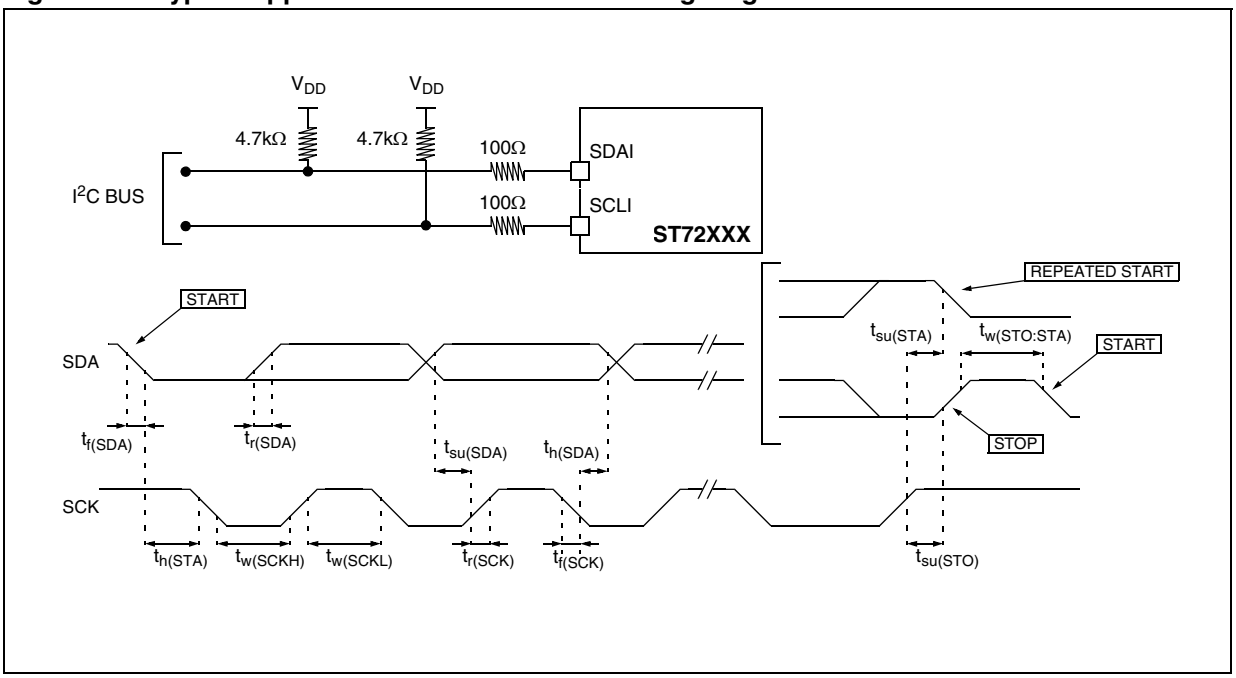


Figure 76. Typical application with I²C bus and timing diagram



1. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.

Figure 77. Typical application with ADC

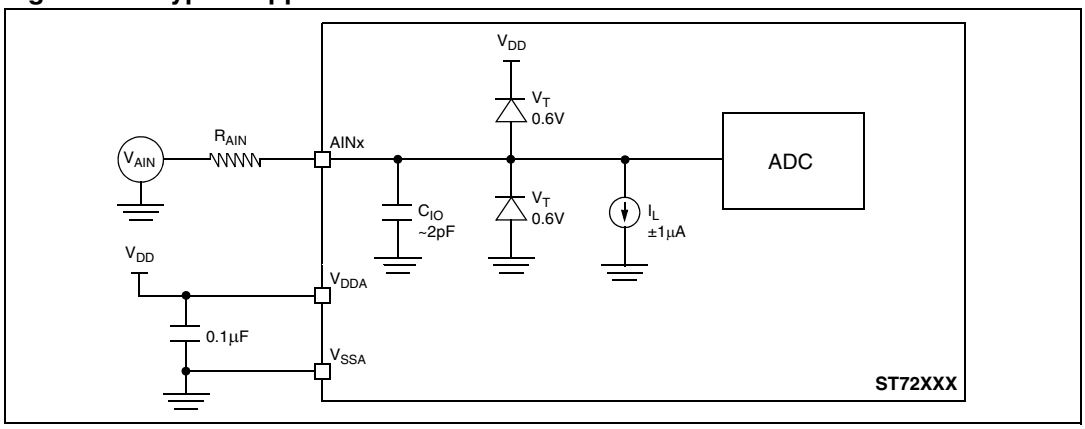


Table 79. ADC accuracy with V_{DD}=5 V, f_{CPU}= 8 MHz, f_{ADC}=4 MHz, R_{AIN}< 10 kΩ

Symbol	Parameter	Typ	Max(1)(2)
$\|E_T\|$	Total unadjusted error(3)	1.5	2
$\|E_{OI}\|$	Offset error(3)	0.5	1
$\|E_{GI}\|$	Gain Error(3)	0.5	1.5
$\|E_D\|$	Differential linearity error(3)	1	1.5
$\|E_L\|$	Integral linearity error(3)	1	1.5

1. Data based on characterization results over the whole temperature range, not tested in production.
2. Data based on characterization results, to guarantee 99.73% within ± max value from 0 to 70 °C (± 3s distribution limits).
3. ADC Accuracy vs. Negative Injection Current:
For I_{INJ-}=0.8mA, the typical leakage induced inside the die is 1.6µA and the effect on the ADC accuracy is a loss of 1 LSB for each 10KΩ increase of the external analog source impedance. This effect on the ADC accuracy has been observed under worst-case conditions for injection:
- negative injection
- injection to an input with analog capability, adjacent to the enabled Analog input
- at 5V V_{DD} supply, and worst case temperature.

14.1 Package mechanical data

Figure 79. 32-pin plastic dual in-line package, shrink 400-mil width, package outline

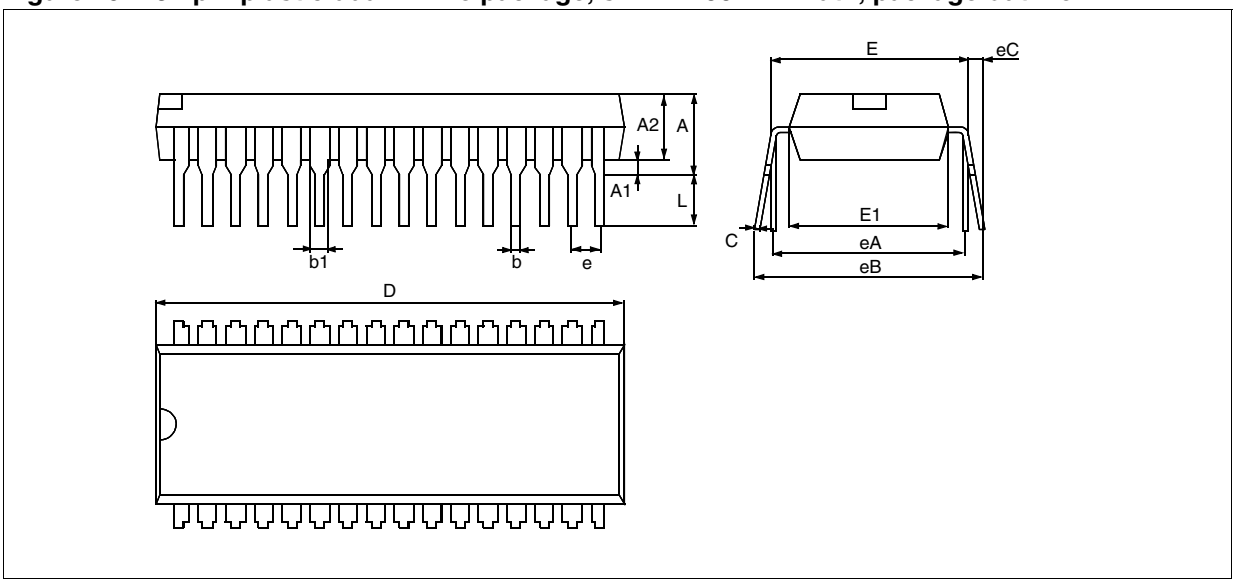


Table 80. 32-pin plastic dual in-line package, shrink 400-mil width, package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	3.560	3.760	5.080	0.1400	0.1480	0.2000
A1	0.510			0.0200		
A2	3.050	3.560	4.570	0.1200	0.1400	0.1800
b	0.360	0.460	0.580	0.0140	0.0180	0.0230
b1	0.760	1.020	1.400	0.0300	0.0400	0.0550
C	0.200	0.250	0.360	0.0080	0.0100	0.0140
D	27.430		28.450	1.0800	1.1000	1.1200
E	9.910	10.410	11.050	0.3900	0.4100	0.4350
E1	7.620	8.890	9.400	0.3000	0.3500	0.3700
e		1.780			0.0700	
eA		10.160			0.4000	
eB			12.700			0.5000
eC			1.400			0.0550
L	2.540	3.050	3.810	0.1000	0.1200	0.15000
	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

environment (IDE) with high-level language debugger, editor, project manager and integrated programming interface.

15.3.3 Programming tools

During the development cycle, the **ST7-EMU3 series emulators** and the **RLink** provide in-circuit programming capability for programming the Flash microcontroller on your application board.

In addition ST provides dedicated programming tools including the **ST7-EPB programming boards**, which include all the sockets required to program any of the devices in a specific ST7 sub-family.

For production programming of ST7 devices, ST's third-party tool partners also provide a complete range of gang and automated programming solutions, which are ready to integrate into your production environment.

15.3.4 Order codes for ST7263Bx development tools

Table 87. Development tool order codes for the ST7263Bx family

MCU	Starter kit	Evaluation board	Emulator	In-circuit debugger/programmer	Dedicated programmer
ST7263Bx	ST72F63B-SK/RAIS	ST7MDTULS-EVAL	ST7MDTU3-EMU3	STX-RLINK	ST7MDTU3-EPB

For additional ordering codes for spare parts and accessories, refer to the online product selector at www.st.com/mcu.