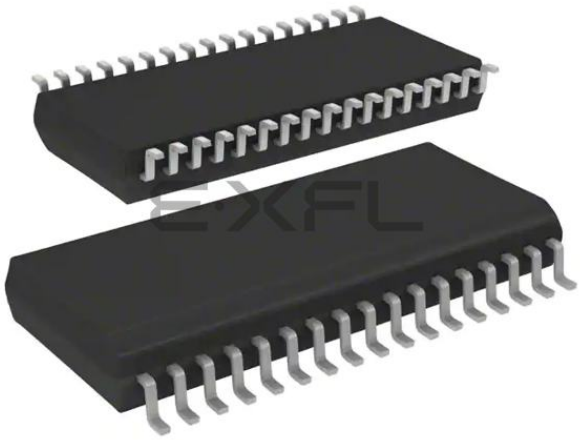

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	34-BSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63bk2m1

List of figures

6.2 Clock system

6.2.1 General description

The MCU accepts either a crystal or ceramic resonator, or an external clock signal to drive the internal oscillator. The internal clock (f_{CPU}) is derived from the external oscillator frequency (f_{OSC}), which is divided by 3 (and by 2 or 4 for USB, depending on the external clock used). The internal clock is further divided by 2 by setting the SMS bit in the miscellaneous register.

Using the OSC24/12 bit in the option byte, a 12 MHz or a 24 MHz external clock can be used to provide an internal frequency of either 2, 4 or 8 MHz while maintaining a 6 MHz for the USB (refer to *Figure 18*).

The internal clock signal (f_{CPU}) is also routed to the on-chip peripherals. The CPU clock signal consists of a square wave with a duty cycle of 50%.

The internal oscillator is designed to operate with an AT-cut parallel resonant quartz or ceramic resonator in the frequency range specified for f_{osc}. The circuit shown in *Figure 17* is recommended when using a crystal, and *Table 8* lists the recommended capacitance. The crystal and associated components should be mounted as close as possible to the input pins in order to minimize output distortion and start-up stabilization time.

Table 8. Recommended Values for 24 MHz crystal resonator

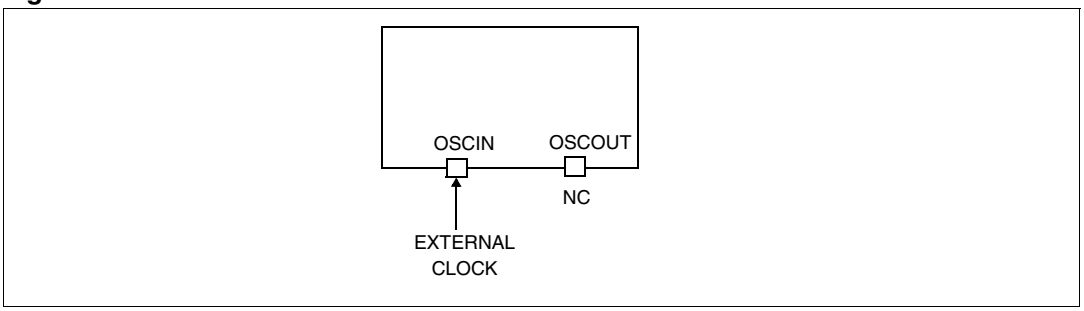
Recommended capacitance and resistance			
R_{SMAX}(1)	20 Ω	25 Ω	70 Ω
C_{OSCIN}	56pF	47pF	22pF
C_{OSCOUT}	56pF	47pF	22pF
R_P	1-10 MΩ	1-10 MΩ	1-10 MΩ

1. R_{SMAX} is the equivalent serial resistor of the crystal (see crystal specification).

6.2.2 External clock

An external clock may be applied to the OSCIN input with the OSCOUT pin not connected, as shown on *Figure 16*. The t_{OXOV} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} (see *Table 62: Control timing characteristics*).

Figure 16. External clock source connections



7							0
D7	D6	D5	D4	D3	D2	D1	D0
Read/write							

[7:0] **D[7:0]** *Data register 8 bits.*

Data Direction register (PxDDR)

Address

Port A Data Direction register (PADDR): 0001h

Port B Data Direction register (PBDDR): 0003h

Port C Data Direction register (PCDDR): 0005h

Port D Data Direction register (PDDDR): 0007h

Reset value

Port A: 0000 0000 (00h)

Port B: 0000 0000 (00h)

Port C: 1111 x000 (FXh)

Port D: 0000 0000 (00h)

Note: For Port C, unused bits (7-3) are not accessible

7							0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Read/write							

[7:0]D **D[7:0]** *Data Direction register 8 bits.*

The DDR register gives the input/output direction configuration of the pins. Each bit is set and cleared by software.

0: input mode

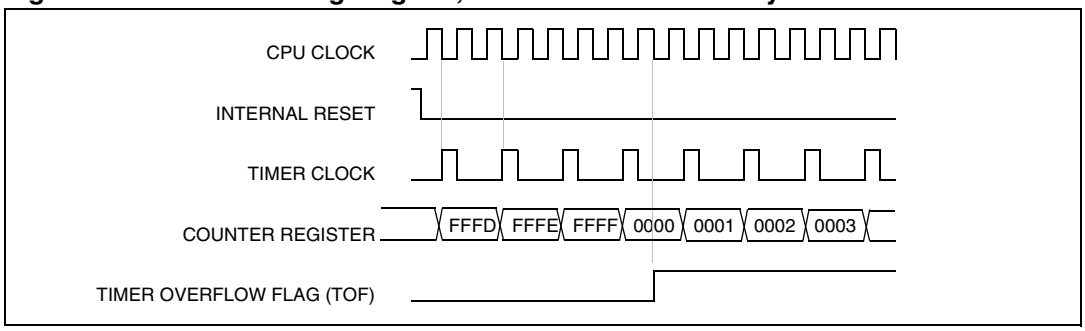
1: output mode

Table 16. I/O ports register map

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
00	PADR	MSB							LSB
01	PADDR	MSB							LSB
02	PBDR	MSB							LSB
03	PBDDR	MSB							LSB
04	PCDR	MSB							LSB
05	PCDDR	MSB							LSB
06	PDDR	MSB							LSB
07	PDDDR	MSB							LSB

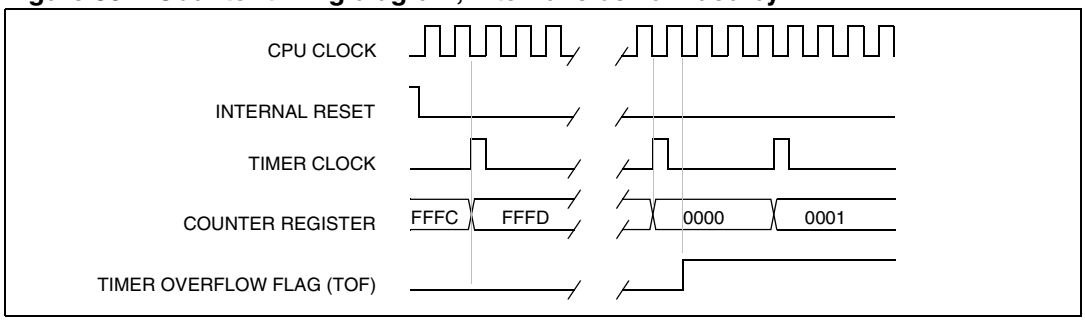
A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 29. Counter timing diagram, internal clock divided by 2



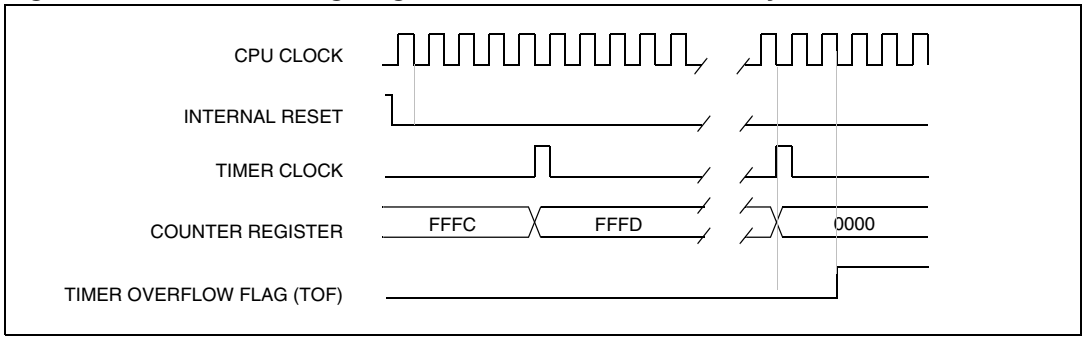
1. The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Figure 30. Counter timing diagram, internal clock divided by 4



1. The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Figure 31. Counter timing diagram, internal clock divided by 8



1. The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Note: 1 After reading the ICiHR register, transfer of input capture data is inhibited and ICFi will never be set until the ICiLR register is also read.

2 The ICiR register contains the free running counter value which corresponds to the most recent input capture.

3 The two input capture functions can be used together even if the timer also uses the two output compare functions.

4 In One Pulse mode and PWM mode only input Capture 2 can be used.

5 The alternate inputs (ICAP1 and ICAP2) are always directly connected to the timer. So any transitions on these pins activates the input capture function.
Moreover if one of the ICAPi pins is configured as an input and the second one as an output, an interrupt can be generated if the user toggles the output pin and if the ICIE bit is set.
This can be avoided if the input capture function i is disabled by reading the ICiHR (see note 1).

6 The TOF bit can be used with interrupt generation in order to measure events that go beyond the timer range (FFFFh).

Figure 32. Input Capture block diagram

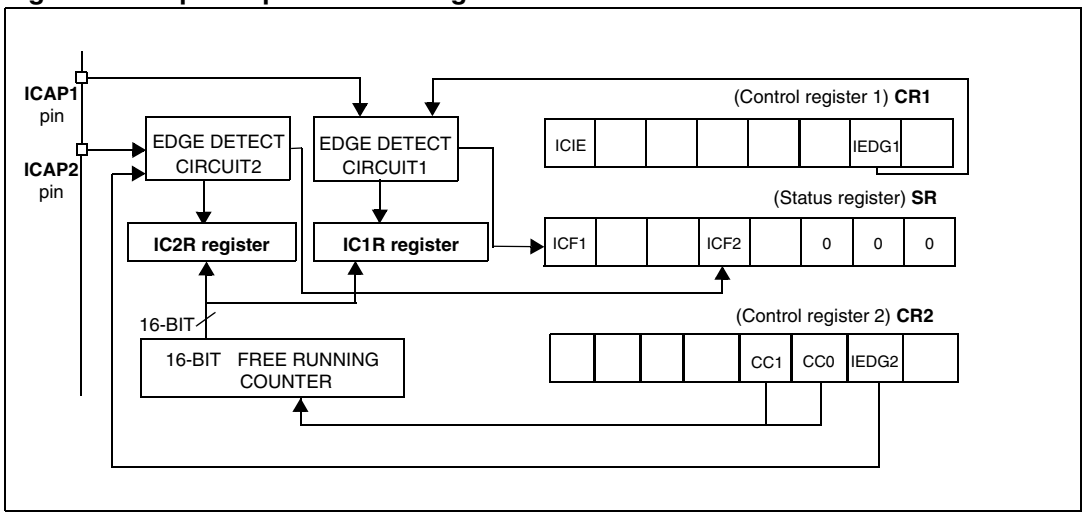
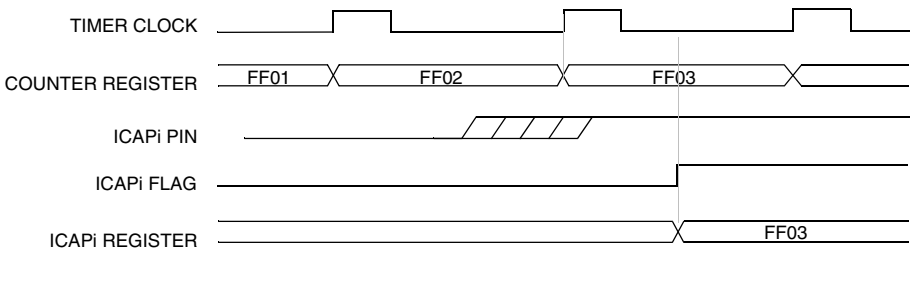


Figure 33. Input Capture timing diagram



1. The rising edge is the active edge.

11.2.7 Register description

Each Timer is associated with three control and status registers, and with six pairs of data registers (16-bit values) relating to the two input captures, the two output compares, the counter and the alternate counter.

Control register 1 (CR1)

Reset value: 0000 0000 (00h)

7							0
ICIE	OCIE	TOIE	FOLV2	FOLV1	OLVL2	IEDG1	OLVL1
Read/write							

7 **ICIE** input *Capture Interrupt Enable.*

0: Interrupt is inhibited.

1: A timer interrupt is generated whenever the ICF1 or ICF2 bit of the SR register is set.

6 **OCIE** output *Compare Interrupt Enable.*

0: Interrupt is inhibited.

1: A timer interrupt is generated whenever the OCF1 or OCF2 bit of the SR register is set.

5 **TOIE** *Timer Overflow Interrupt Enable.*

0: Interrupt is inhibited.

1: A timer interrupt is enabled whenever the TOF bit of the SR register is set.

4 **FOLV2** *Forced output Compare 2.*
This bit is set and cleared by software.

0: No effect on the OCMP2 pin.

1:Forces the OLVL2 bit to be copied to the OCMP2 pin, if the OC2E bit is set and even if there is no successful comparison.

3 **FOLV1** *Forced output Compare 1.*
This bit is set and cleared by software.

0: No effect on the OCMP1 pin.

1: Forces OLVL1 to be copied to the OCMP1 pin, if the OC1E bit is set and even if there is no successful comparison.

2 **OLVL2** *output Level 2.*
This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OC2R register and OCxE is set in the CR2 register. This value is copied to the OCMP1 pin in One Pulse mode and Pulse Width Modulation mode.

1 **IEDG1** *input Edge 1.*
This bit determines which type of level transition on the ICAP1 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

0 **OLVL1** output *Level 1.*
The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OC1R register and the OC1E bit is set in the CR2 register.

Table 36. USB register map and reset values (continued)

Address (Hex.)	Register Name	7	6	5	4	3	2	1	0
27	IDR Reset value	DA7 x	DA6 x	EP1 x	EP0 x	CNT3 0	CNT2 0	CNT1 0	CNT0 0
28	ISTR Reset value	SUSP 0	DOVR 0	CTR 0	ERR 0	IOVR 0	ESUSP 0	RESET 0	SOF 0
29	IMR Reset value	SUSPM 0	DOVRM 0	CTRM 0	ERRM 0	IOVRM 0	ESUSPM 0	RESETM 0	SOFM 0
2A	CTLR Reset value	0 0	0 0	0 0	0 0	RESUME 0	PDWN 1	FSUSP 1	FRES 0
2B	DADDR Reset value	0 0	ADD6 0	ADD5 0	ADD4 0	ADD3 0	ADD2 0	ADD1 0	ADD0 0
2C	EP0RA Reset value	ST_OUT 0	DTOG_TX 0	STAT_TX1 0	STAT_TX0 0	TBC3 x	TBC2 x	TBC1 x	TBC0 x
2D	EP0RB Reset value	1 1	DTOG_RX 0	STAT_RX 1 0	STAT_RX 0 0	0 0	0 0	0 0	0 0
2E	EP1RA Reset value	ST_OUT 0	DTOG_TX 0	STAT_TX1 0	STAT_TX0 0	TBC3 x	TBC2 x	TBC1 x	TBC0 x
2F	EP1RB Reset value	CTRL 0	DTOG_RX 0	STAT_RX 1 0	STAT_RX 0 0	EA3 x	EA2 x	EA1 x	EA0 x
30	EP2RA Reset value	ST_OUT 0	DTOG_TX 0	STAT_TX1 0	STAT_TX0 0	TBC3 x	TBC2 x	TBC1 x	TBC0 x
31	EP2RB Reset value	CTRL 0	DTOG_RX 0	STAT_RX 1 0	STAT_RX 0 0	EA3 x	EA2 x	EA1 x	EA0 x

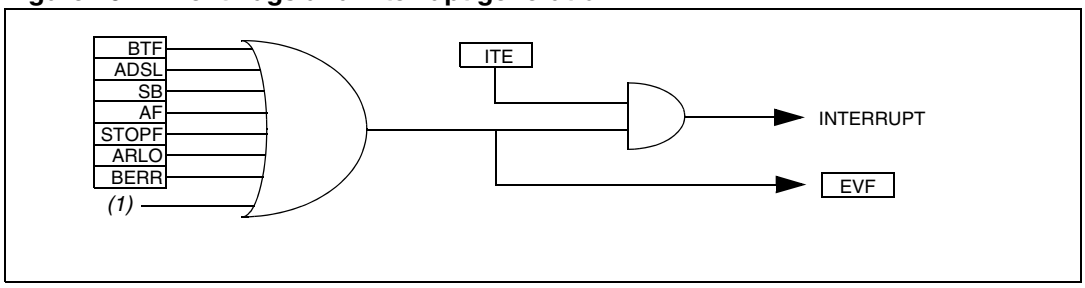
11.5.5 Low power modes

Table 41. Low power modes

Mode	Description
WAIT	No effect on I²C interface. I²C interrupts cause the device to exit from Wait mode.
HALT	I²C registers are frozen. In Halt mode, the I²C interface is inactive and does not acknowledge data on the bus. The I²C interface resumes operation when the MCU is woken up by an interrupt with “exit from Halt mode” capability.

11.5.6 Interrupts

Figure 49. Event flags and interrupt generation



1. EVF can also be set by EV6 or an error from the SR2 register.

Table 42. Interrupts

Interrupt event	Event flag	Enable control bit	Exit from Wait	Exit from Halt
End of Byte Transfer Event	BTF	ITE	Yes	No
Address Matched Event (Slave mode)	ADSL		Yes	No
Start Bit Generation Event (Master mode)	SB		Yes	No
Acknowledge Failure Event	AF		Yes	No
Stop Detection Event (Slave mode)	STOPF		Yes	No
Arbitration Lost Event (Multimaster configuration)	ARLO		Yes	No
Bus Error Event	BERR		Yes	No

The I²C interrupt events are connected to the same interrupt vector (see Interrupts chapter).

They generate an interrupt if the corresponding Enable Control Bit is set and the I-bit in the CC register is reset (RIM instruction).

I²C Data register (DR)

These bits contain the byte to be received or transmitted on the bus.

- Transmitter mode: byte transmission start automatically when the software writes in the DR register.
- Receiver mode: the first data byte is received automatically in the DR register using the least significant bit of the address. The following data bytes are then received one by one after reading the DR register.

Reset value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0
Read/write							

I²C Own Address register (OAR)

Reset value: 0000 0000 (00h)

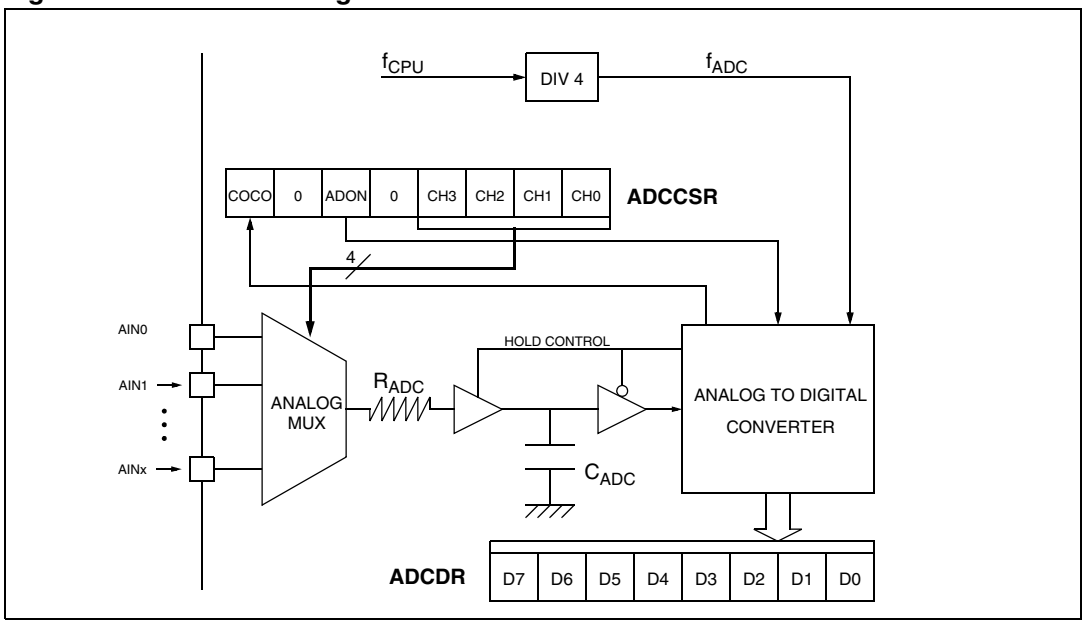
7							0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
Read/write							

[7:1] **ADD[7:1]** *Interface address.*
These bits define the I²C bus address of the interface. They are not cleared when the interface is disabled (PE=0).

0 **ADD0** *Address direction bit.*
This bit is don't care, the interface acknowledges either 0 or 1. It is not cleared when the interface is disabled (PE=0).

Note: Address 01h is always ignored.

Figure 50. ADC block diagram



Digital A/D conversion result

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than or equal to V_{DDA} (high-level voltage reference) then the conversion result in the DR register is FFh (full scale) without overflow indication.

If input voltage (V_{AIN}) is lower than or equal to V_{SSA} (low-level voltage reference) then the conversion result in the DR register is 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDR register. The accuracy of the conversion is described in the parametric section.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allotted time.

A/D conversion phases

The A/D conversion is based on two conversion phases as shown in *Figure 51*:

- Sample capacitor loading [duration: t_{LOAD}]
  During this phase, the V_{AIN} input voltage to be measured is loaded into the C_{ADC} sample capacitor.
- A/D conversion [duration: t_{CONV}]
  During this phase, the A/D conversion is computed (8 successive approximations cycles) and the C_{ADC} sample capacitor is disconnected from the analog input pin to get the optimum analog to digital conversion accuracy.

While the ADC is on, these two phases are continuously repeated.

At the end of each conversion, the sample capacitor is kept loaded with the previous measurement load. The advantage of this behavior is that it minimizes the current consumption on the analog pin in case of single input channel measurement.

Software procedure

Refer to the control/status register (CSR) and data register (DR) in *Section 11.6.6* for the bit definitions and to *Figure 51* for the timings.

ADC configuration

The total duration of the A/D conversion is 12 ADC clock periods ($1/f_{ADC}=4/f_{CPU}$).

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the CSR register:

- Select the CH[3:0] bits to assign the analog channel to be converted.

ADC conversion

In the CSR register:

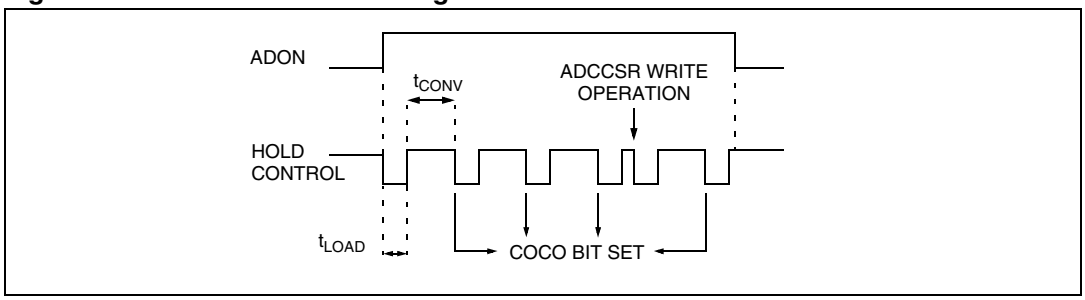
- Set the ADON bit to enable the A/D converter and to start the first conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

- The COCO bit is set by hardware.
- No interrupt is generated.
- The result is in the DR register and remains valid until the next conversion has ended.

A write to the CSR register (with ADON set) aborts the current conversion, resets the COCO bit and starts a new conversion.

Figure 51. ADC conversion timings



11.6.4 Low power modes

Table 44. Low power modes

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from Halt mode, the A/D Converter requires a stabilization time before accurate conversions can be performed.

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

11.6.5 Interrupts

None

11.6.6 Register description

Control/Status register (CSR)

Reset value: 0000 0000 (00h)

7							0
COCO	0	ADON	0	CH3	CH2	CH1	CH0
Read/write							

7 **COCO** *Conversion Complete*
This bit is set by hardware. It is cleared by software reading the result in the DR register or writing to the CSR register.
0: Conversion is not complete
1: Conversion can be read from the DR register

6 Reserved. must always be cleared.

5 **ADON** *A/D Converter On*
This bit is set and cleared by software.
0: A/D converter is switched off
1: A/D converter is switched on

4 Reserved. must always be cleared.

[3:0] **CH[3:0]** *Channel Selection*
These bits are set and cleared by software. They select the analog input to convert (see *Table 45*).

Table 45. Channel selection

Channel pin(1)	CH3(2)	CH2	CH1	CH0
AIN0	0	0	0	0
AIN1	0	0	0	1
AIN2	0	0	1	0
AIN3	0	0	1	1
AIN4	0	1	0	0
AIN5	0	1	0	1
AIN6	0	1	1	0
AIN7	0	1	1	1
AIN8	1	0	0	0
AIN9	1	0	0	1
AIN10	1	0	1	0
AIN11	1	0	1	1

1. The number of pins AND the channel selection varies according to the device. Refer to the device pinout.

Figure 64. V_{OL} high sink V_{DD}=5 V

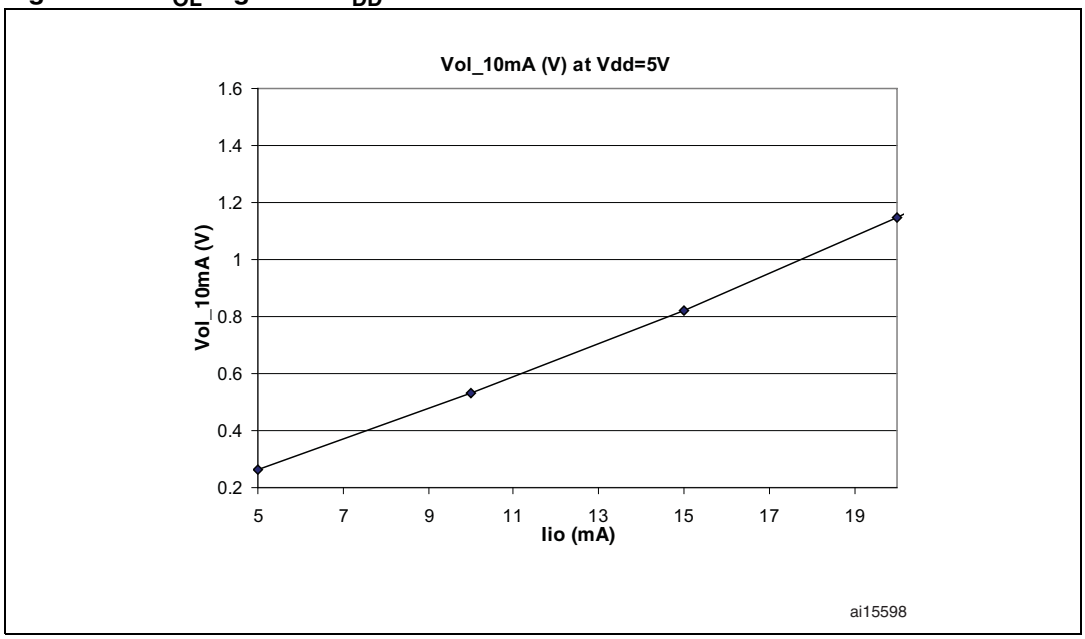


Figure 65. V_{OL} very high sink V_{DD}=5 V

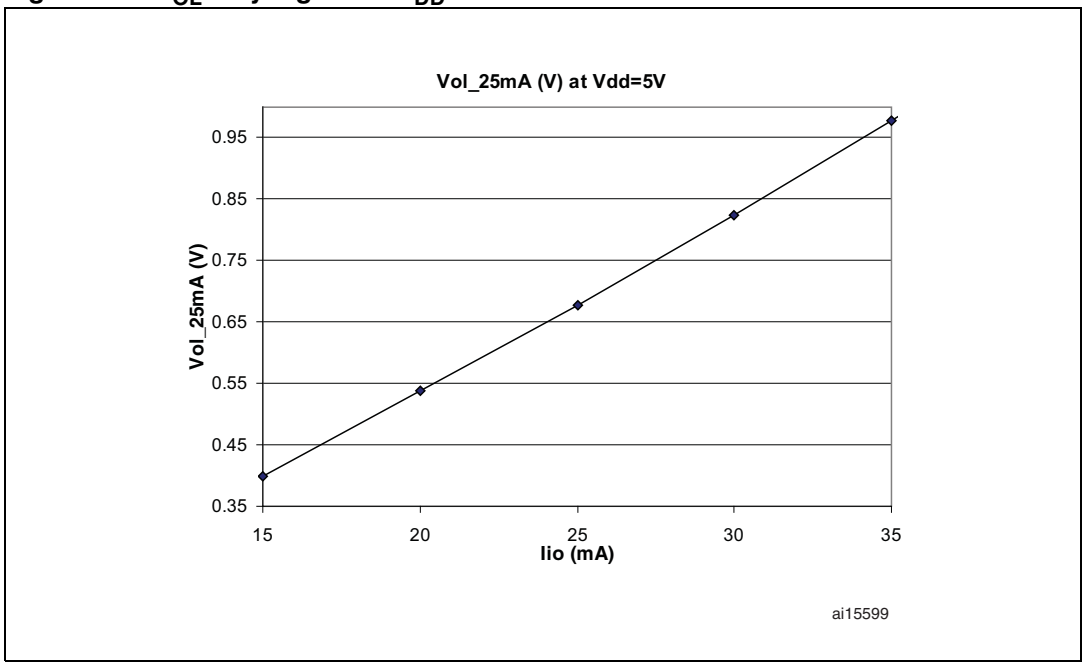


Figure 66. V_{OL} standard vs. V_{DD}

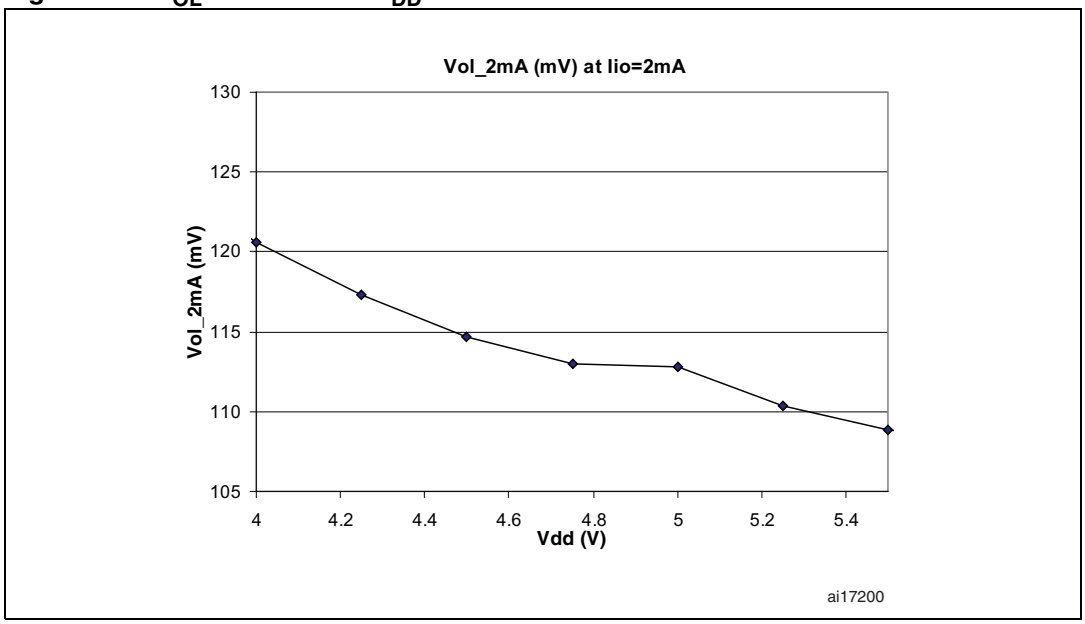


Figure 67. V_{OL} high sink vs. V_{DD}

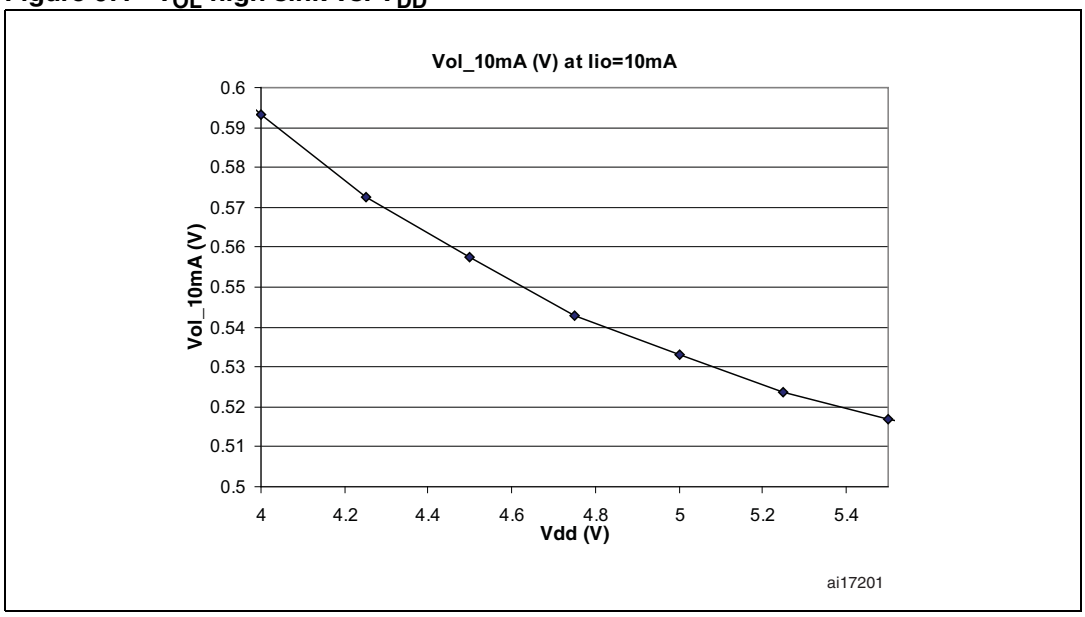


Figure 70. $|V_{DD}-V_{OH}|$ @ V_{DD}=5 V (high current)

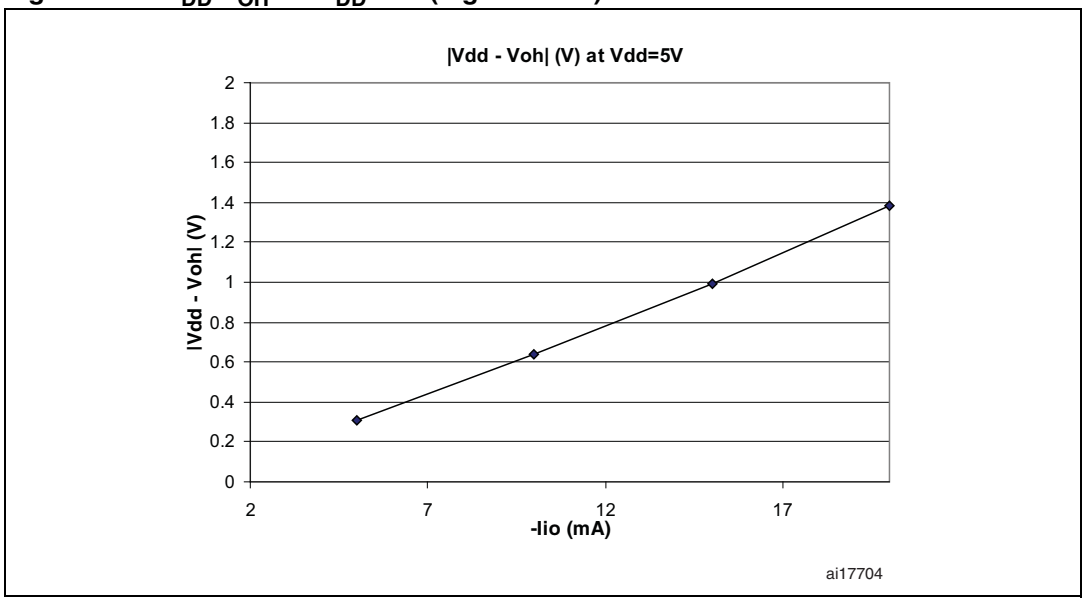


Figure 71. $|V_{DD}-V_{OH}|$ @ I_{IO}=2 mA (low current)

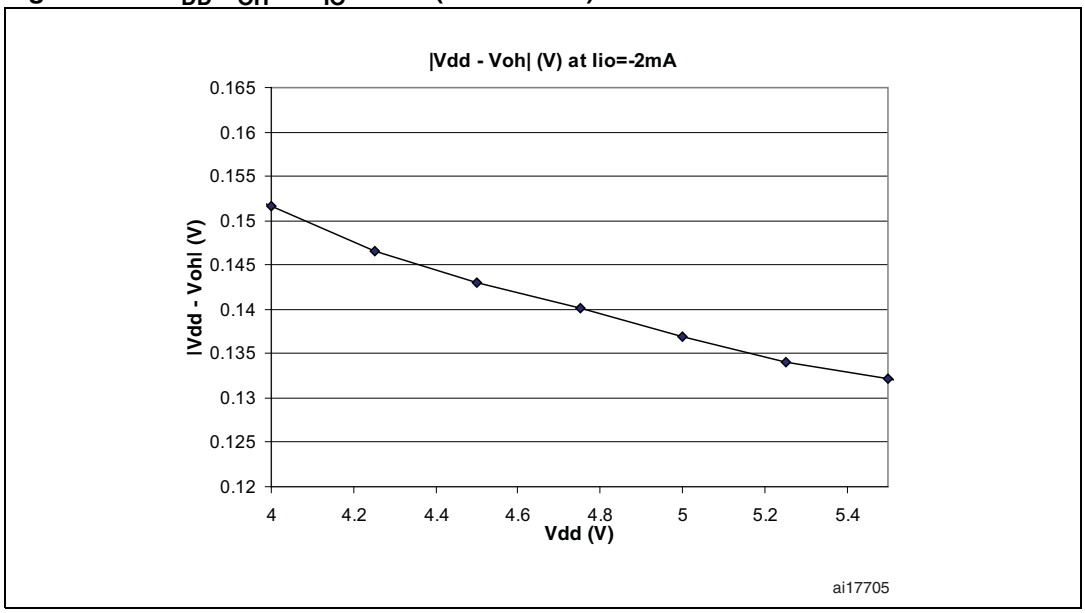


Table 77 gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Table 77. SCL frequency(1)(2)(3)(4)

f_{SCL} (kHz)	I2CCCR Value							
	f_{CPU}=4 MHz				f_{CPU}=8 MHz			
	V_{DD} = 4.1 V		V_{DD} = 5 V		V_{DD} = 4.1 V		V_{DD} = 5 V	
	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ
400	NA	NA	NA	NA	83h	83	83h	83h
300	NA	NA	NA	NA	85h	85h	85h	85h
200	83h	83h	83h	83h	8Ah	89h	8Ah	8Ah
100	10h	10h	10h	10h	24h	23h	24h	23h
50	24h	24h	24h	24h	4Ch	4Ch	4Ch	4Ch
20	5Fh	5Fh	5Fh	5Fh	FFh	FFh	FFh	FFh

1. Legend: R_P = External pull-up resistance; f_{SCL} = I^2C speed; NA = not achievable.
2. The above variations depend on the accuracy of the external components used.
3. For speeds around 200 kHz, achieved speed can have ±5% tolerance.
4. For other speed ranges, achieved speed can have ±2% tolerance.

13.11 8-bit ADC

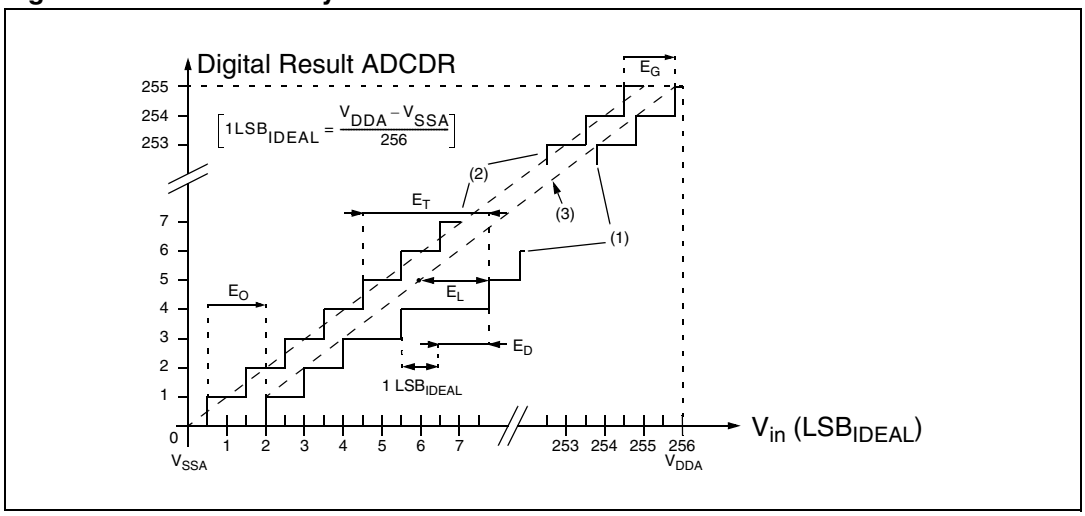
Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 78. 8-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		-	-	4	MHz
V_{AIN}	Conversion range voltage(2)		V_{SSA}	-	V_{DDA}	V
R_{AIN}	External input resistor		-	-	10(3)	κΩ
C_{ADC}	Internal sample and hold capacitor		-	6	-	pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8 MHz, f_{ADC}=2 MHz	0(4)			µs
t_{ADC}	Conversion time (Sample+Hold)		6			
	- Sample capacitor loading time - Hold conversion time		4 8			$1/f_{ADC}$

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V.
2. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refer to V_{DD} and V_{SS}.
3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
4. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Figure 78. ADC accuracy characteristics



1. (1) Example of an actual transfer curve; (2) The ideal transfer curve; (3) End point correlation line.
2. **E_T**=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   E_O=Offset Error: deviation between the first actual transition and the first ideal one.
   E_G=Gain Error: deviation between the last ideal transition and the last actual one.
   E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 88. ST7 application notes (continued)

Identification	Description
AN1014	How to Minimize the ST7 Power Consumption
AN1015	Software Techniques for Improving Microcontroller EMC Performance
AN1040	Monitoring the Vbus Signal for USB Self-Powered Devices
AN1070	ST7 Checksum Self-Checking Capability
AN1181	Electrostatic Discharge Sensitive Measurement
AN1324	Calibrating the RC Oscillator of the ST7FLITE0 MCU Using the Mains
AN1502	Emulated Data EEPROM with ST7 HDFLASH Memory
AN1529	Extending the Current & Voltage Capability on the ST7265 VDDF Supply
AN1530	Accurate Timebase for Low-cost ST7 Applications with Internal RC Oscillator
AN1605	Using an Active RC to Wakeup the ST7LITE0 from Power Saving mode
AN1636	Understanding and Minimizing ADC Conversion Errors
AN1828	PIR (Passive Infrared) Detector Using the ST7FLITE05/09/SUPERLITE
AN1946	Sensorless BLDC Motor Control and BEMF Sampling Methods with ST7MC
AN1953	PFC for ST7MC Starter Kit
AN1971	ST7LITE0 Microcontrolled Ballast
Programming and tools	
AN 978	ST7 Visual DeVELOP Software Key Debugging Features
AN 983	Key Features of the Cosmic ST7 C-Compiler Package
AN 985	Executing Code In ST7 RAM
AN 986	Using the Indirect Addressing mode with ST7
AN 987	ST7 Serial Test Controller Programming
AN 988	Starting with ST7 Assembly Tool Chain
AN1039	ST7 Math Utility Routines
AN1071	Half Duplex USB-to-Serial Bridge Using the ST72611 USB Microcontroller
AN1106	Translating Assembly Code from HC05 to ST7
AN1179	Programming ST7 Flash Microcontrollers in Remote ISP mode (In-situ Programming)
AN1446	Using the ST72521 Emulator to Debug an ST72324 Target Application
AN1477	Emulated Data EEPROM with Xflash Memory
AN1527	Developing a USB Smartcard Reader with ST7SCR
AN1575	On-Board Programming Methods for XFLASH and HDFLASH ST7 MCUs
AN1576	In-application Programming (IAP) Drivers for ST7 HDFLASH or XFLASH MCUs
AN1577	Device Firmware Upgrade (DFU) Implementation for ST7 USB Applications
AN1601	Software Implementation for ST7DALI-EVAL
AN1603	Using the ST7 USB Device Firmware Upgrade Development Kit (DFU-DK)

Table 89. Document revision history (continued)

Date	Revision	Changes
03-Oct-06	6	Important Notes section renamed to Known Limitations, *Section 16: Known limitations* New PA2 limitation added, *Section 16: Known limitations* *Figure 85 on page 183* added for silicon revision identification
20-Aug-07	7	New 16K LQFP48 package added to product family. Note added to V_{OH} data in *Section Table 71.: Output driving current* List of supported partnumber availability updated, *Table 86* Download address updated in *Section 15.3.4: Order codes for ST7263Bx development tools* and Option list.
12-Jun-2009	8	Removed FASTROM devices as well as 32 and 16 Kbyte ROM devices. Added caution note in *Section 6.1: Reset*. Replaced CCR by CC (Condition Code) register when the I bit is concerned. Updated alternate function condition for PB4 to PB7 in *Table 13: Port B description*. Renamed t_{DOG} and T_{DOGL}, t_{WDG} and t_{WDGL}. Removed EMC protective circuitry in *Figure 74: RESET pin protection when LVD is disabled* (device works correctly without these components). Removed all mentions to SPI interface. Removed dynamic latchup in *Section 13.7.3: Absolute maximum ratings (electrical sensitivity)*. Modified notes below *Table 85: Thermal characteristics*. Update *Table 86: Supported order codes* and *Figure 84: Option list*. Updated ECOPACK text, and removed recommended wave soldering profile and recommended reflow soldering oven profile, in *Section 14: Package characteristics*.