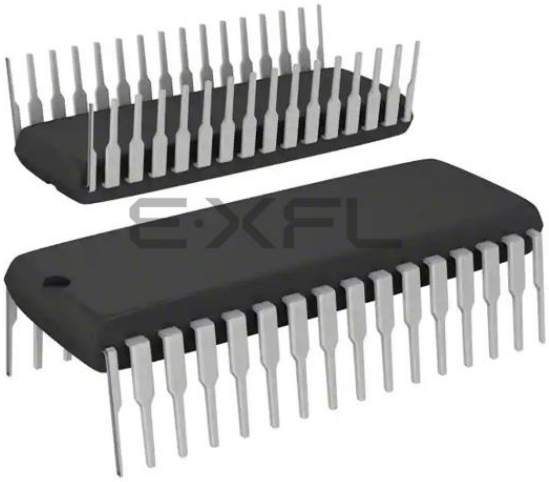

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63bk4b1

List of figures

Legend / Abbreviations for *Table 3* and *Table 4*:

Type: I = input, O = output, S = supply

In/Output level:C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: 10 mA = 10mA high sink (Fn N-buffer only)

25 mA = 25 mA very high sink (on N-buffer only)
Port and control configuration:

- Input:float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull, T = True open drain

The RESET configuration of each pin is shown in bold. This configuration is kept as long as the device is under reset state.

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
1	1	7	6	V_{DD}	S									Power supply voltage (4- 5.5 V)	
2	2	8	7	OSCOUT	O									Oscillator output	
3	3	9	8	OSCIN	I									Oscillator input	
4	4	10	9	V_{SS}	S									Digital ground	
5	5	11	10	PC2/USBOE	I/O	CT			X				X	Port C2	USB output Enable
6	6	12	13	PC1/TDO	I/O	CT			X				X	Port C1	SCI Transmit Data output
7	7	13	14	PC0/RDI	I/O	CT			X				X	Port C0	SCI Receive Data input
8	8	14	15	$\overline{\text{RESET}}$	I/O				X			X		Reset	
-	9	15	16	NC	--									Not connected	
-	-	16	17	NC	--									Not connected	
-	-	-	18	NC	--									Not connected	
-	-	-	19	NC	--									Not connected	
-	-	-	20	NC	--									Not connected	
-	-	-	21	NC	--									Not connected	
-	-	-	22	NC	--									Not connected	
9	10	17	23	PB7/AIN7/IT8	I/O	CT	10mA	X		X	X		X	Port B7	ADC analog input 7
10	11	18	24	PB6/AIN6/IT7	I/O	CT	10mA	X		X	X		X	Port B6	ADC analog input 6
11	12	19	25	V_{PP}/TEST	S									Programming supply	
12	13	20	26	PB5/AIN5/IT6	I/O	CT	10mA	X		X	X		X	Port B5	ADC analog input 5
13	14	21	27	PB4/AIN4/IT5	I/O	CT	10mA	X		X	X		X	Port B4	ADC analog input 4
14	15	22	28	PB3/AIN3	I/O	CT	10mA	X			X		X	Port B3	ADC analog input 3

3 Register and memory map

As shown in *Figure 7*, the MCU is capable of addressing 32 Kbytes of memories and I/O registers.

The available memory locations consist of up to 1024 bytes of RAM including 64 bytes of register locations, and up to 32K bytes of user program memory in which the upper 32 bytes are reserved for interrupt vectors. The RAM space includes up to 128 bytes for the stack from 0100h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

Caution: Memory locations noted “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 7. Memory map

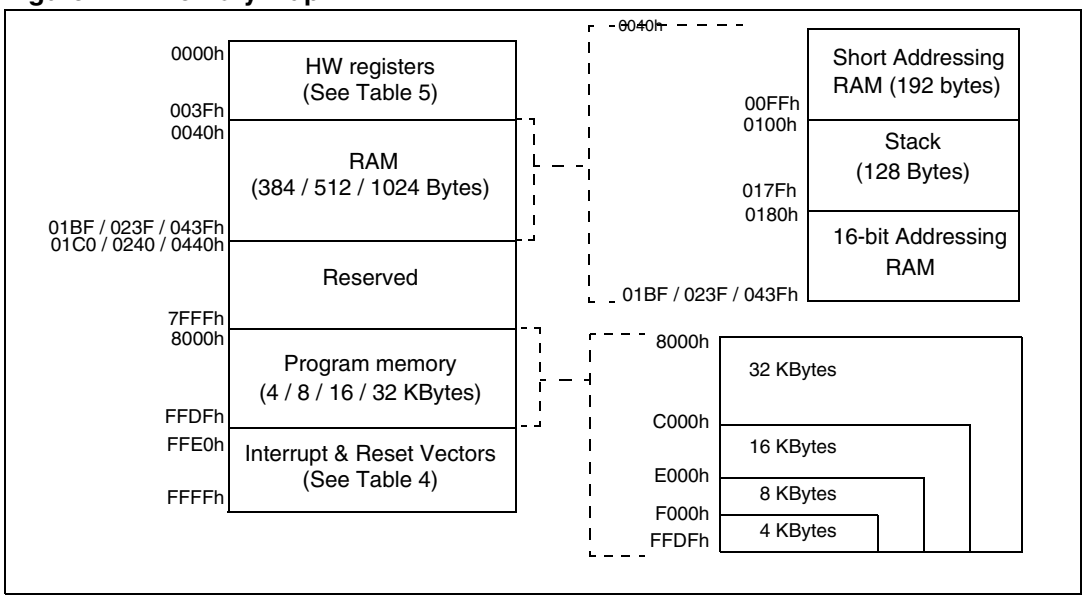


Table 5. Interrupt vector map

Vector address	Description	Masked	Remarks	Exit from Halt
FFE0h-FFEDh	Reserved area			
FFEEh-FFEFh	USB interrupt vector	I- bit	Internal interrupt	No
FFF0h-FFF1h	SCI interrupt vector	I- bit	Internal interrupt	No
FFF2h-FFF3h	I²C interrupt vector	I- bit	Internal interrupt	No
FFF4h-FFF5h	TIMER interrupt vector	I- bit	Internal interrupt	No
FFF6h-FFF7h	IT1 to IT8 interrupt vector	I- bit	External interrupt	Yes
FFF8h-FFF9h	USB End Suspend mode interrupt vector	I- bit	External interrupts	Yes
FFFAh-FFFBh	Flash start programming interrupt vector	I- bit	Internal interrupt	Yes
FFFCh-FFFDh	TRAP (software) interrupt vector	None	CPU interrupt	No
FFFEh-FFFFh	RESET vector	None		Yes

pointed to by the SP. Then the other registers are stored in the next locations as shown in *Figure 10*.

- When an interrupt is received, the SP is decremented and the context is pushed on the stack.
- On return from interrupt, the SP is incremented and the context is popped from the stack.

A subroutine call occupies two locations and an interrupt five locations in the stack area.

Figure 10. Stack manipulation example

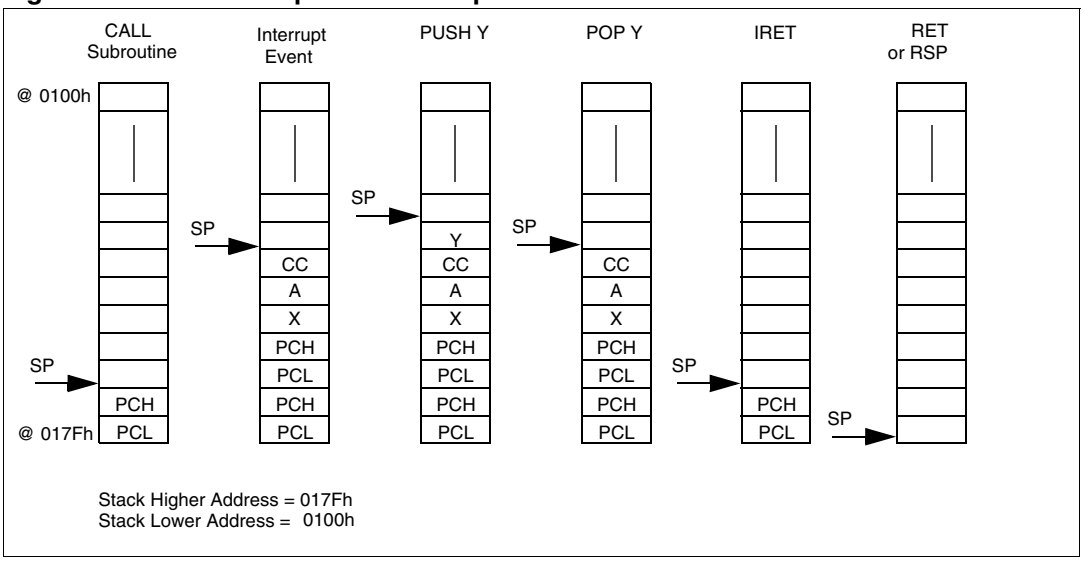
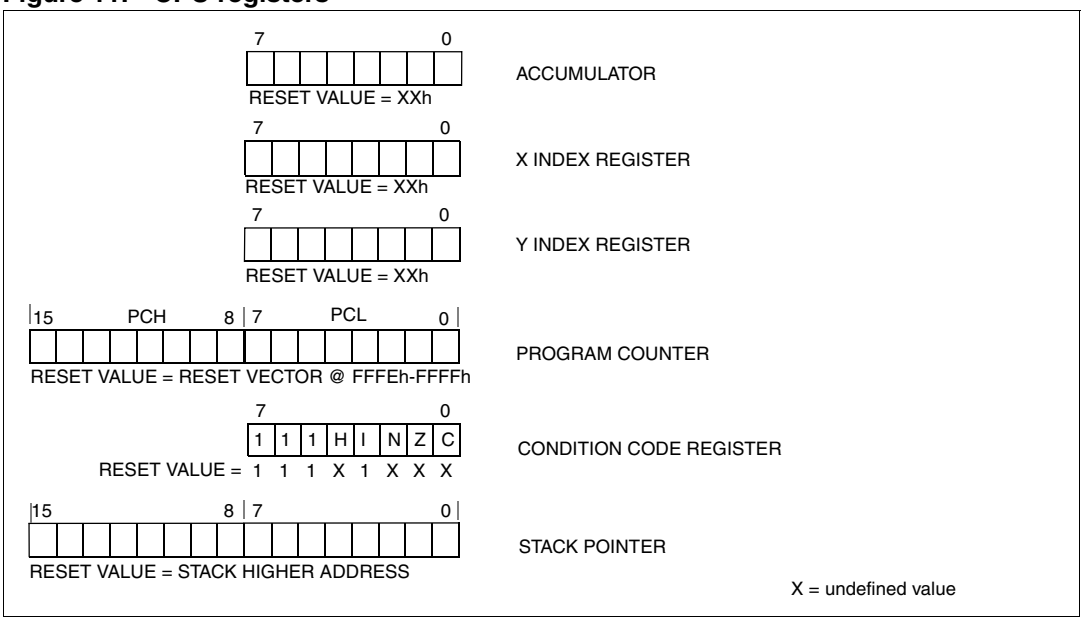


Figure 11. CPU registers



9 I/O ports

9.1 Introduction

The I/O ports offer different functional modes:

- Transfer of data through digital inputs and outputs and for specific pins
- Analog signal input (ADC)
- Alternate signal input/output for the on-chip peripherals
- External interrupt generation

An I/O port consists of up to 8 pins. Each pin can be programmed independently as a digital input (with or without interrupt generation) or a digital output.

9.2 Functional description

Each port is associated to 2 main registers:

- Data register (DR)
- Data Direction register (DDR)

Each I/O pin may be programmed using the corresponding register bits in DDR register: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

Table 10. I/O pin functions

DDR	Mode
0	Input
1	Output

Input modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Note: 1 All the inputs are triggered by a Schmitt trigger.

2 When switching from input mode to output mode, the DR register should be written first to output the correct value as soon as the port is configured as an output.

Interrupt function

When an I/O is configured as an input with interrupt, an event on this I/O can generate an external interrupt request to the CPU. The interrupt sensitivity is given independently according to the description mentioned in the ITRFRE interrupt register.

Each pin can independently generate an interrupt request.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see interrupts section). If more than one input pin is selected simultaneously as an interrupt source, this is logically ORed. For this reason if one of the interrupt pins is tied low, the other ones are masked.

9.3 I/O port implementation

The hardware implementation on each I/O port depends on the settings in the DDR register and specific feature of the I/O port such as ADC input or true open drain.

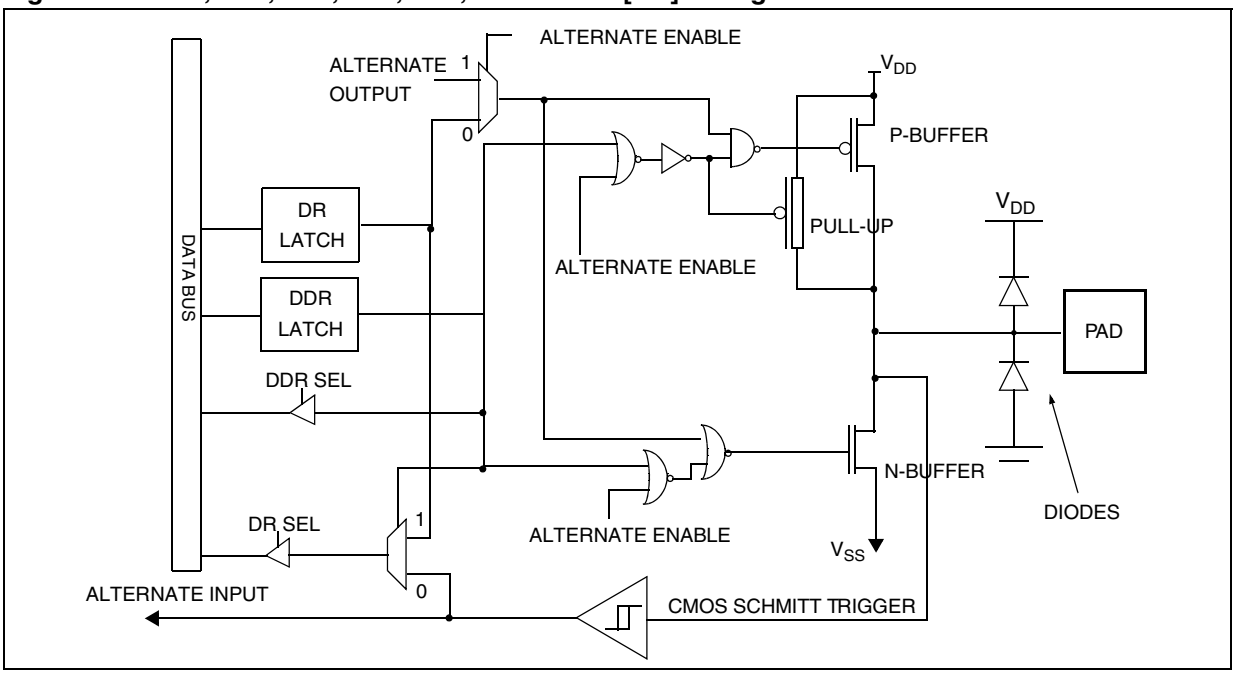
9.3.1 Port A

Table 11. Port A0, A3, A4, A5, A6, A7 description

PORT A	I/Os		Alternate function	
	Input(1)	Output	Signal	Condition
PA0	with pull-up	push-pull	MCO (Main Clock output)	MCO = 1 (MISCR)
PA3	with pull-up	push-pull	Timer EXTCLK	CC1 =1 CC0 = 1 (Timer CR2)
PA4	with pull-up	Push-pull	Timer ICAP1	
			IT1 Schmitt triggered input	IT1E = 1 (ITIFRE)
PA5	with pull-up	Push-pull	Timer ICAP2	
			IT2 Schmitt triggered input	IT2E = 1 (ITIFRE)
PA6(2)	with pull-up	Push-pull	Timer OCMP1	OC1E = 1
			IT3 Schmitt triggered input	IT3E = 1 (ITIFRE)
PA7	with pull-up	Push-pull	Timer OCMP2	OC2E = 1
			IT4 Schmitt triggered input	IT4E = 1 (ITIFRE)

1. Reset state.
2. Not available on SO24

Figure 22. PA0, PA3, PA4, PA5, PA6, PA7 and PD[7:4] configuration



Output Compare

In this section, the index, *i*, may be 1 or 2 because there are two output compare functions in the 16-bit timer.

This function can be used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the output Compare register and the free running counter, the output compare function:

- Assigns pins with a programmable value if the OC*i*E bit is set
- Sets a flag in the status register
- Generates an interrupt if enabled

Two 16-bit registers output Compare register 1 (OC1R) and output Compare register 2 (OC2R) contain the value to be compared to the counter register each timer clock cycle.

Table 20. OC/R register

	MS Byte	LS Byte
OC*i*R	OC*i*HR	OC*i*LR

These registers are readable and writable and are not affected by the timer hardware. A reset event changes the OC*i*R value to 8000h.

Timing resolution is one count of the free running counter: ($f_{CPU/CC[1:0]}$).

Procedure

To use the output compare function, select the following in the CR2 register:

1. Set the OC*i*E bit if an output is needed then the OCMP*i* pin is dedicated to the output compare *i* signal.
2. Select the timer clock (CC[1:0]) (see *Table 24*).
3. Select the following in the CR1 register:
   a) Select the OLVL*i* bit to applied to the OCMP*i* pins after the match occurs.
   b) Set the OCIE bit to generate an interrupt if it is needed.

When a match is found between OC*i*R register and CR register:

- OCF*i* bit is set.
- The OCMP*i* pin takes OLVL*i* bit value (OCMP*i* pin latch is forced low during reset).
- A timer interrupt is generated if the OCIE bit is set in the CR1 register and the I bit is cleared in the CC register (CC).

The OC*i*R register value required for a specific timing application can be calculated using the following formula:

$$\Delta \text{ OC}i\text{R} = \frac{\Delta t * f_{CPU}}{\text{PRESC}}$$

Where:

Δt = Output compare period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

Control register 1 (SCICR1)

Reset value: x000 0000 (x0h)

7							0
R8	T8	SCID	M	WAKE	PCE	PS	PIE
Read/write							

7 **R8** *Receive data bit 8.*
This bit is used to store the 9th bit of the received word when M=1.

6 **T8** *Transmit data bit 8.*
This bit is used to store the 9th bit of the transmitted word when M=1.

5 **SCID** *Disabled for low power consumption*
When this bit is set the SCI prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption.This bit is set and cleared by software.

0: SCI enabled

1: SCI prescaler and outputs disabled

4 **M** *Word length.*
This bit determines the word length. It is set or cleared by software.
0: 1 Start bit, 8 Data bits, 1 Stop bit
1: 1 Start bit, 9 Data bits, 1 Stop bit

Note: The M bit must not be modified during a data transfer (both transmission and reception).

3 **WAKE** *Wakeup method.*
This bit determines the SCI wakeup method, it is set or cleared by software.
0: Idle Line
1: Address Mark

2 **PCE** *Parity control enable.*
This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M=1; 8th bit if M=0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission).

0: Parity control disabled

1: Parity control enabled

1 **PS** *Parity selection.*
This bit selects the odd or even parity when the parity generation/detection is enabled (PCE bit set). It is set and cleared by software. The parity will be selected after the current byte.

0: Even parity

1: Odd parity

0 **PIE** *Parity interrupt enable.*
This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). It is set and cleared by software.

0: Parity error interrupt disabled

1: Parity error interrupt enabled.

2 RE *Receiver enable.*
This bit enables the receiver. It is set and cleared by software.
0: Receiver is disabled
1: Receiver is enabled and begins searching for a start bit

1 RWU *Receiver wakeup.*
This bit determines if the SCI is in mute mode or not. It is set and cleared by software and can be cleared by hardware when a wakeup sequence is recognized.
0: Receiver in Active mode
1: Receiver in Mute mode
Note: Before selecting Mute mode (setting the RWU bit), the SCI must receive some data first, otherwise it cannot function in Mute mode with wakeup by idle line detection.

0 **SBK** *Send break.*
This bit set is used to send break characters. It is set and cleared by software.
0: No break character is transmitted
1: Break characters are transmitted
Note: If the SBK bit is set to "1" and then to "0", the transmitter will send a BREAK word at the end of the current word.

Data register (SCIDR)

Reset value: Undefined

This register contains the received or transmitted data character, depending on whether it is read from or written to.

7							0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
Read/write							

The Data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR).
The TDR register provides the parallel interface between the internal bus and the output shift register (see *Figure 41*).
The RDR register provides the parallel interface between the input shift register and the internal bus (see *Figure 41*).

Interrupt Status register (ISTR)

Reset value: 0000 0000 (00h)

7							0
SUSP	DOVR	CTR	ERR	IOVR	ESUSP	RESET	SOF
Read.write							

When an interrupt occurs these bits are set by hardware. Software must read them to determine the interrupt type and clear them after servicing.

Note: These bits cannot be set by software.

7 **SUSP** *Suspend mode request*.
This bit is set by hardware when a constant idle state is present on the bus line for more than 3 ms, indicating a suspend mode request from the USB bus. The suspend request check is active immediately after each USB reset event and its disabled by hardware when suspend mode is forced (FSUSP bit of CTLR register) until the end of resume sequence.

6 **DOVR** *DMA over/underrun*.
This bit is set by hardware if the ST7 processor can't answer a DMA request in time.
0: No over/underrun detected
1: Over/underrun detected

5 **CTR** *Correct Transfer.* This bit is set by hardware when a correct transfer operation is performed. The type of transfer can be determined by looking at bits TP3-TP2 in register PIDR. The Endpoint on which the transfer was made is identified by bits EP1-EP0 in register IDR.
0: No Correct Transfer detected
1: Correct Transfer detected
Note: A transfer where the device sent a NAK or STALL handshake is considered not correct (the host only sends ACK handshakes). A transfer is considered correct if there are no errors in the PID and CRC fields, if the DATA0/DATA1 PID is sent as expected, if there were no data overruns, bit stuffing or framing errors.

4 **ERR** *Error.*
This bit is set by hardware whenever one of the errors listed below has occurred:
0: No error detected
1: Timeout, CRC, bit stuffing or nonstandard framing error detected

3 **IOVR** *Interrupt overrun.*
This bit is set when hardware tries to set ERR, or SOF before they have been cleared by software.
0: No overrun detected
1: Overrun detected

2 **ESUSP** *End suspend mode.*
This bit is set by hardware when, during suspend mode, activity is detected that wakes the USB interface up from suspend mode.
This interrupt is serviced by a specific vector, in order to wake up the ST7 from Halt mode.
0: No End Suspend detected
1: End Suspend detected

1 **RESET** *USB reset.*
This bit is set by hardware when the USB reset sequence is detected on the bus.
0: No USB reset signal detected
1: USB reset signal detected
Note: The DADDR, EP0RA, EP0RB, EP1RA, EP1RB, EP2RA and EP2RB registers are reset by a USB reset.

0 **SOF** *Start of frame.*
This bit is set by hardware when a low-speed SOF indication (keep-alive strobe) is seen on the USB bus. It is also issued at the end of a resume sequence.
0: No SOF signal detected
1: SOF signal detected

Note: To avoid spurious clearing of some bits, it is recommended to clear them using a load instruction where all bits which must not be altered are set, and all bits to be cleared are reset. Avoid read-modify-write instructions like AND, XOR.

Interrupt Mask register (IMR)

These bits are mask bits for all interrupt condition bits included in the ISTR. Whenever one of the IMR bits is set, if the corresponding ISTR bit is set, and the I bit in the CC register is cleared, an interrupt request is generated. For an explanation of each bit, please refer to the corresponding bit description in ISTR.

Reset value: 0000 0000 (00h)

7							0
SUSPM	DOVRM	CTRM	ERRM	IOVRM	ESUSPM	RESETM	SOFM
Read.write							

2 **ACK** *Acknowledge enable.*
This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE=0).

0: No acknowledge returned

1: Acknowledge returned after an address byte or a data byte is received

1 **STOP** *Generation of a Stop condition*.
This bit is set and cleared by software. It is also cleared by hardware in master mode. Note: This bit is not cleared when the interface is disabled (PE=0).

In Master mode:
0: No stop generation
1: Stop generation after the current byte transfer or after the current Start condition is sent. The STOP bit is cleared by hardware when the Stop condition is sent.

In Slave mode:
0: No stop generation
1: Release the SCL and SDA lines after the current byte transfer (BTF=1). In this mode the STOP bit has to be cleared by software.

0 **ITE** *Interrupt enable.*
This bit is set and cleared by software and cleared by hardware when the interface is disabled (PE=0).

0: Interrupts disabled

1: Interrupts enabled

Refer to *Figure 49* for the relationship between the events and the interrupt.

SCL is held low when the SB, BTF or ADSL flags or an EV6 event (See *Figure 48*) is detected.

Software procedure

Refer to the control/status register (CSR) and data register (DR) in *Section 11.6.6* for the bit definitions and to *Figure 51* for the timings.

ADC configuration

The total duration of the A/D conversion is 12 ADC clock periods ($1/f_{ADC}=4/f_{CPU}$).

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the CSR register:

- Select the CH[3:0] bits to assign the analog channel to be converted.

ADC conversion

In the CSR register:

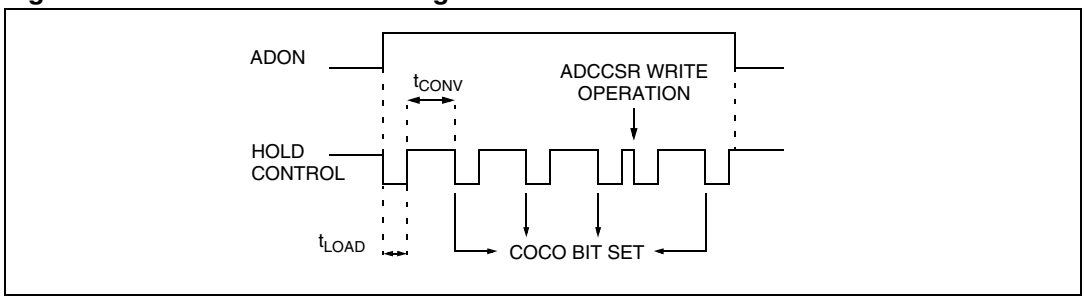
- Set the ADON bit to enable the A/D converter and to start the first conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

- The COCO bit is set by hardware.
- No interrupt is generated.
- The result is in the DR register and remains valid until the next conversion has ended.

A write to the CSR register (with ADON set) aborts the current conversion, resets the COCO bit and starts a new conversion.

Figure 51. ADC conversion timings



11.6.4 Low power modes

Table 44. Low power modes

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from Halt mode, the A/D Converter requires a stabilization time before accurate conversions can be performed.

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

2. For SDIP/SO34 devices, the CH3 bit is always at '0'. If, however, set to '1' on error, channel (11:8) becomes enabled which may result in a higher and unnecessary level of consumption.

Data register (DR)

This register contains the converted analog value in the range 00h to FFh.

Reset value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0
Read only							

Note: Reading this register reset the COCO flag.

Table 46. ADC register map

Address (Hex.)	Register name	7	6	5	4	3	2	1	0
0Ah	DR	AD7 .. AD0							
0Bh	CSR	COCO	0	ADON	0	CH3	CH2	CH1	CH0

13.4 Supply current characteristics

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for Halt mode for which the clock is stopped).

Table 60. Supply current characteristics

Symbol	Parameter	Conditions		Typ	Max	Unit
$\Delta I_{DD(\Delta Ta)}$	Supply current variation vs. temperature	Constant V_{DD} and f_{CPU}		-	10(1)	%
I_{DD}	CPU Run mode	I/Os in input mode	f_{CPU} = 4 MHz	7.5	9(2)(1)	mA
			f_{CPU} = 8 MHz	10.5	13(2)	
	CPU Wait mode		f_{CPU} = 4 MHz	6	8(1)	mA
			f_{CPU} = 8 MHz	8.5	11(2)	
	CPU Halt mode(3)	LVD disabled		25	40(1)	µA
	USB Suspend mode(4)	LVD disabled		100	120	µA
		LVD enabled		230	-	

1. Not tested in production, guaranteed by characterization.
2. Oscillator and watchdog running. All others peripherals disabled.
3. USB Transceiver and ADC are powered down.
4. CPU in Halt mode. Current consumption of external pull-up (1.5Kohms to USBVCC) and pull-down (15Kohms to V_{SSA}) not included.

Figure 55. Typ. I_{DD} in Run at f_{CPU} = 4 and 8 MHz

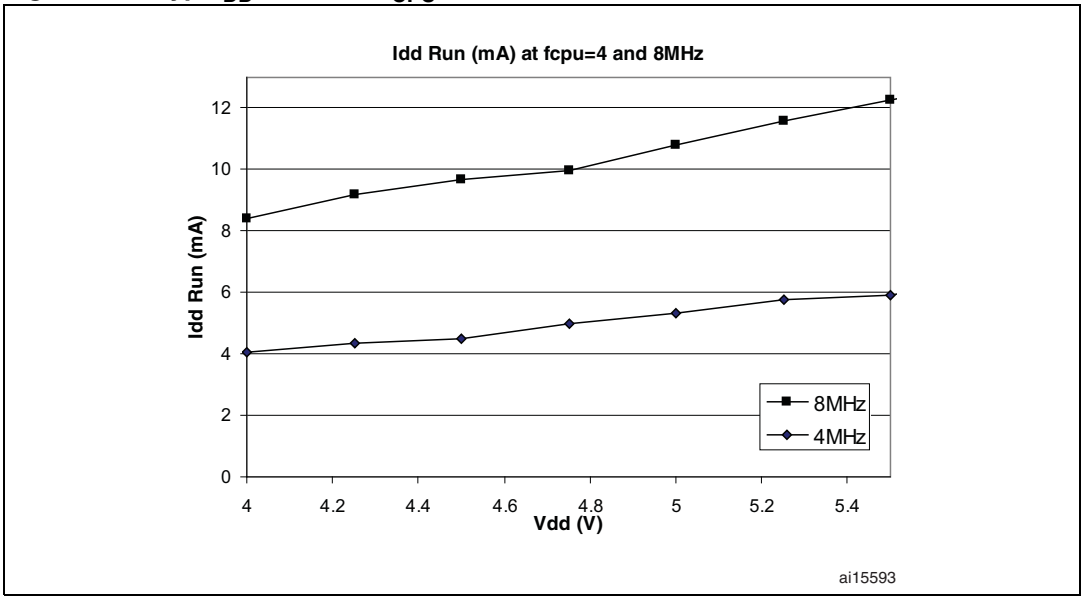


Table 77 gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Table 77. SCL frequency(1)(2)(3)(4)

f_{SCL} (kHz)	I2CCCR Value							
	f_{CPU}=4 MHz				f_{CPU}=8 MHz			
	V_{DD} = 4.1 V		V_{DD} = 5 V		V_{DD} = 4.1 V		V_{DD} = 5 V	
	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ	R_P=3.3 kΩ	R_P=4.7 kΩ
400	NA	NA	NA	NA	83h	83	83h	83h
300	NA	NA	NA	NA	85h	85h	85h	85h
200	83h	83h	83h	83h	8Ah	89h	8Ah	8Ah
100	10h	10h	10h	10h	24h	23h	24h	23h
50	24h	24h	24h	24h	4Ch	4Ch	4Ch	4Ch
20	5Fh	5Fh	5Fh	5Fh	FFh	FFh	FFh	FFh

1. Legend: R_P = External pull-up resistance; f_{SCL} = I^2C speed; NA = not achievable.
2. The above variations depend on the accuracy of the external components used.
3. For speeds around 200 kHz, achieved speed can have ±5% tolerance.
4. For other speed ranges, achieved speed can have ±2% tolerance.

13.11 8-bit ADC

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 78. 8-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		-	-	4	MHz
V_{AIN}	Conversion range voltage(2)		V_{SSA}	-	V_{DDA}	V
R_{AIN}	External input resistor		-	-	10(3)	κΩ
C_{ADC}	Internal sample and hold capacitor		-	6	-	pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8 MHz, f_{ADC}=2 MHz	0(4)			µs
t_{ADC}	Conversion time (Sample+Hold)		6			
	- Sample capacitor loading time - Hold conversion time		4 8			$1/f_{ADC}$

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V.
2. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refer to V_{DD} and V_{SS}.
3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.
4. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Figure 83. 40-lead very thin fine pitch quad flat no-lead package outline

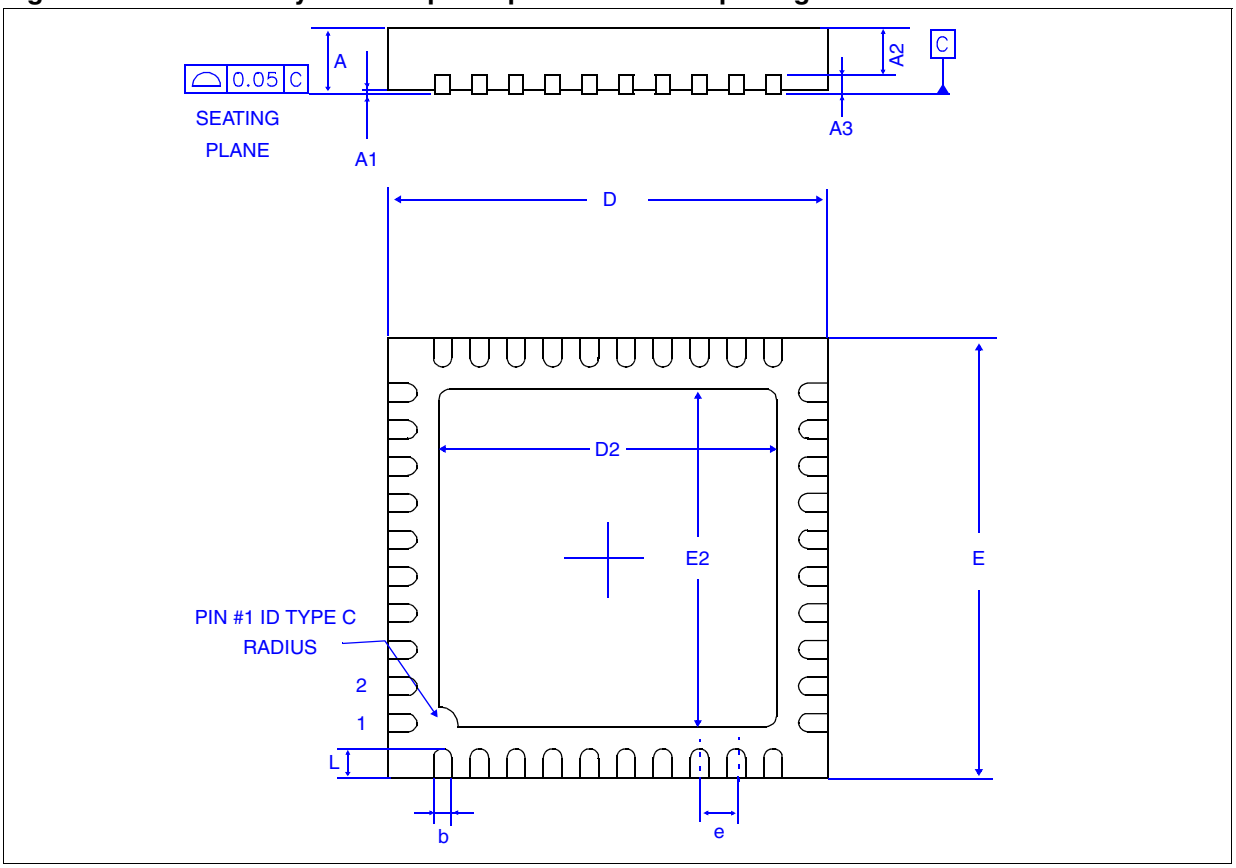


Table 84. 40-lead very thin fine pitch quad flat no-lead package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1		0.020	0.050		0.0008	0.0020
A2		0.650	1.000		0.0260	0.0390
A3		0.200			0.0080	
b	0.180	0.250	0.300	0.0070	0.0100	0.0120
D	5.850	6.000	6.150	0.2300	0.2360	0.2420
D2	2.750	2.90	3.050	0.1080	0.1140	0.1200
E	5.850	6.000	6.150	0.2300	0.2360	0.2420
E2	2.750	2.900	3.050	0.1080	0.1140	0.1200
e		0.500			0.0200	
L	0.300	0.400	0.500	0.0120	0.0160	0.0200
	Number of pins					
N	40					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

15 Device configuration and ordering information

Each device is available for production in user programmable versions (High Density FLASH).

ST72F63B FLASH devices are shipped to customers with a default content (FFh).

This implies that FLASH devices have to be configured by the customer using the Option Byte while the ROM devices are factory-configured.

15.1 Option byte

The Option Byte allows the hardware configuration of the microcontroller to be selected.

The Option Byte has no address in the memory map and can be accessed only in programming mode using a standard ST7 programming tool. The default contents of the FLASH is fixed to F7h. This means that all the options have “1” as their default value, except LVD.

In ROM devices, the Option Byte is fixed in hardware by the ROM code.

Option Byte

7							0
--	--	WDG SW	WD HALT	LVD	--	OSC 24/12	FMP_R

OPT 7:6 Reserved

OPT 5 **WDGSW** *Hardware or Software Watchdog*
This option bit selects the watchdog type.
0: Hardware enabled
1: Software enabled

OPT 4 **WDHALT** *Watchdog and Halt mode*
This option bit determines if a reset is generated when entering Halt mode while the Watchdog is active.
0: No Reset generation when entering Halt mode
1: Reset generation when entering Halt mode

OPT 3 **LVD** *Low voltage detector selection*
This option bit selects the LVD.
0: LVD enabled
1: LVD disabled
Note: Important: on ST7263BK1M1, ST7263BK2M1, ST7263BK2B1, and ST7263BK2B1 ROM devices, this option bit is forced by ST to 0 (LVD always enabled).

17 Revision history

Table 89. Document revision history

Date	Revision	Changes
27-May-05	3	New revision created by merging 32K Flash and non-32K Flash datasheets together. Memory Map, *Figure 7*, expanded to handle all devices and memory sizes. Operating conditions with LVD values modified, *Section 13.3.1: Operating conditions with low voltage detector (LVD)*. Supply current characteristics values and notes updated, *Section 13.4: Supply current characteristics*. IDD Run and Wait graphs replaced, *Figure 55* and *Figure 56 on page 143*. Control timing characteristics modified, *Section Table 62.: Control timing characteristics*. Flash memory table notes and t_{PROG} typical value updated, *Section 13.6.1: Flash memory*. Notes added for I/O Port Pin Characteristics table, *Section Table 70.: General characteristics*. Note for R_{PU} modified, removing reference to data characterization, *Section Table 70*. I_{PU} and R_{PU} graphs added, *Figure 61* and *Figure 62 on page 150*. Notes updated for USB low speed electrical characteristics. Output voltage/current graphs added, Figures *Figure 63.*-*Figure 72.*Thermal Characteristics added for SO24 and TQFP48 packages, *Section 14.2: Thermal characteristics*. Important note added for OPT 3 Option Byte (LVD), *Section 15.1: Option byte*. Supported Part Numbers table updated with full sales type codes, *Table 86*. Option List updated with all device options. Important notes updated with 'USB behavior with LVD disabled', *Section 16.3: USB behavior with LVD disabled*. Clock block diagram redrawn, *Figure 18 on page 36*. DFU added to title and features list. Removed unnecessary notes related to Typical Values (already mentioned in *Section 13.1.2: Typical values*) in electrical characteristic tables sections: *Section 13.3.1*, *Section 13.4*, *Section 13.6.1*, *Section Table 70.*, *Section Table 72*. and *Section 13.11*. Added note for max values in ADC Accuracy, *Section 13.11*. Static Latch Up (LU) class tested only for T_A=25°C, *Section : Static latchup (LU)*
19-Sep-05	4	Flash memory minimum data retention increased to 40 years, *Section 13.6.1: Flash memory* AF bit text modified concerning SCL, I^2C chapter *Section 11.5.7: Register description* Reference made to the Flash Programming Reference Manual for Flash timing values Reset pulse generated by WDG changed to 30 µs, *Section 11.1: Watchdog timer (WDG)* Modified text in *Section 11.3: Serial communications interface (SCI)*, adding Parity error as an interrupt Added ECOPACK information in *Section 14: Package characteristics* Modified I_S value and corresponding note in *Section Table 70.: General characteristics*
06-Apr-06	5	32K and 8K QFN40 Packages added 4K SO24 Package added TQFP package renamed to LQFP

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