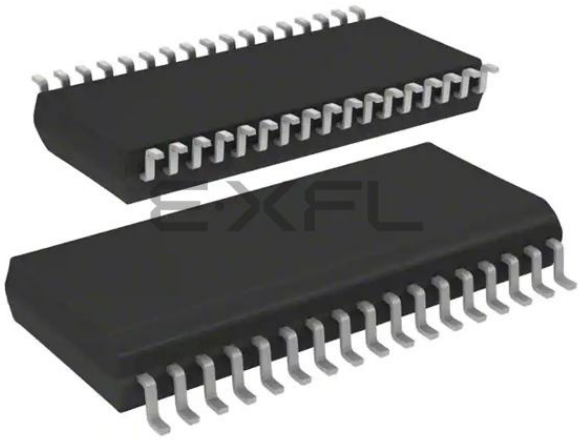

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SCI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	34-BSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f63bk4m1

Legend / Abbreviations for *Table 3* and *Table 4*:

Type: I = input, O = output, S = supply

In/Output level:C_T = CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: 10 mA = 10mA high sink (Fn N-buffer only)

25 mA = 25 mA very high sink (on N-buffer only)
Port and control configuration:

- Input:float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull, T = True open drain

The RESET configuration of each pin is shown in bold. This configuration is kept as long as the device is under reset state.

Table 3. Device pin description (QFN40, LQFP48, SO34 and SDIP32)

Pin n°				Pin name	Type	Level		Port /control						Main function (after reset)	Alternate function
								Input				Output			
SDIP32	SO34	QFN40	LQFP48			Input	Output	float	wpu	int	ana	OD	PP		
1	1	7	6	V_{DD}	S									Power supply voltage (4- 5.5 V)	
2	2	8	7	OSCOUT	O									Oscillator output	
3	3	9	8	OSCIN	I									Oscillator input	
4	4	10	9	V_{SS}	S									Digital ground	
5	5	11	10	PC2/USBOE	I/O	CT			X				X	Port C2	USB output Enable
6	6	12	13	PC1/TDO	I/O	CT			X				X	Port C1	SCI Transmit Data output
7	7	13	14	PC0/RDI	I/O	CT			X				X	Port C0	SCI Receive Data input
8	8	14	15	$\overline{\text{RESET}}$	I/O				X			X		Reset	
-	9	15	16	NC	--									Not connected	
-	-	16	17	NC	--									Not connected	
-	-	-	18	NC	--									Not connected	
-	-	-	19	NC	--									Not connected	
-	-	-	20	NC	--									Not connected	
-	-	-	21	NC	--									Not connected	
-	-	-	22	NC	--									Not connected	
9	10	17	23	PB7/AIN7/IT8	I/O	CT	10mA	X		X	X		X	Port B7	ADC analog input 7
10	11	18	24	PB6/AIN6/IT7	I/O	CT	10mA	X		X	X		X	Port B6	ADC analog input 6
11	12	19	25	V_{PP}/TEST	S									Programming supply	
12	13	20	26	PB5/AIN5/IT6	I/O	CT	10mA	X		X	X		X	Port B5	ADC analog input 5
13	14	21	27	PB4/AIN4/IT5	I/O	CT	10mA	X		X	X		X	Port B4	ADC analog input 4
14	15	22	28	PB3/AIN3	I/O	CT	10mA	X			X		X	Port B3	ADC analog input 3

4 Flash program memory

4.1 Introduction

The ST7 dual voltage High Density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization allows each sector to be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
  - Insertion in a programming tool. In this mode, all sectors including option bytes can be programmed or erased.
  - ICP (in-circuit programming). In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
  - IAP (in-application programming). In this mode, all sectors except Sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register access security system (RASS) to prevent accidental programming or erasing

4.3 Structure

The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see *Table 7*). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see *Figure 8*). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

Table 7. Sectors available in Flash devices

Flash size (Kbytes)	Available sectors
4	Sector 0
8	Sectors 0,1
> 8	Sectors 0,1, 2

5 Central processing unit

5.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

5.2 Main features

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

5.3 CPU registers

The six CPU registers shown in *Figure* are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index registers (X and Y)

In indexed addressing modes, these 8-bit registers are used to create either effective addresses or temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures (not pushed to and popped from the stack).

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (program counter low which is the LSB) and PCH (program counter high which is the MSB).

7 Interrupts

The ST7 core may be interrupted by one of two different methods: maskable hardware interrupts as listed in *Table 9* and a non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in *Figure 19*.

The maskable interrupts must be enabled clearing the I bit in order to be serviced. However, disabled interrupts may be latched and processed when they are enabled (see external interrupts subsection).

When an interrupt has to be serviced:

- Normal processing is suspended at the end of the current instruction execution.
- The PC, X, A and CC registers are saved onto the stack.
- The I bit of the CC register is set to prevent additional interrupts.
- The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to *Table 9* for vector addresses).

The interrupt service routine should finish with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

Note: As a consequence of the IRET instruction, the I bit will be cleared and the main program will resume.

Priority management

By default, a servicing interrupt cannot be interrupted because the I bit is set by hardware entering in interrupt routine.

In the case several interrupts are simultaneously pending, a hardware priority defines which one will be serviced first (see *Table 9*).

Non-maskable software interrupts

This interrupt is entered when the TRAP instruction is executed regardless of the state of the I bit. It will be serviced according to the flowchart on *Figure 19*.

Interrupts and low power mode

All interrupts allow the processor to leave the Wait low power mode. Only external and specific mentioned interrupts allow the processor to leave the Halt low power mode (refer to the “Exit from HALT“ column in *Table 9*).

External interrupts

The pins ITi/PAk and ITj/PBk (i=1,2; j= 5,6; k=4,5) can generate an interrupt when a rising edge occurs on this pin. Conversely, the ITl/PAn and ITm/PBn pins (l=3,4; m= 7,8; n=6,7) can generate an interrupt when a falling edge occurs on this pin.

Interrupt generation will occur if it is enabled with the ITiE bit (i=1 to 8) in the ITRFRE register and if the I bit of the CC is reset.

Peripheral interrupts

Different peripheral interrupt flags in the status register are able to cause an interrupt when they are active if both:

- The I bit of the CC register is cleared.
- The corresponding enable bit is set in the control register.

If any of these two conditions is false, the interrupt is latched and thus remains pending.

Clearing an interrupt request is done by one of the two following operations:

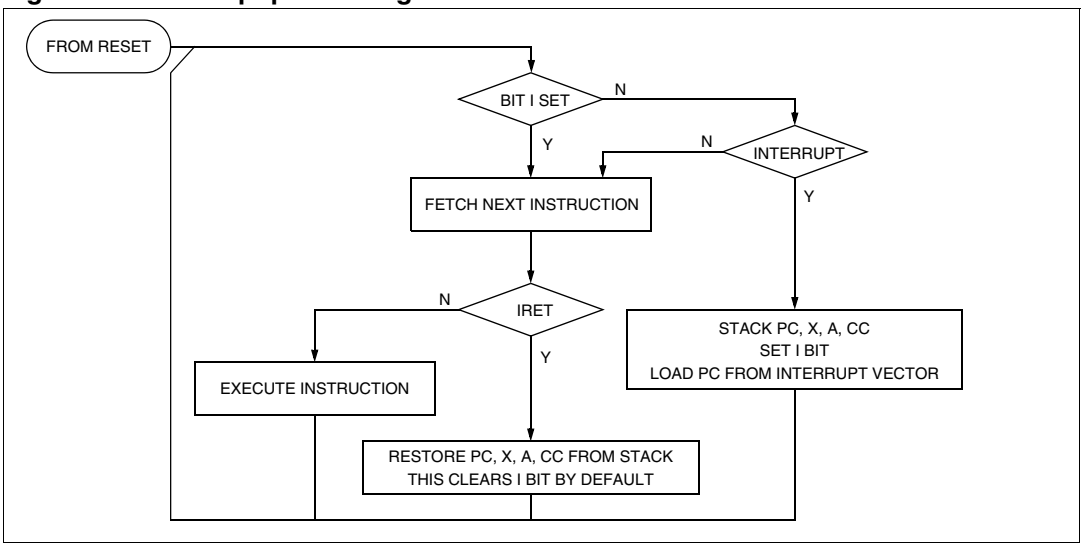
- Writing “0” to the corresponding bit in the status register.
- Accessing the status register while the flag is set followed by a read or write of an associated register.

Note: 1 The clearing sequence resets the internal latch. A pending interrupt (i.e. waiting to be enabled) will therefore be lost if the clear sequence is executed.

2 All interrupts allow the processor to leave the Wait low power mode.

3 Exit from Halt mode may only be triggered by an external interrupt on one of the ITi ports (PA4-PA7 and PB4-PB7), an end suspend mode interrupt coming from USB peripheral, or a reset.

Figure 19. Interrupt processing flowchart



9 I/O ports

9.1 Introduction

The I/O ports offer different functional modes:

- Transfer of data through digital inputs and outputs and for specific pins
- Analog signal input (ADC)
- Alternate signal input/output for the on-chip peripherals
- External interrupt generation

An I/O port consists of up to 8 pins. Each pin can be programmed independently as a digital input (with or without interrupt generation) or a digital output.

9.2 Functional description

Each port is associated to 2 main registers:

- Data register (DR)
- Data Direction register (DDR)

Each I/O pin may be programmed using the corresponding register bits in DDR register: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

Table 10. I/O pin functions

DDR	Mode
0	Input
1	Output

Input modes

The input configuration is selected by clearing the corresponding DDR register bit.

In this case, reading the DR register returns the digital value applied to the external I/O pin.

Note: 1 All the inputs are triggered by a Schmitt trigger.

2 When switching from input mode to output mode, the DR register should be written first to output the correct value as soon as the port is configured as an output.

Interrupt function

When an I/O is configured as an input with interrupt, an event on this I/O can generate an external interrupt request to the CPU. The interrupt sensitivity is given independently according to the description mentioned in the ITRFRE interrupt register.

Each pin can independently generate an interrupt request.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see interrupts section). If more than one input pin is selected simultaneously as an interrupt source, this is logically ORed. For this reason if one of the interrupt pins is tied low, the other ones are masked.

9.3.2 Port B

Table 13. Port B description

Port B	I/O		Alternate function	
	Input(1)	Output	Signal	Condition
PB0	without pull-up	push-pull	Analog input (ADC)	CH[3:0] = 000 (ADCCSR)
PB1	without pull-up	push-pull	Analog input (ADC)	CH[3:0] = 001 (ADCCSR)
			USBOE (USB output enable)(2)	USBOE =1 (MISCR)
PB2	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 010 (ADCCSR)
PB3	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 011 (ADCCSR)
PB4	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 100 (ADCCSR)
			IT5 Schmitt triggered input	IT5E = 1 (ITIFRE)
PB5	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 101 (ADCCSR)
			IT6 Schmitt triggered input	IT6E = 1 (ITIFRE)
PB6	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 110 (ADCCSR)
			IT7 Schmitt triggered input	IT7E = 1 (ITIFRE)
PB7	without pull-up	push-pull	Analog input (ADC)	CH[3:0]= 111 (ADCCSR)
			IT8 Schmitt triggered input	IT8E = 1 (ITIFRE)

1. Reset State
2. On SO24 only

Control register 2 (CR2)

Reset value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG
Read/write							

7 **OC1E** output *Compare 1 Pin Enable.*
This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in output Compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the output Compare 1 function of the timer remains active.

0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP1 pin alternate function enabled.

6 **OC2E** output *Compare 2 Pin Enable.*
This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in output Compare mode). Whatever the value of the OC2E bit, the output Compare 2 function of the timer remains active.

0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O).

1: OCMP2 pin alternate function enabled.

5 **OPM** *One Pulse mode.*

0: One Pulse mode is not active.

1: One Pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.

4 **PWM** *Pulse Width Modulation.*

0: PWM mode is not active.

1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.

[3:2] **CC[1:0]** *Clock Control.*

The timer clock mode depends on these bits (see *Table 24*).

If the external clock pin is not available, programming the external clock configuration stops the counter.

1 **IEDG2** *input Edge 2.*
This bit determines which type of level transition on the ICAP2 pin will trigger the capture.

0: A falling edge triggers the capture.

1: A rising edge triggers the capture.

0 **EXEDG** *External Clock Edge.*
This bit determines which type of level transition on the external clock pin EXTCLK will trigger the counter register.

0: A falling edge triggers the counter register.

1: A rising edge triggers the counter register.

Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see *Figure 41*).

Procedure

1. Select the M bit to define the word length.
2. Select the desired baud rate using the SCIBRR and the SCIETPR registers.
3. Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.
4. Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CC register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit or after the break frame) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CC register.

Clearing the TC bit is performed by the following software sequence:

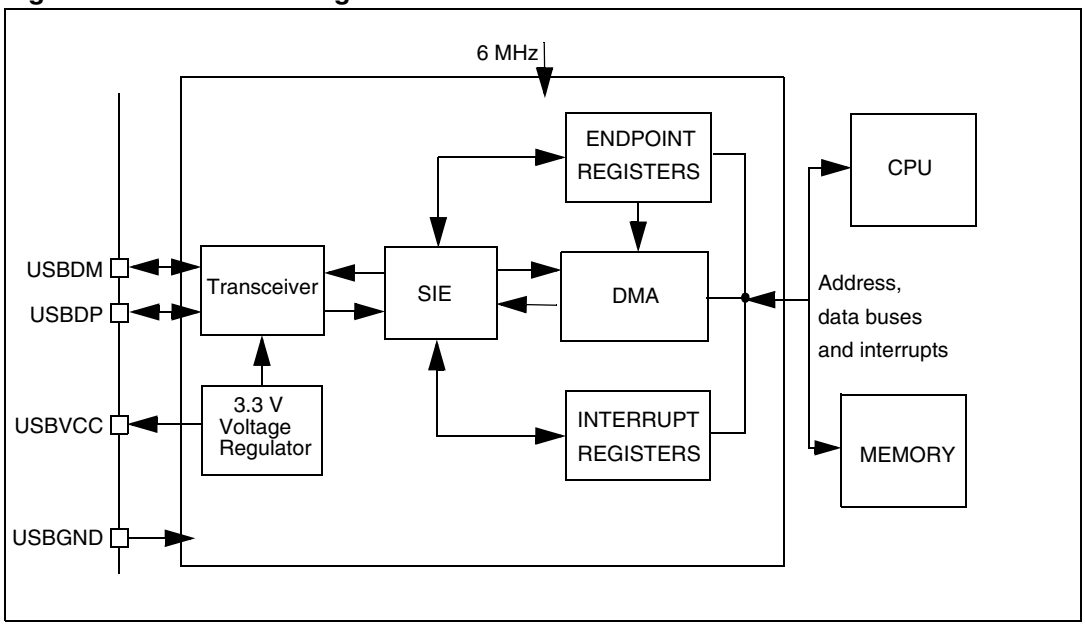
1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see *Figure 42*).

Figure 44. USB block diagram



11.4.4 Register description

DMA Address register (DMAR)

Reset value: undefined

7							0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
Read.write							

[7:0] **DA[15:8]** *DMA address bits 15-8.*

Software must write the start address of the DMA memory area whose most significant bits are given by DA15-DA6. The remaining 6 address bits are set by hardware. See the description of the IDR register and *Figure 45*.

PID register (PIDR)

Reset value: xx00 0000 (x0h)

7							0
TP3	TP2	0	0	0	RX_ SEZ	RXD	0
Read only							

[7:6] **TP[3:2]** *Token PID bits 3 & 2.*
USB token PIDs are encoded in four bits. **TP[3:2]** correspond to the variable token PID bits 3 & 2.
: PID bits 1 & 0 have a fixed value of 01.

Note: When a CTR interrupt occurs (see register ISTR) the software should read the TP3 and TP2 bits to retrieve the PID name of the token received. The USB standard defines TP bits (see Table 33).

[5:3] Reserved. Forced by hardware to 0.

2 **RX_SEZ** *Received single-ended zero*
This bit indicates the status of the RX_SEZ transceiver output.
0: No SE0 (single-ended zero) state
1: USB lines are in SE0 (single-ended zero) state

1 **RXD** *Received data*
0: No K-state
1: USB lines are in K-state
This bit indicates the status of the RXD transceiver output (differential receiver output).
If the environment is noisy, the RX_SEZ and RXD bits can be used to secure the application. By interpreting the status, software can distinguish a valid End Suspend event from a spurious wakeup due to noise on the external USB line. A valid End Suspend is followed by a Resume or Reset sequence. A Resume is indicated by RXD=1, a Reset is indicated by RX_SEZ=1.

0 Reserved. Forced by hardware to 0.

Table 33. TP bit definition

TP3	TP2	PID Name
0	0	OUT
1	0	IN
1	1	SETUP

11.5 I²C bus interface

11.5.1 Introduction

The I²C bus interface serves as an interface between the microcontroller and the serial I²C bus. It provides both multimaster and slave functions, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It supports fast I²C mode (400 kHz).

11.5.2 Main features

- Parallel-bus/I²C protocol converter
- Multimaster capability
- 7-bit addressing
- Transmitter/receiver flag
- End-of-byte transmission flag
- Transfer problem detection

I²C master features

- Clock generation
- I²C bus busy flag
- Arbitration Lost Flag
- End of byte transmission flag
- Transmitter/Receiver Flag
- Start bit detection flag
- Start and Stop generation

I²C slave features

- Stop bit detection
- I²C bus busy flag
- Detection of misplaced start or stop condition
- Programmable I²C Address detection
- Transfer problem detection
- End-of-byte transmission flag
- Transmitter/Receiver flag

11.5.3 General description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and vice versa, using either an interrupt or polled handshake. The interrupts are enabled or disabled by software. The interface is connected to the I²C bus by a data pin (SDAI) and by a clock pin (SCLI). It can be connected both with a standard I²C bus and a Fast I²C bus. This selection is made by software.

3 **BTF** *Byte transfer finished.*
This bit is set by hardware as soon as a byte is correctly received or transmitted with interrupt generation if ITE=1. It is cleared by software reading SR1 register followed by a read or write of DR register. It is also cleared by hardware when the interface is disabled (PE=0).

Following a byte transmission, this bit is set after reception of the acknowledge clock pulse. In case an address byte is sent, this bit is set only after the EV6 event (See *Figure 48*). BTF is cleared by reading SR1 register followed by writing the next byte in DR register.

Following a byte reception, this bit is set after transmission of the acknowledge clock pulse if ACK=1. BTF is cleared by reading SR1 register followed by reading the byte from DR register.

The SCL line is held low while BTF=1.

0: Byte transfer not done

1: Byte transfer succeeded

2 **ADSL** *Address matched (Slave mode).* This bit is set by hardware as soon as the received slave address matched with the OAR register content or a general call is recognized. An interrupt is generated if ITE=1. It is cleared by software reading SR1 register or by hardware when the interface is disabled (PE=0).

The SCL line is held low while ADSL=1.

0: Address mismatched or not received

1: Received address matched

1 **M/SL** *Master/Slave.*
This bit is set by hardware as soon as the interface is in Master mode (writing START=1). It is cleared by hardware after detecting a Stop condition on the bus or a loss of arbitration (ARLO=1). It is also cleared when the interface is disabled (PE=0).

0: Slave mode

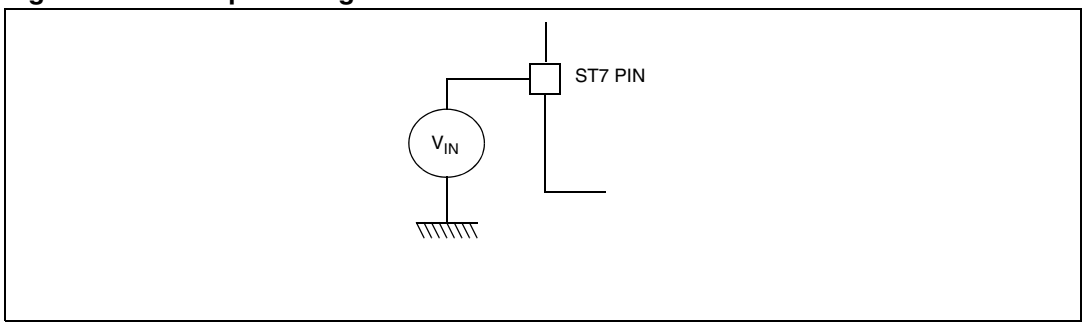
1: Master mode

0 **SB** *Start bit (Master mode).*
This bit is set by hardware as soon as the Start condition is generated (following a write START=1). An interrupt is generated if ITE=1. It is cleared by software reading SR1 register followed by writing the address byte in DR register. It is also cleared by hardware when the interface is disabled (PE=0).

0: No Start condition

1: Start condition generated

Figure 53. Pin input voltage



13.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

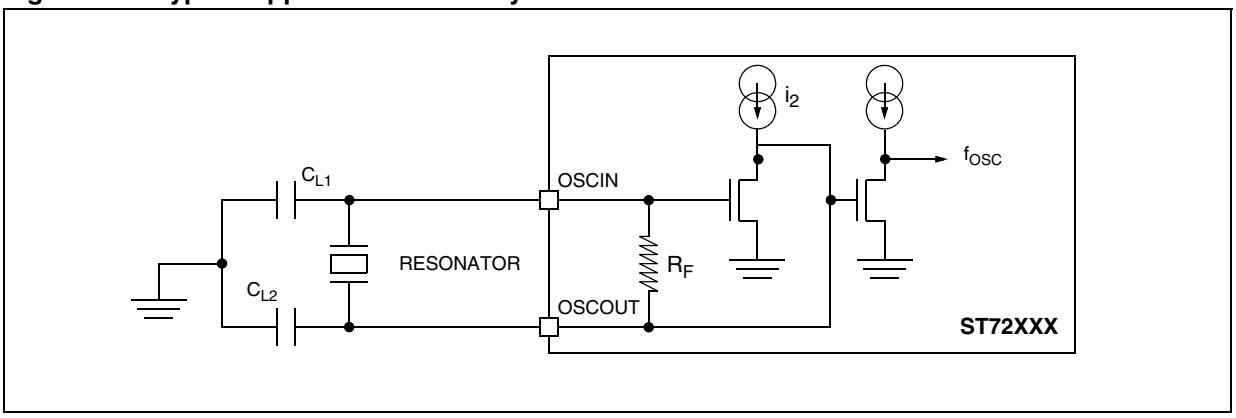
Note: Directly connecting the $\overline{RESET}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7 kΩ for $\overline{RESET}$, 10 kΩ for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration.

Table 55. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	6.0	V
V_{IN} (1)(2)	Input voltage on true open drain pins	V_{SS}-0.3 to 6.0	
	Input voltage on any other pin	V_{SS}-0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body model)	*Section 13.7.3*	

1. Directly connecting the RESET and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7 kΩ for RESET, 10 kΩ for I/Os). Unused I/O pins must be tied in the same way to VDD or VSS according to their reset configuration.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.

Figure 58. Typical application with a crystal resonator



13.6 Memory characteristics

Subject to general operating conditions for f_{CPU}, and T_A unless otherwise specified.

Table 64. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or RESET)	2.0	-	-	V

1. Guaranteed by design. Not tested in production.

13.6.1 Flash memory

Operating Conditions: f_{CPU} = 8 MHz.

Table 65. Dual voltage Flash memory(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CPU}	Operating frequency	Read mode	-	-	8	MHz
		Write / Erase mode, T_A=25 °C	-	-	8	
V_{PP}	Programming voltage	4.0 V ≤V_{DD} ≤ 5.5 V	11.4	-	12.6	V
I_{PP}	V_{PP} current	Write / Erase	-	30	-	mA
t_{VPP}	Internal V_{PP} stabilization time		-	10	-	µs
t_{RET}	Data retention	T_A ≤ 5 5°C	40	-	-	years
N_{RW}	Write/erase cycles	T_A=25 °C	100	-	-	cycles

1. Refer to the Flash programming reference manual for the typical HDFlash programming and erase timing values.

Figure 61. Typ. I_{PU} vs. V_{DD}

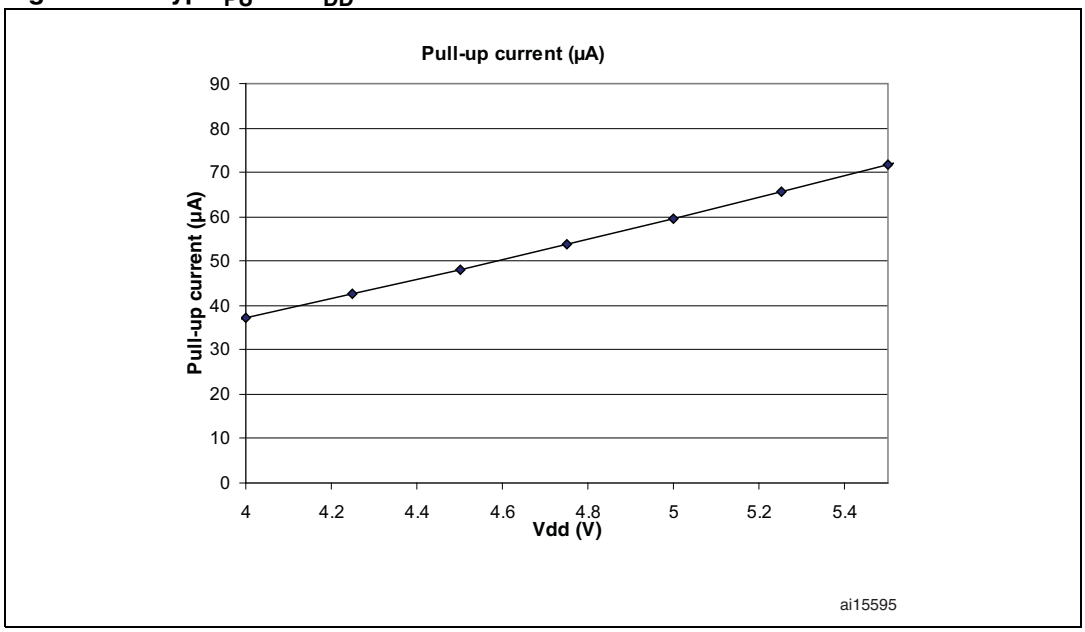


Figure 62. Typ. R_{PU} vs. V_{DD}

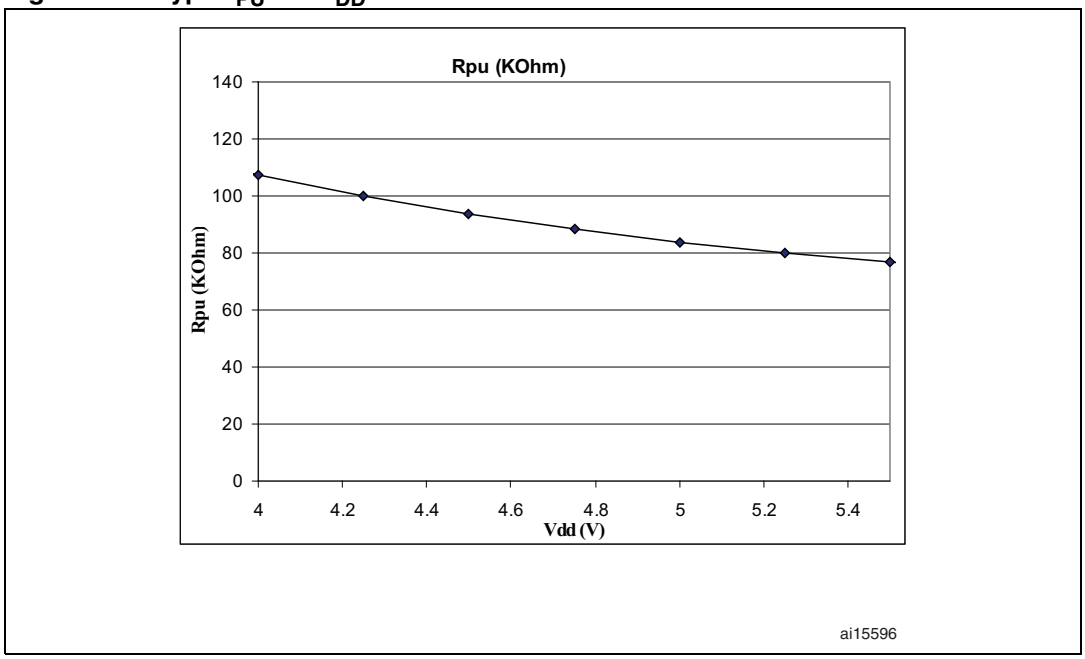
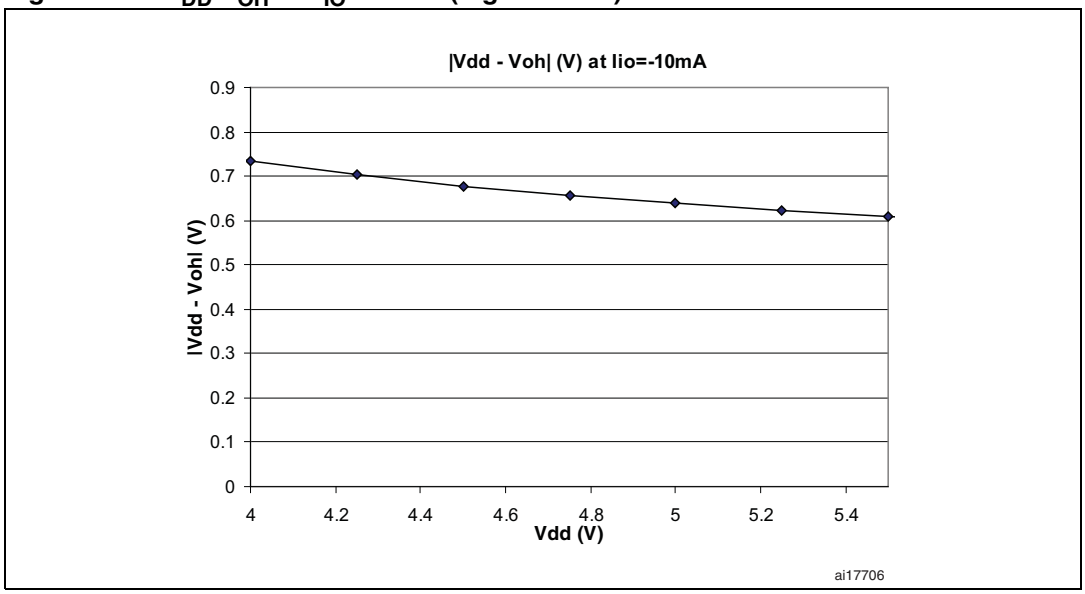


Figure 72. $|V_{DD}-V_{OH}|$ @ I_{IO}=10 mA (high current)



13.9 Control pin characteristics

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 72. Asynchronous $\overline{\text{RESET}}$ pin

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	Input high level voltage			0.7xV_{DD}	-	V_{DD}	V
V_{IL}	Input low voltage			V_{SS}	-	0.3xV_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis(1)			-	400	-	mV
V_{OL}	Output low level voltage(2)	V_{DD}=5 V	I_{IO}=5 mA	-	-	0.8	V
			I_{IO}=7.5 mA	-	-	1.3	
R_{ON}	Weak pull-up equivalent resistor (3)	V_{IN}=V_{SS}	V_{DD}=5 V	50	80	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources		-	6 30	-	1/f_{SFOSC} µs
$t_{h(RSTL)in}$	External reset pulse hold time(4)			5	-	-	µs

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
2. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 13.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.
4. To guarantee the reset of the device, a minimum pulse has to be applied to $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

14.2 Thermal characteristics

Table 85. Thermal characteristics

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) SDIP32 SO34 SO24 LQFP48 QFN40	 60 75 70 80 34	°C/W
P_D	Power dissipation(1)	500	mW
T_{Jmax}	Maximum junction temperature(2)	150	°C

1. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$. The power dissipation of an application can be defined by the user with the formula: $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} the port power dissipation depending on the ports used in the application.
2. The maximum chip-junction temperature is based on technology characteristics.

14.3 Soldering and glueability information

Recommended glue for SMD plastic packages dedicated to molding compound with silicone:

- Heraeus: PD945, PD955
- Loctite: 3615, 3298

16.5 Halt mode power consumption with ADC on

Description

If the A/D converter is being used when Halt mode is entered, the power consumption in Halt mode may exceed the maximum specified in the datasheet.

Workaround

Switch off the ADC by software (ADON=0) before executing a HALT instruction.

16.6 SCI wrong BREAK duration

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 20 bits instead of 10 bits if M=0
- 22 bits instead of 11 bits if M=1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may generate one break more than expected.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (fCPU=8MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

1. Disable interrupts
2. Reset and Set TE (IDLE request)
3. Set and Reset SBK (Break Request)
4. Re-enable interrupts