Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-BFQFP
Supplier Device Package	128-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2633f25iv

H8S/2633 Group Manuals:

Document Title	Document No.
H8S/2633 Group Hardware Manual	This manual
H8S/2600 Series, H8S/2000 Series Software Manual	REJ09B0139

Users Manuals for Development Tools:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimized Linkage Editor User's Manual	REJ10J2039
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B0211
High-performance Embedded Workshop User's Manual	REJ10J2169

Application Notes:

Document Title	Document No.
H8S Family Technical Q & A	REJ05B0397

Item	Page	Revision (See Manual for Details)
18.4 Usage Notes	893	Table amended

Table 18.8 I^2C Bus Timing (with Maximum Influence of t_{Sr}/t_{Sf})

Item	t_{cyc} Indication		t_{Sr}/t_{Sf} Influence (Max.)	I^2C Bus Specification (Min.)	Time Indication (at Maximum Transfer Rate) [ns] ϕ = 5 MHz	ϕ = 8 MHz	ϕ = 10 MHz	ϕ = 16 MHz	ϕ = 20 MHz	ϕ = 25 MHz	ϕ = 28 MHz
t_{SDASO} (master)	$1t_{SCLLO}$ *3 $-3t_{cyc}$ $(-t_{Sr})$	Standard mode	–1000	250	3100	3325	3400	3513	3550	3580	3593
		High-speed mode	–300	100	400	625	700	813	850	880	893
t_{SDASO} (slave)	$1t_{SCLL}$ *3 $-12t_{cyc}$ *2 $(-t_{Sr})$	Standard mode	–1000	250	3100	3325	3400	3513	3550	3580	3593
		High-speed mode	–300	100	400	625	700	813	850	880	893

Notes amended

Notes 2. Value when the IICX bit is set to 1. When the IICX bit is cleared to 0, the value is $(1t_{SCLL} – 6t_{cyc})$.

3. Calculated using the I^2C bus specification values (standard mode: 4700 ns min.; high-speed mode: 1300 ns min.).

902 Description added

- Notes on Wait Operation in Master Mode

  During master mode operation using the wait function, when the interrupt flag IRIC bit is cleared from 1 to 0 between the falling edge of the 7th clock cycle and the falling edge of the 8th clock cycle, in some cases no wait is inserted after the falling edge of the 8th clock cycle and the clock pulse of the 9th clock cycle is output continuously.

  Observe the following with regard to clearing the IRIC flag while using the wait function.

  At the rising edge of the 9th clock cycle, set the IRIC flag to 1 and then clear it to zero before the rising edge of the 1st clock cycle (while the value of the BC2 to BC0 counter value is 2 or greater).

  If clearing of the IRIC flag is delayed by interrupt processing or the like and the BC counter value reaches 1 or 0, confirm that the SCL pin state is low-level after the BC2 to BC0 counter has reached 0 and then clear the IRIC flag. (See figure 18.28.)

Figure 18.28 Timing of IRIC Flag Clearing During Wait Operation

Figure added

Bit 3	Bit 2	Bit 1	Bit 0	
AE3	**AE2**	**AE1**	**AE0**	**Description**
0	0	0	0	A8–A23 address output disabled (Initial value*)
			1	A8 address output enabled; A9–A23 address output disabled
		1	0	A8, A9 address output enabled; A10–A23 address output disabled
			1	A8–A10 address output enabled; A11–A23 address output disabled
	1	0	0	A8–A11 address output enabled; A12–A23 address output disabled
			1	A8–A12 address output enabled; A13–A23 address output disabled
		1	0	A8–A13 address output enabled; A14–A23 address output disabled
			1	A8–A14 address output enabled; A15–A23 address output disabled
1	0	0	0	A8–A15 address output enabled; A16–A23 address output disabled
			1	A8–A16 address output enabled; A17–A23 address output disabled
		1	0	A8–A17 address output enabled; A18–A23 address output disabled
			1	A8–A18 address output enabled; A19–A23 address output disabled
	1	0	0	A8–A19 address output enabled; A20–A23 address output disabled
			1	A8–A20 address output enabled; A21–A23 address output disabled (Initial value*)
		1	0	A8–A21 address output enabled; A22, A23 address output disabled
			1	A8–A23 address output enabled

Note: * In expanded mode with ROM, bits AE3 to AE0 are initialized to B'0000.
In ROMless expanded mode, bits AE3 to AE0 are initialized to B'1101.
Address pins A0 to A7 are made address outputs by setting the corresponding DDR bits to 1.

Name	Symbol	I/O	Function
Lower column strobe*	$\overline{\text{LCAS}}$*	Output	DRAM lower column address strobe signal*
Wait	$\overline{\text{WAIT}}$	Input	Wait request signal when accessing external 3-state access space.
Bus request	$\overline{\text{BREQ}}$	Input	Request signal that releases bus to external device.
Bus request acknowledge	$\overline{\text{BACK}}$	Output	Acknowledge signal indicating that bus has been released.
Bus request output	$\overline{\text{BREQO}}$	Output	External bus request signal used when internal bus master accesses external space when external bus is released.

Note: * This function is not available in the H8S/2695.

7.1.4 Register Configuration

Table 7.2 summarizes the registers of the bus controller.

Table 7.2 Bus Controller Registers

			Initial Value		
Name	Abbreviation	R/W	Power-On Reset	Manual Reset	Address*1
Bus width control register	ABWCR	R/W	H'FF/H'00*2	Retained	H'FED0
Access state control register	ASTCR	R/W	H'FF	Retained	H'FED1
Wait control register H	WCRH	R/W	H'FF	Retained	H'FED2
Wait control register L	WCRL	R/W	H'FF	Retained	H'FED3
Bus control register H	BCRH	R/W	H'D0	Retained	H'FED4
Bus control register L	BCRL	R/W	H'08	Retained	H'FED5
Pin function control register	PFCR	R/W	H'0D/H'00	Retained	H'FDEB
Memory control register	MCR*3	R/W	H'00	Retained	H'FED6
DRAM control register	DRAMCR*3	R/W	H'00	Retained	H'FED7
Refresh timer counter	RTCNT*3	R/W	H'00	Retained	H'FED8
Refresh time constant register	RTCOR*3	R/W	H'FF	Retained	H'FED9

Notes: 1. Lower 16 bits of the address.
2. Determined by the MCU operating mode.
3. This function is not available in the H8S/2695.

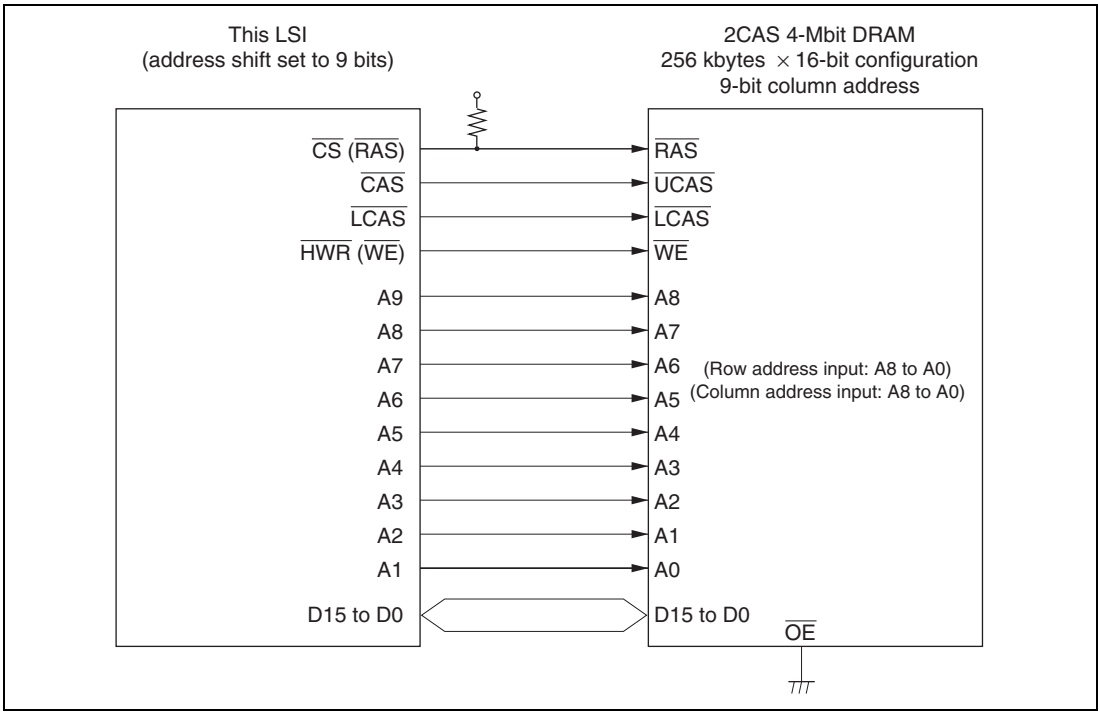

Figure 7.20 High-speed Page Mode DRAM

Port	Description	Pins	Mode 4	Mode 5	Mode 6	Mode 7
Port E	• 8-bit I/O port • Built-in MOS input pull-up	PE7/D7 PE6/D6 PE5/D5 PE4/D4 PE3/D3 PE2/D2 PE1/D1 PE0 /D0	In 8-bit-bus mode: I/O port In 16-bit-bus mode: data bus input/output			I/O port
Port F	• 8-bit I/O port	PF7/φ	When DDR = 0: input port When DDR = 1 (after reset): φ output			When DDR = 0 (after reset): input port When DDR = 1: φ output
		PF6 /$\overline{\text{AS}}$/$\overline{\text{LCAS}}$ PF5 /$\overline{\text{RD}}$ PF4 /$\overline{\text{HWR}}$ PF3/$\overline{\text{LWR}}$/$\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$	$\overline{\text{RD}}$, $\overline{\text{HWR}}$, $\overline{\text{LWR}}$ outputs $\overline{\text{ADTRG}}$, $\overline{\text{IRQ3}}$ input When LCASS = 0: $\overline{\text{AS}}$ output When RMTS2 to RMTS0 = B'001 to B'011, CW2 = 0, and LCASS = 1: $\overline{\text{LCAS}}$ output			I/O port $\overline{\text{ADTRG}}$, $\overline{\text{IRQ3}}$ input
		PF2/$\overline{\text{LCAS}}$/$\overline{\text{WAIT}}$/$\overline{\text{BREQO}}$	When WAITE = 0 and BREQOE = 0 (after reset): I/O port When WAITE = 1 and BREQOE = 0: $\overline{\text{WAIT}}$ input When WAITE = 0 and BREQOE = 1: $\overline{\text{BREQO}}$ input When RMTS2 to RMTS0 = B'001 to B'011, CW2 = 0, and LCASS = 0: $\overline{\text{LCAS}}$ output			I/O port
		PF1/$\overline{\text{BACK}}$/BUZZ PF0/$\overline{\text{BREQ}}$/$\overline{\text{IRQ2}}$	When BRLE = 0 (after reset): I/O port When BRLE = 1: $\overline{\text{BREQ}}$ input, $\overline{\text{BACK}}$ output BUZZ output, $\overline{\text{IRQ2}}$ input			BUZZ output $\overline{\text{IRQ2}}$ input I/O port

10A.8 Port B

10A.8.1 Overview

Port B is an 8-bit I/O port. Port B pins also function as TPU I/O pins (TIOCA3, TIOCB3, TIOCC3, TIOCD3, TIOCA4, TIOCB4, TIOCA5, and TIOCB5) and as address outputs; the pin functions change according to the operating mode.

Port B has a built-in MOS input pull-up function that can be controlled by software.

Figure 10A.7 shows the port B pin configuration.

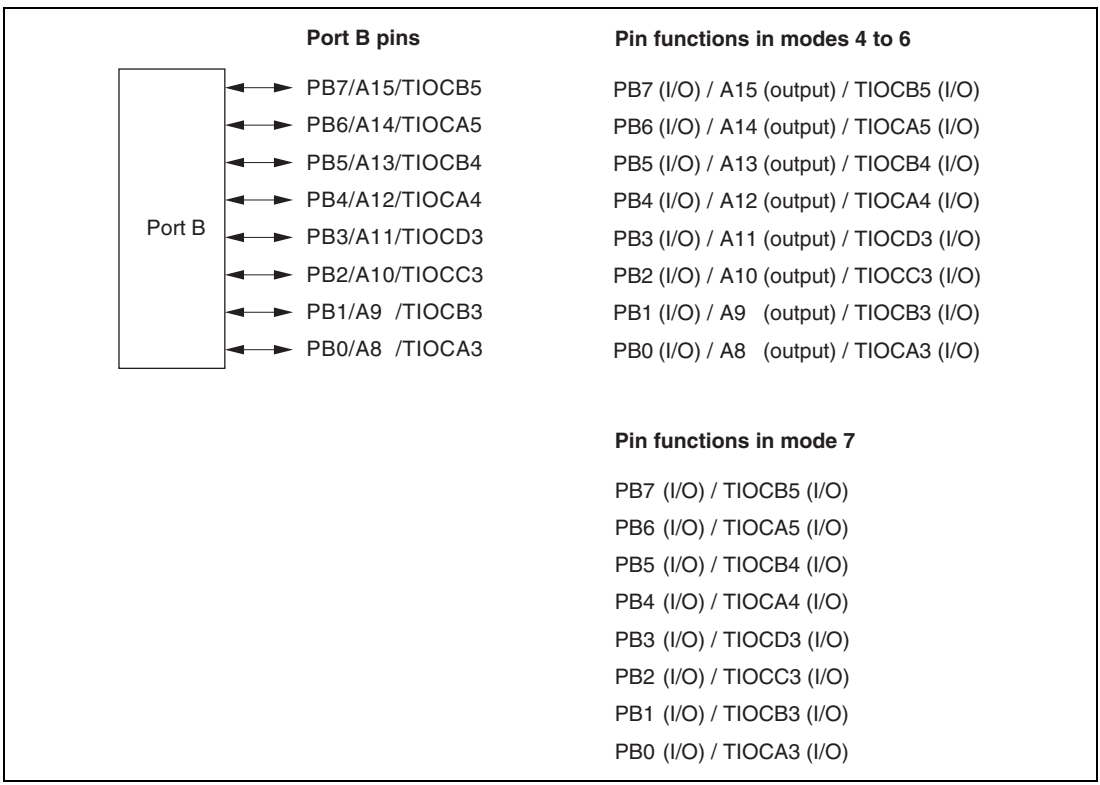

Figure 10A.7 Port B Pin Functions

10A.8.4 MOS Input Pull-Up Function

Port B has a built-in MOS input pull-up function that can be controlled by software. MOS input pull-up can be specified as on or off on an individual bit basis.

In modes 4 to 6, if a pin is in the input state in accordance with the settings in PFCR, in the TPU's TIOR, and in DDR, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

In mode 7, if a pin is in the input state in accordance with the settings in the TPU's TIOR and in DDR, setting the corresponding PBPCR bit to 1 turns on the MOS input pull-up for that pin.

The MOS input pull-up function is in the off state after a power-on reset, and in hardware standby mode. The prior state is retained by a manual reset or in software standby mode.

Table 10A.15 summarizes the MOS input pull-up states.

Table 10A.15 MOS Input Pull-Up States (Port B)

Pin States	Power-On Reset	Hardware Standby Mode	Manual Reset	Software Standby Mode	In Other Operations
Address output or TPU output	OFF	OFF	OFF	OFF	OFF
Other than above			ON/OFF	ON/OFF	ON/OFF

Legend:
OFF: MOS input pull-up is always off.
ON/OFF: On when PBDDR = 0 and PBPCR = 1; otherwise off.

10B.2.3 Pin Functions

Port 1 pins also function as TPU I/O pins (TCLKA, TCLKB, TCLKC, TCLKD, TIOCA0, TIOCB0, TIOCC0, TIOCD0, TIOCA1, TIOCB1, TIOCA2, and TIOCB2), external interrupt input pins ($\overline{IRQ0}$ and $\overline{IRQ1}$), and address bus output pins (A23 to A20). Port 1 pin functions are shown in table 10B.3.

Table 10B.3 Port 1 Pin Functions

Pin	Selection Method and Pin Functions
P17/TIOCB2/ TCLKD	The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOB3 to IOB0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), bits TPSC2 to TPSC0 in TCR0 and TCR5, and bit P17DDR.

TPU Channel 2 Setting	Table Below (1)	Table Below (2)	
P17DDR	—	0	1
Pin function	TIOCB2 output	P17 input	P17 output
		TIOCB2 input*1	
	TCLKD input*2		

Notes: 1. TIOCB2 input when MD3 to MD0 = B'0000 or B'01xx, and IOB3 = 1.
2. TCLKD input when the setting for either TCR0 or TCR5 is: TPSC2 to TPSC0 = B'111.
TCLKD input when channels 2 and 4 are set to phase counting mode.

TPU Channel 2 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000, B'01xx		B'0010	B'0011		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	—	B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	—	PWM mode 2 output	—

x: Don't care

Port C Data Register (PCDR)

Bit	:	7	6	5	4	3	2	1	0
		PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCDR is an 8-bit readable/writable register that stores output data for the port C pins (PC7 to PC0).

PCDR is initialized to H'00 by a power-on reset, and in hardware standby mode. It retains its prior state by a manual reset or in software standby mode.

Port C Register (PORTC)

Bit	:	7	6	5	4	3	2	1	0
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins PC7 to PC0.

PORTC is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port C pins (PC7 to PC0) must always be performed on PCDR.

If a PORTC read is performed while PCDDR bits are set to 1, the PCDR values are read. If a PORTC read is performed while PCDDR bits are cleared to 0, the pin states are read.

After a power-on reset and in hardware standby mode, PORTC contents are determined by the pin states, as PCDDR and PCDR are initialized. PORTC retains its prior state by a manual reset or in software standby mode.

13.4 Interrupts

13.4.1 Interrupt Sources and DTC Activation

(The H8S/2695 does not have a DTC function or an 8-bit timer)

There are three 8-bit timer interrupt sources: CMIA, CMIB, and OVI. Their relative priorities are shown in table 13.3. Each interrupt source is set as enabled or disabled by the corresponding interrupt enable bit in TCR, and independent interrupt requests are sent for each to the interrupt controller. It is also possible to activate the DTC by means of CMIA and CMIB interrupts.

Table 13.3 8-Bit Timer Interrupt Sources

Channel	Interrupt Source	Description	DTC Activation	Priority
0	CMIA0	Interrupt by CMFA	Possible	High
	CMIB0	Interrupt by CMFB	Possible	
	OVI0	Interrupt by OVF	Not possible	
1	CMIA1	Interrupt by CMFA	Possible	
	CMIB1	Interrupt by CMFB	Possible	
	OVI1	Interrupt by OVF	Not possible	
2	CMIA2	Interrupt by CMFA	Possible	
	CMIB2	Interrupt by CMFB	Possible	
	OVI2	Interrupt by OVF	Not possible	
3	CMIA3	Interrupt by CMFA	Possible	
	CMIB3	Interrupt by CMFB	Possible	
	OVI3	Interrupt by OVF	Not possible	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

13.4.2 A/D Converter Activation

The A/D converter can be activated only by channel 0 compare match A.

If the ADTE bit in TCSR0 is set to 1 when the CMFA flag is set to 1 by the occurrence of channel 0 compare match A, a request to start A/D conversion is sent to the A/D converter. If the 8-bit timer conversion start trigger has been selected on the A/D converter side at this time, A/D conversion is started.

The FSX bit also specifies whether or not SARX slave address recognition is performed in slave mode. For details, see the description of the FS bit in SAR.

18.2.4 I²C Bus Mode Register (ICMR)

Bit	:	7	6	5	4	3	2	1	0
		MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ICMR is an 8-bit readable/writable register that selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the master mode transfer clock frequency and the transfer bit count. ICMR is assigned to the same address as SAR. ICMR can be written and read only when the ICE bit is set to 1 in ICCR.

ICMR is initialized to H'00 by a reset and in hardware standby mode.

Bit 7—MSB-First/LSB-First Select (MLS): Selects whether data is transferred MSB-first or LSB-first.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side when MLS = 0, and toward the LSB side when MLS = 1. Receive data bits read from the LSB side should be treated as valid when MLS = 0, and bits read from the MSB side when MLS = 1.

Do not set this bit to 1 when the I²C bus format is used.

Bit 7

MLS	Description	
0	MSB-first	(Initial value)
1	LSB-first	

Bit 6—Wait Insertion Bit (WAIT): Selects whether to insert a wait between the transfer of data and the acknowledge bit, in master mode with the I²C bus format. When WAIT is set to 1, after the fall of the clock for the final data bit, the IRIC flag is set to 1 in ICCR, and a wait state begins (with SCL at the low level). When the IRIC flag is cleared to 0 in ICCR, the wait ends and the acknowledge bit is transferred. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted.

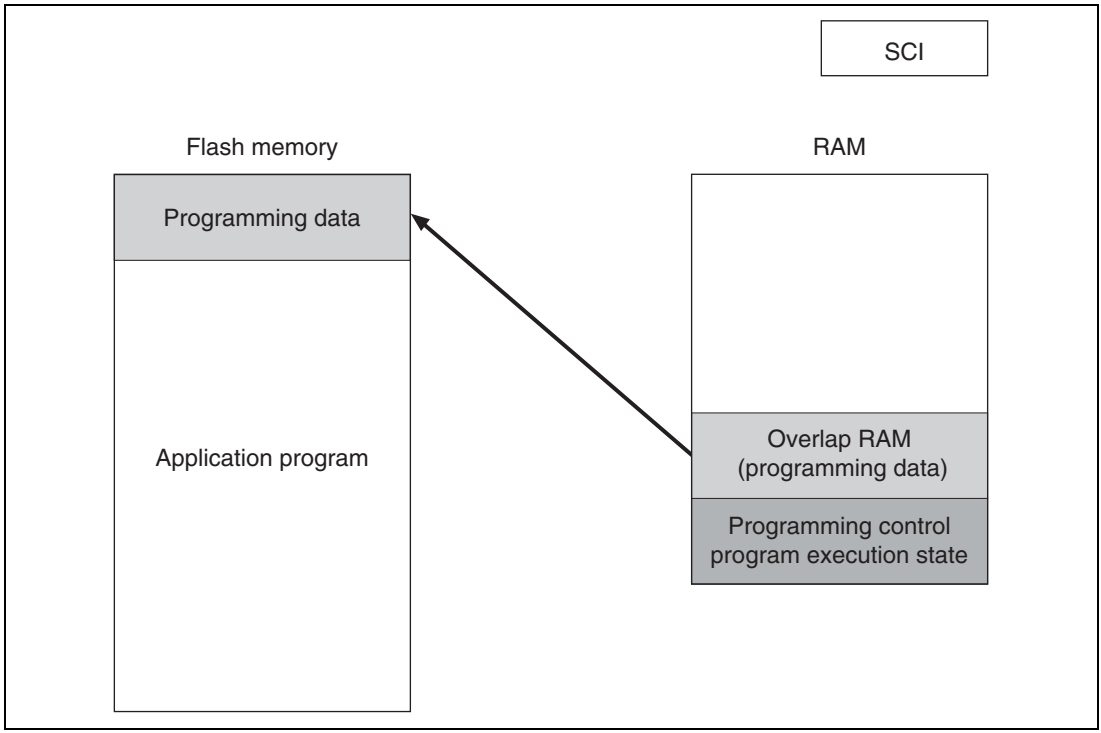

Figure 22.5 Writing Overlap RAM Data in User Program Mode

22.4.6 Differences between Boot Mode and User Program Mode

Table 22.4 Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Erase/erase-verify Program/program-verify Emulation

Note: * To be provided by the user, in accordance with the recommended algorithm.

External Clock: Table 23A.4 and figure 23A.7 show the input conditions for the external clock.

Table 23A.4 External Clock Input Conditions

		V_{cc} = 3.0 V to 3.6 V, PV_{cc} = 3.0 V to 5.5 V		V_{cc} = 3.0 V to 3.6 V, PV_{cc} = 5.0 V ±10%			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
External clock input low pulse width	t_{EXL}	20	—	15	—	ns	Figure 23A.7
External clock input high pulse width	t_{EXH}	20	—	15	—	ns	
External clock rise time	t_{EXr}	—	10	—	5	ns	
External clock fall time	t_{EXf}	—	10	—	5	ns	

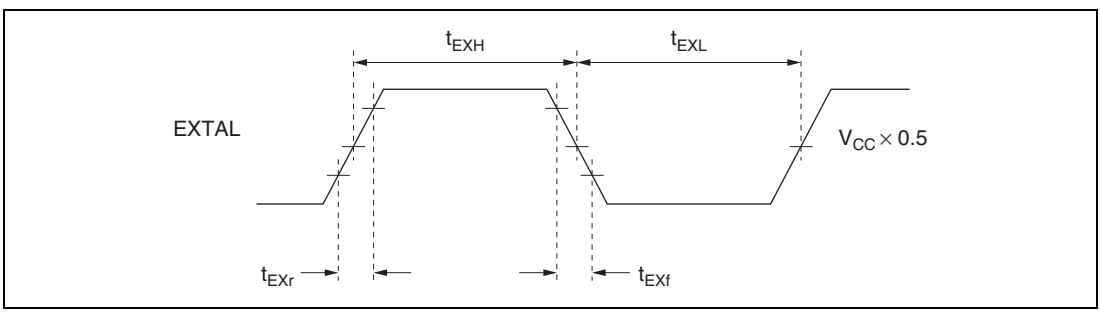

Figure 23A.7 External Clock Input Timing

23B.2 Register Descriptions

23B.2.1 System Clock Control Register (SCKCR)

Bit	:	7	6	5	4	3	2	1	0
		PSTOP	—	—	—	STCS	SCK2	SCK1	SCK0
Initial value:		0	0	0	0	0	0	0	0
R/W	:	R/W	—	—	—	R/W	R/W	R/W	R/W

SCKCR is an 8-bit readable/writable register that performs ϕ clock output control, selection of operation when the PLL circuit frequency multiplication factor is changed, and medium-speed mode control.

SCKCR is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit 7—ϕ Clock Output Disable (PSTOP): Controls ϕ output.

	Description			
Bit 7 PSTOP	**High-Speed Mode, Medium-Speed Mode, Subactive Mode**	**Sleep Mode Subsleep Mode**	**Software Standby Mode, Watch Mode*, Direct Transitions***	**Hardware Standby Mode**
0	ϕ output (initial value)	ϕ output	Fixed high	High impedance
1	Fixed high	Fixed high	Fixed high	High impedance

Note: * This function is not available in the H8S/2695.

Bits 6 to 4—Reserved: These bits are always read as 0 and cannot be modified.

Bit 3—Frequency Multiplication Factor Switching Mode Select (STCS): Selects the operation when the PLL circuit frequency multiplication factor is changed.

Bit 3 STCS	**Description**
0	Specified multiplication factor is valid after transition to software standby mode, watch mode, and subactive mode (Initial value)
1	Specified multiplication factor is valid immediately after STC bits are rewritten

24.11 Direct Transitions (This function is not available in the H8S/2695)

24.11.1 Overview of Direct Transitions

There are three modes, high-speed, medium-speed, and subactive, in which the CPU executes programs. When a direct transition is made, there is no interruption of program execution when shifting between high-speed and subactive modes. Direct transitions are enabled by setting the LPWRCR DTON bit to 1, then executing the SLEEP instruction. After a transition, direct transition interrupt exception processing starts.

(1) Direct Transitions from High-Speed Mode to Subactive Mode

Execute the SLEEP instruction in high-speed mode when the SBYCR SSBY bit = 1, LPWRCR LSON bit = 1, and DTON bit = 1, and TSCR (WDT1) PSS bit = 1 to make a transition to subactive mode.

(2) Direct Transitions from Subactive Mode to High-Speed Mode

Execute the SLEEP instruction in subactive mode when the SBYCR SSBY bit = 1, LPWRCR LSON bit = 0, and DTON bit = 1, and TSCR (WDT1) PSS bit = 1 to make a direct transition to high-speed mode after the time set in SBYCR STS2 to STS0 has elapsed.

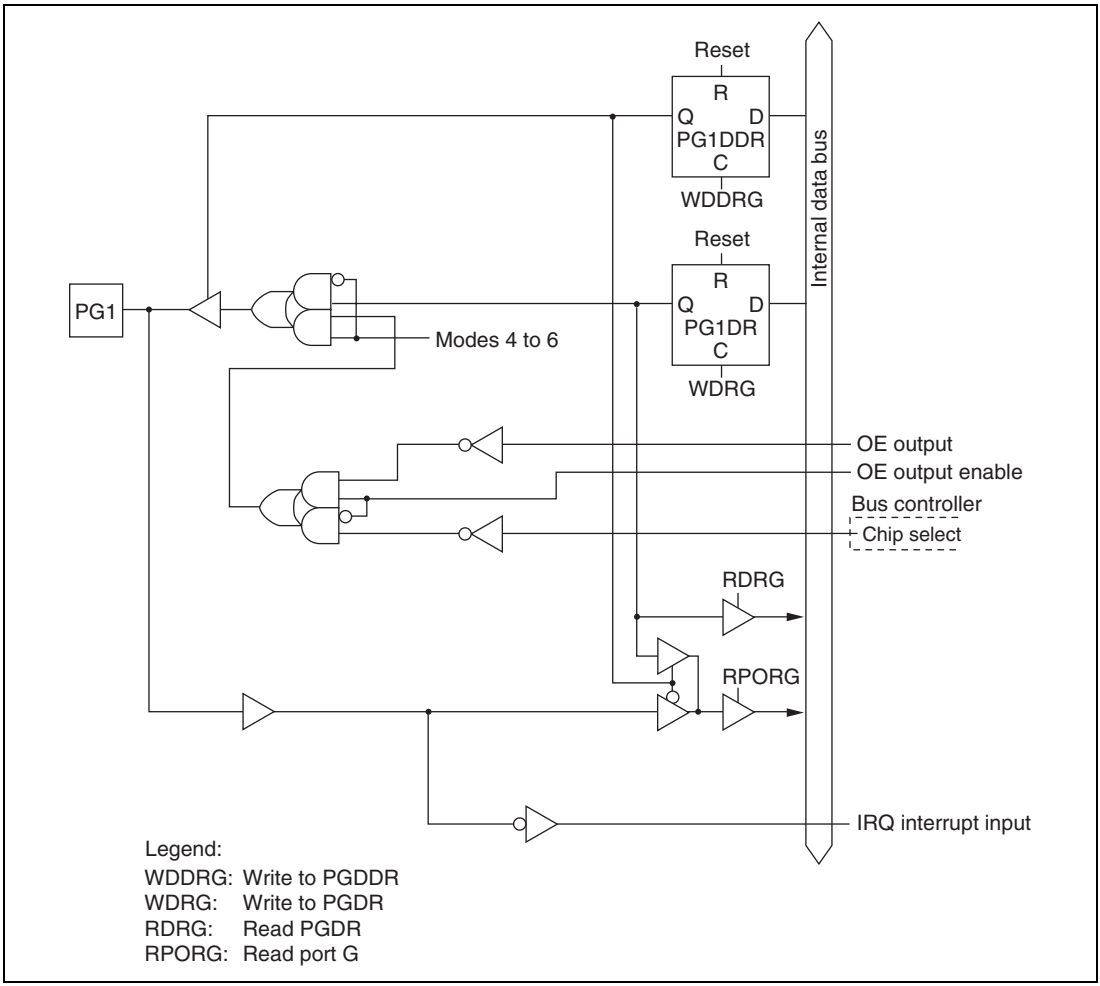

Figure C.12 (b) Port G Block Diagram (Pin PG1)

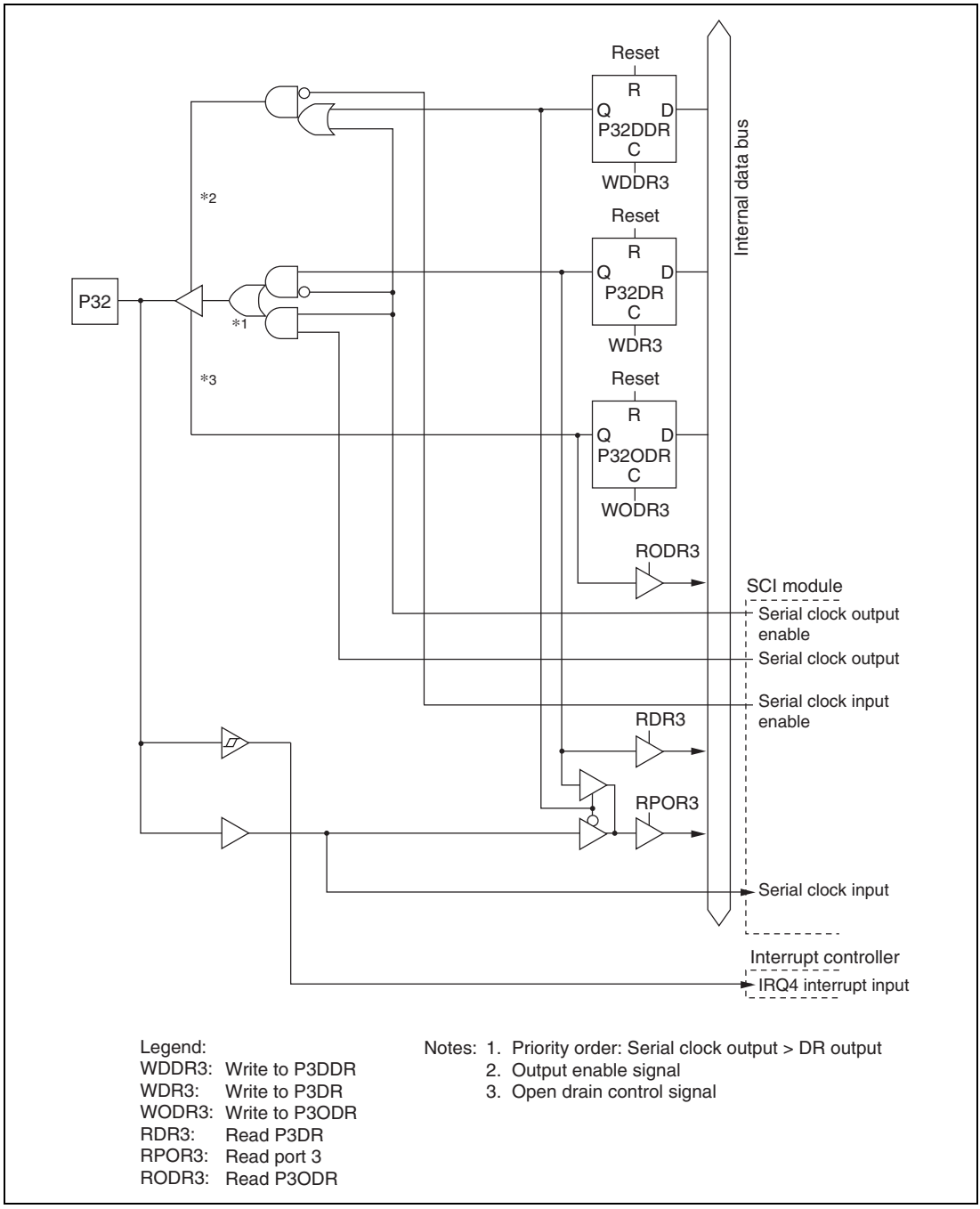

Figure C.14 (c) Port 3 Block Diagram (Pin P32)

Port Name Pin Name	MCU Operating Mode	Power-On Reset	Manual Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
PG3/$\overline{CS1}$ PG2/$\overline{CS2}$	4 to 6	T	kept	T	[DDR = 1, OPE = 0] T [DDR = 1, OPE = 1] H [DDR = 0] T	T	[DDR = 0] Input port [DDR = 1] $\overline{CS2}$ to $\overline{CS1}$
	7	T	kept	T	kept	kept	I/O port
PG1/$\overline{CS3}$/ $\overline{OE}$/$\overline{IRQ7}$	4 to 6	T	kept	T	[DDR = 1, OPE = 0] T [DDR = 1, OPE = 1] H [DDR = 0] T	T	[DDR = 0] Input port [OE = 0, DDR = 1] $\overline{CS3}$ [OE = 1, DDR = 1] $\overline{OE}$
	7	T	kept	T	kept	kept	I/O port
PG0/$\overline{CAS}$/ $\overline{IRQ6}$	4 to 6	T	kept	T	[DRAME = 0] kept [DRAME = 1, OPE = 1] $\overline{CAS}$ [DRAME = 1, OPE = 1] T	T	[DRAME = 0] I/O port [DRAME = 1] $\overline{CAS}$
	7	T	kept	T	kept	kept	I/O port

Legend:

H: High level
L: Low level
T: High impedance
kept: Input port becomes high-impedance, output port retains state
DDR: Data direction register
OPE: Output port enable
WAITE: Wait input enable
BRLE: Bus release enable
BREQOE: BREQO pin enable
DRAME: DRAM space setting
LCASE: DRAM space setting, CW2 = LCASS = 0

Note: * Indicates the state after completion of the executing bus cycle.