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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8S/2600 |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, SCI, SmartCard |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 73 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 16x10b; D/A 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-TQFP |
| Supplier Device Package | 120-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2633te16v |

| | H8S/2633 Group | | | | H8S/2633R Group | |
|---|---|---|---|---|---|---|
| | **H8S/2633F-ZTAT** | **H8S/2633** | **H8S/2632** | **H8S/2631** | **H8S/2633RF-ZTAT** | **H8S/2695** |
| 32 kHz oscillator | See section 23A, Clock Pulse Generator (H8S/2633, H8S/2632, H8S/2631, H8S/2633F) | | | | See section 23B, Clock Pulse Generator (H8S/2633R, H8S/2695) | — |
| Clock Pulse Generator | See section 23A, Clock Pulse Generator (H8S/2633, H8S/2632, H8S/2631, H8S/2633F) | | | | See section 23B, Clock Pulse Generator (H8S/2633R, H8S/2695) | |
| EXTAL input level | See section 25, Electrical Characteristics (H8S/2633, H8S/2632, H8S/2631, H8S/2633F) | | | | See section 26, Electrical Characteristics (H8S/2633R) | See section 27, Electrical Characteristics (H8S/2695) |
| Recommended external PLL circuit | See section 23A, Clock Pulse Generator (H8S/2633, H8S/2632, H8S/2631, H8S/2633F) | | | | See section 23B, Clock Pulse Generator (H8S/2633R, H8S/2695) | |
| Interrupt processing vector table | See section 5, Interrupt Controller<br>See table 5.4 (a) | | | | | See section 5, Interrupt Controller<br>See table 5.4 (b) |

| Name | Symbol | I/O | Function |
|---|---|---|---|
| Lower column strobe* | $\overline{\text{LCAS}}$* | Output | DRAM lower column address strobe signal* |
| Wait | $\overline{\text{WAIT}}$ | Input | Wait request signal when accessing external 3-state access space. |
| Bus request | $\overline{\text{BREQ}}$ | Input | Request signal that releases bus to external device. |
| Bus request acknowledge | $\overline{\text{BACK}}$ | Output | Acknowledge signal indicating that bus has been released. |
| Bus request output | $\overline{\text{BREQO}}$ | Output | External bus request signal used when internal bus master accesses external space when external bus is released. |

Note: * This function is not available in the H8S/2695.

### 7.1.4 Register Configuration

Table 7.2 summarizes the registers of the bus controller.

**Table 7.2 Bus Controller Registers**

| | | | Initial Value | | |
|---|---|---|---|---|---|
| Name | Abbreviation | R/W | Power-On Reset | Manual Reset | Address*1 |
| Bus width control register | ABWCR | R/W | H'FF/H'00*2 | Retained | H'FED0 |
| Access state control register | ASTCR | R/W | H'FF | Retained | H'FED1 |
| Wait control register H | WCRH | R/W | H'FF | Retained | H'FED2 |
| Wait control register L | WCRL | R/W | H'FF | Retained | H'FED3 |
| Bus control register H | BCRH | R/W | H'D0 | Retained | H'FED4 |
| Bus control register L | BCRL | R/W | H'08 | Retained | H'FED5 |
| Pin function control register | PFCR | R/W | H'0D/H'00 | Retained | H'FDEB |
| Memory control register | MCR*3 | R/W | H'00 | Retained | H'FED6 |
| DRAM control register | DRAMCR*3 | R/W | H'00 | Retained | H'FED7 |
| Refresh timer counter | RTCNT*3 | R/W | H'00 | Retained | H'FED8 |
| Refresh time constant register | RTCOR*3 | R/W | H'FF | Retained | H'FED9 |

Notes: 1. Lower 16 bits of the address.
2. Determined by the MCU operating mode.
3. This function is not available in the H8S/2695.

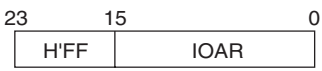
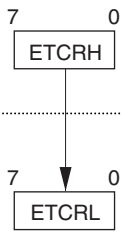
### 8.5.4 Repeat Mode

Repeat mode can be specified by setting the RPE bit in DMACR to 1, and clearing the DTIE bit to 0. In repeat mode, MAR is updated after each byte or word transfer in response to a single transfer request, and this is executed the number of times specified in ETCR. On completion of the specified number of transfers, MAR and ETCRL are automatically restored to their original settings and operation continues.

One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR.

Table 8.8 summarizes register functions in repeat mode.

**Table 8.8 Register Functions in Repeat Mode**

| | Function | | | |
|---|---|---|---|---|
| **Register** | **DTDIR = 0** | **DTDIR = 1** | **Initial Setting** | **Operation** |
|  | Source address register | Destination address register | Start address of transfer destination or transfer source | Incremented/ decremented every transfer. Initial setting is restored when value reaches H'0000 |
|  | Destination address register | Source address register | Start address of transfer source or transfer destination | Fixed |
|  | Holds number of transfers<br>Transfer counter | | Number of transfers<br>Number of transfers | Fixed<br>Decremented every transfer. Loaded with ETCRH value when count reaches H'00 |

Legend:
MAR: Memory address register
IOAR: I/O address register
ETCR: Transfer count register
DTDIR: Data transfer direction bit

### 9.3.4 Location of Register Information in Address Space

Figure 9.5 shows how the register information should be located in the address space.

Locate the MRA, SAR, MRB, DAR, CRA, and CRB registers, in that order, from the start address of the register information (contents of the vector address). In the case of chain transfer, register information should be located in consecutive areas.

Locate the register information in the on-chip RAM (addresses: H'FFEBC0 to H'FFEFBF).

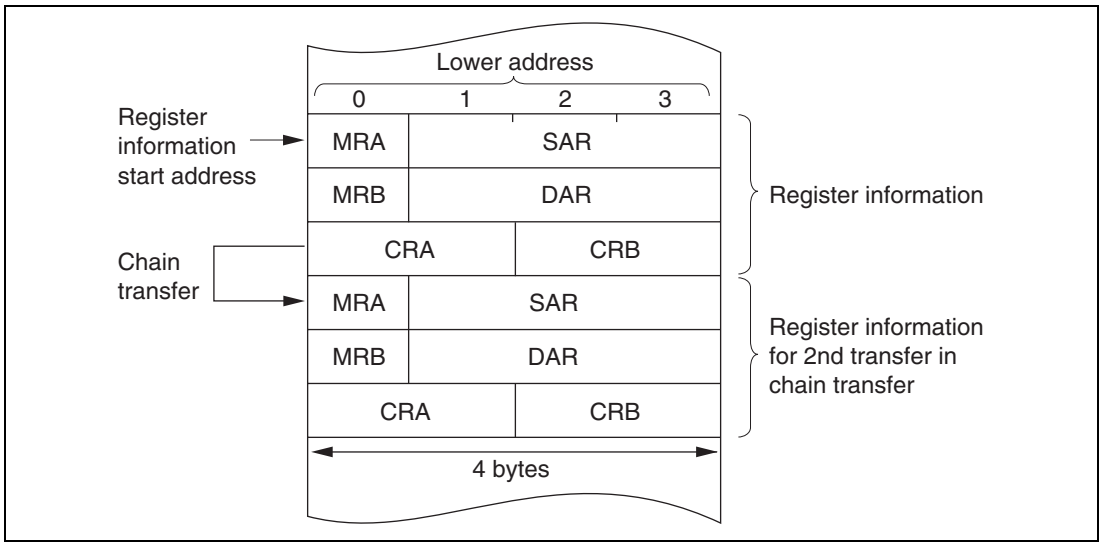



**Figure 9.5 Location of Register Information in Address Space**

| Pin | Selection Method and Pin Functions |
|---|---|
| P16/PO14/ TIOCA2/PWM2/ $\overline{\text{IRQ1}}$ | The pin function is switched as shown below according to the combination of the TPU channel 2 setting (by bits MD3 to MD0 in TMDR2, bits IOA3 to IOA0 in TIOR2, and bits CCLR1 and CCLR0 in TCR2), OEA bit in DACR3, bit NDER14 in NDERH, and bit P16DDR. |

| TPU Channel 2 Setting | Table Below (1) | Table Below (2) | | | |
|---|---|---|---|---|---|
| OEA | — | 0 | 0 | 0 | 1 |
| P16DDR | — | 0 | 1 | 1 | — |
| NDER14 | — | — | 0 | 1 | — |
| Pin function | TIOCA2 output | P16 input | P16 output | PO14 output | PWM2 output |
| | | TIOCA2 input*1 | | | |
| | $\overline{\text{IRQ1}}$ input | | | | |

| TPU Channel 2 Setting | (2) | (1) | (2) | (1) | (1) | (2) |
|---|---|---|---|---|---|---|
| MD3 to MD0 | B'0000, B'01xx | | B'001x | B'0010 | B'0011 | |
| IOA3 to IOA0 | B'0000<br>B'0100<br>B'1xxx | B'0001 to B'0011<br>B'0101 to B'0111 | B'xx00 | Other than B'xx00 | | |
| CCLR1, CCLR0 | — | — | — | — | Other than B'01 | B'01 |
| Output function | — | Output compare output | — | PWM mode 1 output*2 | PWM mode 2 output | — |

x: Don't care

Notes: 1. TIOCA2 input when MD3 to MD0 = B'0000 or B'01xx, and IOA3 = 1.
2. TIOCB2 output is disabled.

### Port B Data Register (PBDR)

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | PB7DR | PB6DR | PB5DR | PB4DR | PB3DR | PB2DR | PB1DR | PB0DR |
| Initial value | : | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | : | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

PBDR is an 8-bit readable/writable register that stores output data for the port B pins (PB7 to PB0). PBDR is initialized to H'00 by a power-on reset, and in hardware standby mode. It retains its prior state by a manual reset or in software standby mode.

### Port B Register (PORTB)

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Initial value | : | —* | —* | —* | —* | —* | —* | —* | —* |
| R/W | : | R | R | R | R | R | R | R | R |

Note: * Determined by state of pins PB7 to PB0.

PORTB is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port B pins (PB7 to PB0) must always be performed on PBDR.

If a PORTB read is performed while PBDDR bits are set to 1, the PBDR values are read. If a PORTB read is performed while PBDDR bits are cleared to 0, the pin states are read.

After a power-on reset and in hardware standby mode, PORTB contents are determined by the pin states, as PBDDR and PBDR are initialized. PORTB retains its prior state in software standby mode.

| Port | Description | Pins | Mode 4 | Mode 5 | Mode 6 | Mode 7 |
|---|---|---|---|---|---|---|
| Port 7 | 8-bit I/O port | P77/TxD3<br>P76/RxD3<br>P75/SCK3<br>P74/$\overline{\text{MRES}}$<br>P73/$\overline{\text{CS7}}$<br>P72/$\overline{\text{CS6}}$<br>P71/$\overline{\text{CS5}}$<br>P70/$\overline{\text{CS4}}$ | 8-bit I/O port also functioning as bus control output pins ($\overline{\text{CS4}}$ to $\overline{\text{CS7}}$), SCI I/O pins (SCK3, RxD3, TxD3), and the manual reset input pin ($\overline{\text{MRES}}$) | | | 8-bit I/O port also functioning as SCI I/O pins (SCK3, RxD3, TxD3) and the manual reset input pin ($\overline{\text{MRES}}$) |
| Port 9 | • 8-bit input port | P97/AN15<br>P96/AN14<br>P95/AN13<br>P94/AN12<br>P93/AN11<br>P92/AN10<br>P91/AN9<br>P90/AN8 | 8-bit input port also functioning as A/D converter analog inputs (AN15 to AN8) | | | |
| Port A | • 4-bit I/O port<br>• Built-in MOS input pull-up<br>• Open-drain output capability | PA3/A19/SCK2<br>PA2/A18/RxD2<br>PA1/A17/TxD2<br>PA0/A16 | 4-bit I/O port also functioning as SCI (channel 2) I/O pins (TxD2, RxD2, SCK2) and address outputs (A19 to A16) | | | 4-bit I/O port also functioning as SCI (channel 2) I/O pins (TxD2, RxD2, SCK2) |
| Port B | 8-bit I/O port<br>Built-in MOS input pull-up<br>Open-drain output capability | PB7/A15/TIOCB5<br>PB6/A14/TIOCA5<br>PB5/A13/TIOCB4<br>PB4/A12/TIOCA4<br>PB3/A11/TIOCD3<br>PB2/A10/TIOCC3<br>PB1/A9/TIOCB3<br>PB0/A8/TIOCA3 | 8-bit I/O port also functioning as TPU I/O pins (TIOCB5, TIOCA5, TIOCB4, TIOCA4, TIOCD3, TIOCC3, TIOCB3, TIIOCA3) and address outputs (A15 to A8) | | | 8-bit I/O port also functioning as TPU I/O pins (TIOCB5, TIOCA5, TIOCB4, TIOCA4, TIOCD3, TIOCC3, TIOCB3, TIIOCA3) |

P1DR is initialized to H'00 by a power-on reset, and in hardware standby mode. It retains its prior state by a manual reset or in software standby mode.

**Port 1 Register (PORT1)**

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |
| Initial value | : | —* | —* | —* | —* | —* | —* | —* | —* |
| R/W | : | R | R | R | R | R | R | R | R |

Note: * Determined by state of pins P17 to P10.

PORT1 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 1 pins (P17 to P10) must always be performed on P1DR.

If a PORT1 read is performed while P1DDR bits are set to 1, the P1DR values are read. If a PORT1 read is performed while P1DDR bits are cleared to 0, the pin states are read.

After a power-on reset and in hardware standby mode, PORT1 contents are determined by the pin states, as P1DDR and P1DR are initialized. PORT1 retains its prior state by a manual reset or in software standby mode.

**Pin** **Selection Method and Pin Functions**

PF3/LWR/ADTRG/ IRQ3

The pin function is switched as shown below according to the operating mode, the bus mode, A/D converter bits TRGS1 and TRGS0, and bit PF3DDR.

| Operating mode | Modes 4 to 6 | | | Mode 7 | |
|---|---|---|---|---|---|
| Bus mode | 16-bit bus mode | 8-bit bus mode | | — | |
| PF3DDR | — | 0 | 1 | 0 | 1 |
| Pin function | LWR output pin | PF3 input pin | PF3 output pin | PF3 input pin | PF3 output pin |
| | | ADTRG input pin*1 | | | |
| | | IRQ3 input pin*2 | | | |

Notes: 1. ADTRG input when TRGS0 = TRGS1 = 1.
2. When used as an external interrupt input pin, do not use as an I/O pin for another function.

PF2/ WAIT/ BREQO

The pin function is switched as shown below according to the combination of the operating mode and bits BREQOE, WAITE, ABW5 to ABW2, and PF2DDR.

| Operating Mode | Modes 4 to 6 | | | | Mode 7 | |
|---|---|---|---|---|---|---|
| BREQOE | 0 | | | 1 | — | |
| WAITE | 0 | | 1 | — | — | |
| PF2DDR | 0 | 1 | — | — | 0 | 1 |
| Pin function | PF2 input pin | PF2 output pin | WAIT input pin | BREQO output pin | PF2 input pin | PF2 output pin |

PF1/BACK

The pin function is switched as shown below according to the combination of the operating mode and bits BRLE and PF1DDR.

| Operating Mode | Modes 4 to 6 | | | Mode 7 | |
|---|---|---|---|---|---|
| BRLE | 0 | | 1 | — | |
| PF1DDR | 0 | 1 | — | 0 | 1 |
| Pin function | PF1 input pin | PF1 output pin | BACK output pin | PF1 input pin | PF1 output pin |

### Waveform Output by Compare Match

The TPU can perform 0, 1, or toggle output from the corresponding output pin using compare match.

**Example of setting procedure for waveform output by compare match:** Figure 11.9 shows an example of the setting procedure for waveform output by compare match

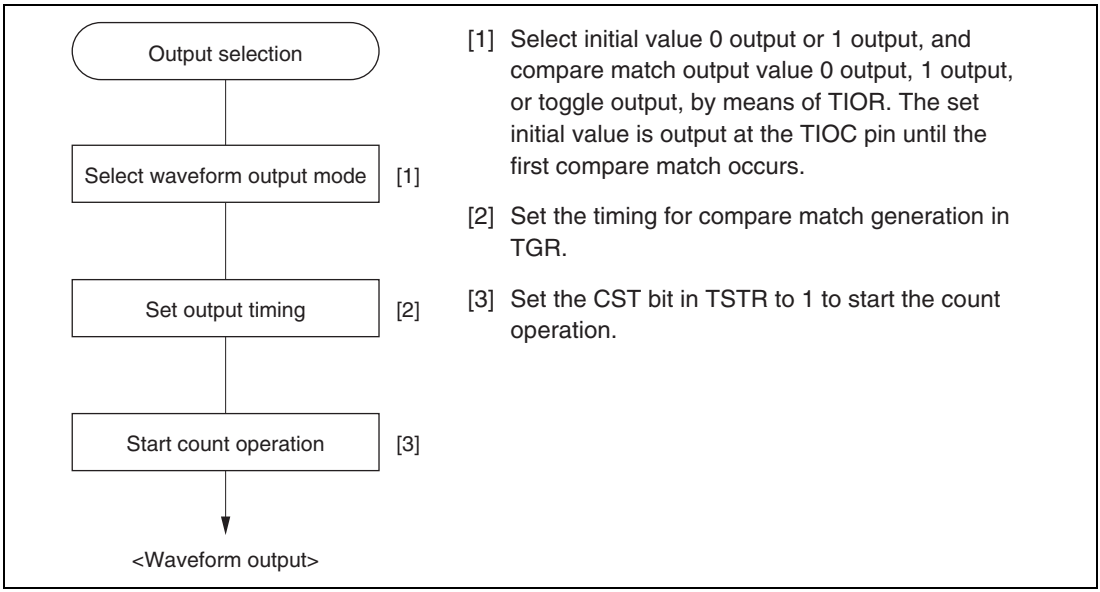



**Figure 11.9 Example of Setting Procedure for Waveform Output by Compare Match**

Figure 16.17 shows an example of SCI operation in transmission.

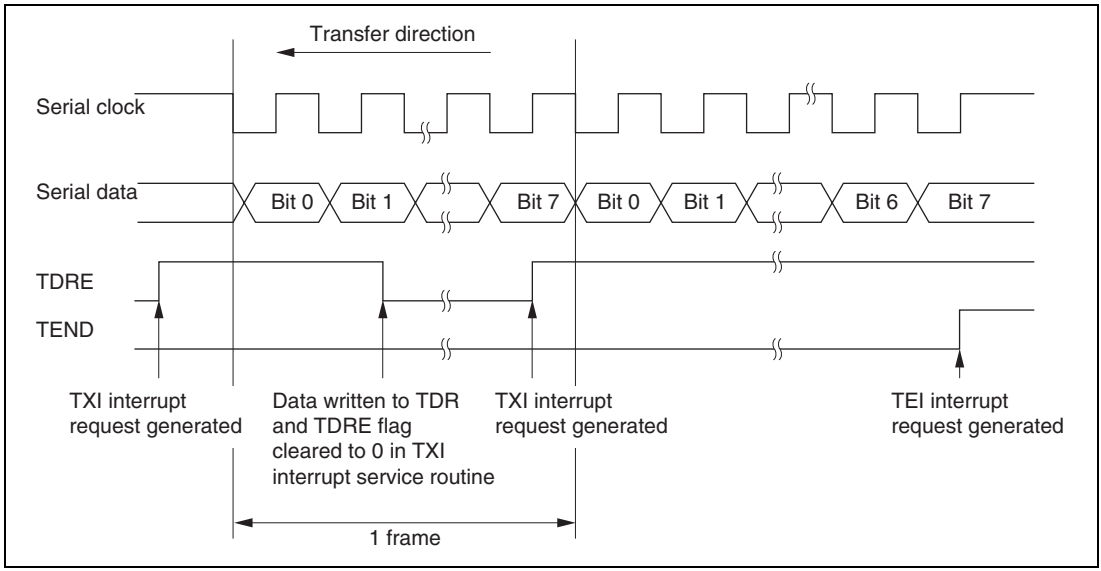



**Figure 16.17 Example of SCI Operation in Transmission**

**Serial data reception (clocked synchronous mode):** Figure 16.18 shows a sample flowchart for serial reception.

The following procedure should be used for serial data reception.

When changing the operating mode from asynchronous to clocked synchronous, be sure to check that the ORER, PER, and FER flags are all cleared to 0.

The RDRF flag will not be set if the FER or PER flag is set to 1, and neither transmit nor receive operations will be possible.

## 16.4 SCI Interrupts

The SCI has four interrupt sources: the transmit-end interrupt (TEI) request, receive-error interrupt (ERI) request, receive-data-full interrupt (RXI) request, and transmit-data-empty interrupt (TXI) request. Table 16.13 shows the interrupt sources and their relative priorities. Individual interrupt sources can be enabled or disabled with the TIE, RIE, and TEIE bits in the SCR. Each kind of interrupt request is sent to the interrupt controller independently.

When the TDRE flag in SSR is set to 1, a TXI interrupt request is generated. When the TEND flag in SSR is set to 1, a TEI interrupt request is generated. A TXI interrupt can activate the DMAC* or DTC* to perform data transfer. The TDRE flag is cleared to 0 automatically when data transfer is performed by the DMAC* or DTC*. The DMAC* or DTC* cannot be activated by a TEI interrupt request.

When the RDRF flag in SSR is set to 1, an RXI interrupt request is generated. When the ORER, PER, or FER flag in SSR is set to 1, an ERI interrupt request is generated. An RXI interrupt can activate the DMAC* or DTC* to perform data transfer. The RDRF flag is cleared to 0 automatically when data transfer is performed by the DMAC* or DTC*. The DMAC* or DTC* cannot be activated by an ERI interrupt request.

Note that the DMAC* cannot be activated by interrupts of SCI channels 2 to 4.

Note: * DMAC and DTC functions are not available in the H8S/2695.

**Bit 4**

| TRS | Description |
|---|---|
| 0 | Receive mode (Initial value)<br>[Clearing conditions]<br>1. When 0 is written by software (in cases other than setting condition 3)<br>2. When 0 is written in TRS after reading TRS = 1 (in case of clearing condition 3)<br>3. When bus arbitration is lost after transmission is started in I²C bus format master mode |
| 1 | Transmit mode<br>[Setting conditions]<br>1. When 1 is written by software (in cases other than clearing conditions 3 and 4)<br>2. When 1 is written in TRS after reading TRS = 0 (in case of clearing conditions 3 and 4)<br>3. When 1 is received as the R/W bit of the first frame in I²C bus format slave mode |

**Bit 3—Acknowledge Bit Judgement Selection (ACKE):** Specifies whether the value of the acknowledge bit returned from the receiving device when using the I²C bus format is to be ignored and continuous transfer is performed, or transfer is to be aborted and error handling, etc., performed if the acknowledge bit is 1. When the ACKE bit is 0, the value of the received acknowledge bit is not indicated by the ACKB bit, which is always 0.

In the H8S/2633 Group, the DTC* can be used to perform continuous transfer. The DTC* is activated when the IRTR interrupt flag is set to 1 (IRTR is one of two interrupt flags, the other being IRIC). When the ACKE bit is 0, the TDRE, IRIC, and IRTR flags are set on completion of data transmission, regardless of the value of the acknowledge bit. When the ACKE bit is 1, the TDRE, IRIC, and IRTR flags are set on completion of data transmission when the acknowledge bit is 0, and the IRIC flag alone is set on completion of data transmission when the acknowledge bit is 1.

When the DTC* is activated, the TDRE, IRIC, and IRTR flags are cleared to 0 after the specified number of data transfers have been executed. Consequently, interrupts are not generated during continuous data transfer, but if data transmission is completed with a 1 acknowledge bit when the ACKE bit is set to 1, the DTC* is not activated and an interrupt is generated, if enabled.

Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.

Note: * The DTC function is not available in the H8S/2695.

## 22.5 Register Descriptions

### 22.5.1 Flash Memory Control Register 1 (FLMCR1)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | FWE | SWE1 | ESU1 | PSU1 | EV1 | PV1 | E1 | P1 |
| Initial value: | —* | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note: * Determined by the state of the FWE pin.

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode for addresses H'00000 to H'3FFFF is entered by setting SWE1 bit to 1 when FWE = 1, then setting the PV1 or EV1 bit. Program mode for addresses H'00000 to H'3FFFF is entered by setting SWE1 bit to 1 when FWE = 1, then setting the PSU1 bit, and finally setting the P1 bit. Erase mode for addresses H'00000 to H'3FFFF is entered by setting SWE1 bit to 1 when FWE = 1, then setting the ESU1 bit, and finally setting the E1 bit. FLMCR1 is initialized by a power-on reset, and in hardware standby mode and software standby mode. Its initial value is H'80 when a high level is input to the FWE pin, and H'00 when a low level is input. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writes are enabled only in the following cases: Writes to bit SWE1 of FLMCR1 enabled when FWE = 1, to bits ESU1, PSU1, EV1, and PV1 when FWE = 1 and SWE1 = 1, to bit E1 when FWE = 1, SWE1 = 1 and ESU1 = 1, and to bit P1 when FWE = 1, SWE1 = 1, and PSU1 = 1.

**Bit 7—Flash Write Enable Bit (FWE):** Sets hardware protection against flash memory programming/erasing.

**Bit 7**

| FWE | Description |
|---|---|
| 0 | When a low level is input to the FWE pin (hardware-protected state) |
| 1 | When a high level is input to the FWE pin |

### 23A.3.2 External Clock Input

**Circuit Configuration:** An external clock signal can be input as shown in the examples in figure 23A.6. If the XTAL pin is left open, make sure that stray capacitance is no more than 10 pF.

In example (b), make sure that the external clock is held high in standby mode.

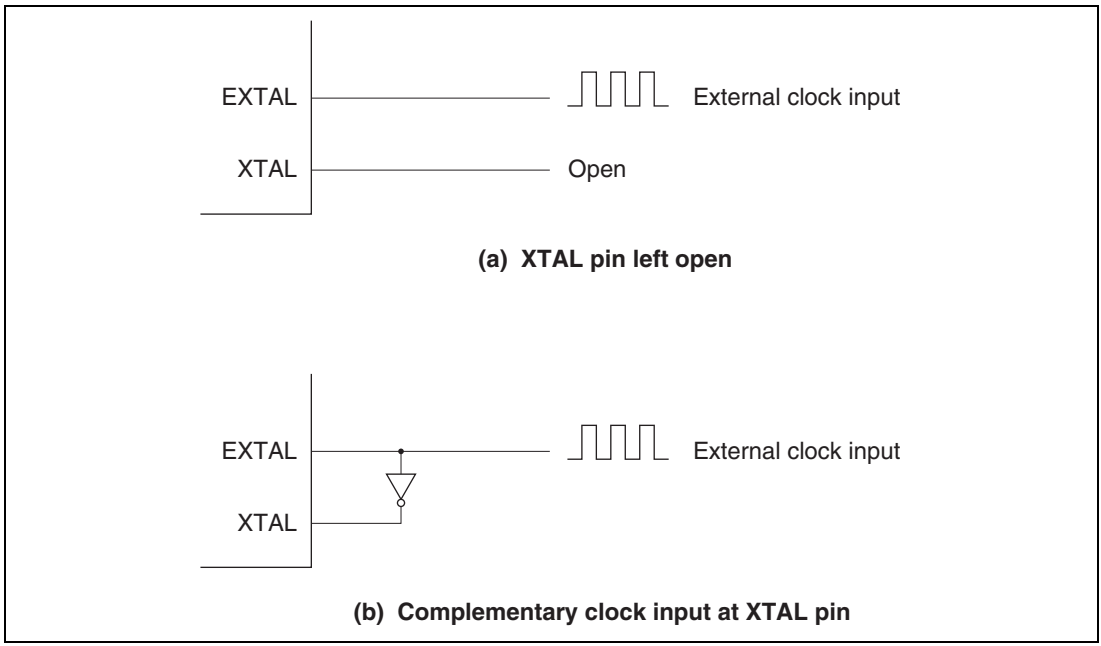



**Figure 23A.6 External Clock Input (Examples)**

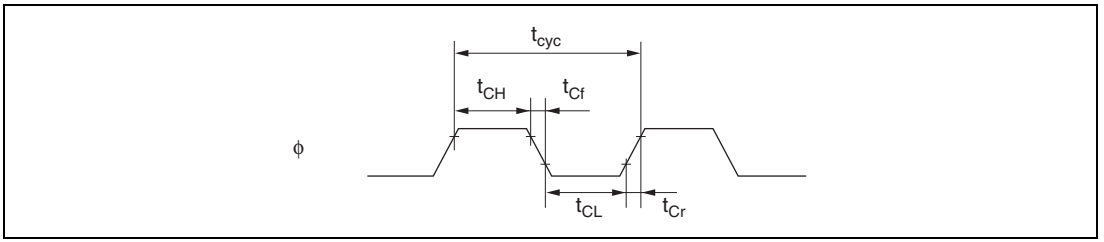



**Figure 25.2 System Clock Timing**

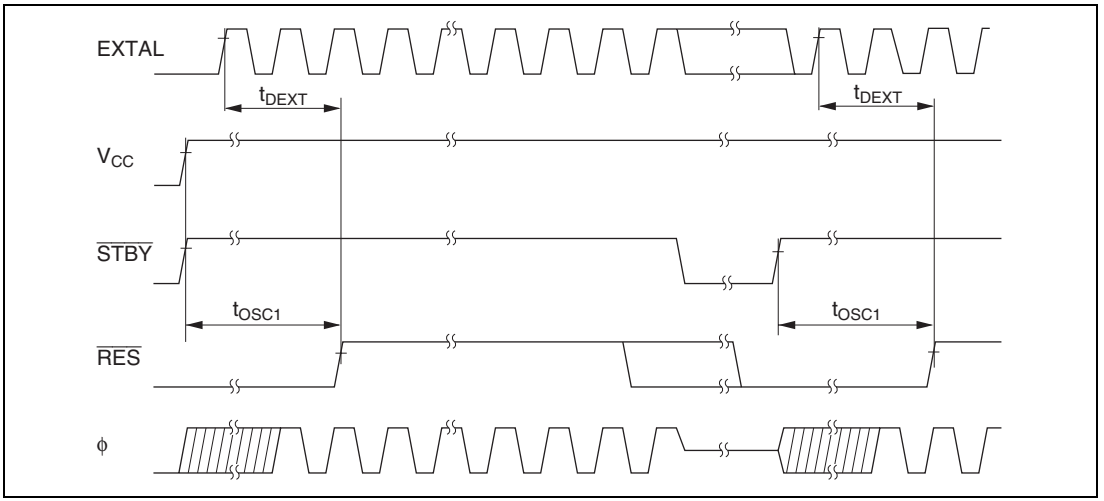



**Figure 25.3 Oscillator Settling Timing**

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| MOS input pull-up current | Ports A to E | $-I_P$ | 50 | — | 300 | µA | $V_{in}$ = 0 V |
| Input capacitance | $\overline{RES}$ | $C_{in}$ | — | — | 30 | pF | $V_{in}$ = 0 V |
| | NMI | | — | — | 30 | pF | f = 1 MHz |
| | All input pins except $\overline{RES}$ and NMI | | — | — | 15 | pF | $T_a$ = 25°C |
| Current dissipation*2 | Normal operation | $I_{CC}$*4 | — | 70 | 84 | mA | f = 28 MHz |
| | Sleep mode | | — | 55 | 77 | mA | f = 28 MHz |
| | All modules stopped | | — | 40 | — | mA | f = 28 MHz (reference values) |
| | Medium-speed mode (φ/32) | | — | 54 | — | mA | f = 28 MHz (reference values) |
| | Standby mode | | — | 0.1 | 5.0 | µA | $T_a \leq$ 50°C |
| | | | — | — | 20 | | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 0.6 | 2.0 | mA | $AV_{CC}$ = 5.0 V |
| | Idle | | — | 0.1 $T_a$ = 25°C | 5.0 | µA | |
| Reference power supply current | During A/D conversion | $AI_{CC}$ | — | 4.0 | 5.0 | mA | $V_{ref}$ = 5.0 V |
| | Idle | | — | 0.1 $T_a$ = 25°C | 5.0 | µA | |
| RAM standby voltage*3 | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: 1. If the A/D converter is not used, do not leave the $AV_{CC}$, $V_{ref}$, and $AV_{SS}$ pins open. Apply a voltage between 3.3 V and 5.5 V to the $AV_{CC}$ and $V_{ref}$ pins by connecting them to $PV_{CC}$, for instance. Set $V_{ref} \leq AV_{CC}$.

2. Current dissipation values are for $V_{IH} = AV_{CC}$ (ports 4 and 9), or $PV_{CC}$ (other), and $V_{IL}$ = 0 V, with all output pins unloaded and the on-chip MOS pull-up transistors in the off state.

3. The values are for $V_{RAM} \leq PV_{CC} < 3.0$ V, $V_{IH}$ min = $PV_{CC} - 0.1$ V, and $V_{IL}$ max = 0.1 V.

4. $I_{CC}$ depends on $PV_{CC}$ and f as follows:
   $I_{CC}$ max = 15 (mA) + 0.45 (mA/(MHz × V)) × $PV_{CC}$ × f (normal operation)
   $I_{CC}$ max = 15 (mA) + 0.40 (mA/(MHz × V)) × $PV_{CC}$ × f (sleep mode)

## Table A.3 Operation Code Map (4)

| Instruction code | 1st byte | | 2nd byte | | 3rd byte | | 4th byte | | 5th byte | | 6th byte | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AH | AL | BH | BL | CH | CL | DH | DL | EH | EL | FH | FL |

Instruction when most significant bit of FH is 0.
Instruction when most significant bit of FH is 1.

| EL / AHALBHBLCHCLDHDLEH | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6A10aaaa6* | | | | BTST | | | | | | | | | | | | |
| 6A10aaaa7* | | | | | BOR / BIOR | BXOR / BIXOR | BAND / BIAND | BLD / BILD | | | | | | | | |
| 6A18aaaa6* | BSET | BNOT | BCLR | | | | | BST / BIST | | | | | | | | |
| 6A18aaaa7* | | | | | | | | | | | | | | | | |

| Instruction code | 1st byte | | 2nd byte | | 3rd byte | | 4th byte | | 5th byte | | 6th byte | | 7th byte | | 8th byte | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AH | AL | BH | BL | CH | CL | DH | DL | EH | EL | FH | FL | GH | GL | HH | HL |

Instruction when most significant bit of HH is 0.
Instruction when most significant bit of HH is 1.

| GL / AHALBHBL ... FHFLGH | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6A30aaaaaaaa6* | | | | BTST | | | | | | | | | | | | |
| 6A30aaaaaaaa7* | | | | | BOR / BIOR | BXOR / BIXOR | BAND / BIAND | BLD / BILD | | | | | | | | |
| 6A38aaaaaaaa6* | BSET | BNOT | BCLR | | | | | BST / BIST | | | | | | | | |
| 6A38aaaaaaaa7* | | | | | | | | | | | | | | | | |

Note: * aa is the absolute address specification.

## NDRH—Next Data Register H H'FE2C, H'FE2E PPG

Same trigger for pulse output groups.

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | NDR15 | NDR14 | NDR13 | NDR12 | NDR11 | NDR10 | NDR9 | NDR8 |
| Initial value | : | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | : | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | — | — | — | — | — | — | — | — |
| Initial value | : | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | : | — | — | — | — | — | — | — | — |

Different triggers for pulse output groups.

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | NDR15 | NDR14 | NDR13 | NDR12 | — | — | — | — |
| Initial value | : | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| R/W | : | R/W | R/W | R/W | R/W | — | — | — | — |

| Bit | : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | | — | — | — | — | NDR11 | NDR10 | NDR9 | NDR8 |
| Initial value | : | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| R/W | : | — | — | — | — | R/W | R/W | R/W | R/W |

Note: For details see section 12.2.4, Notes on NDR Access.

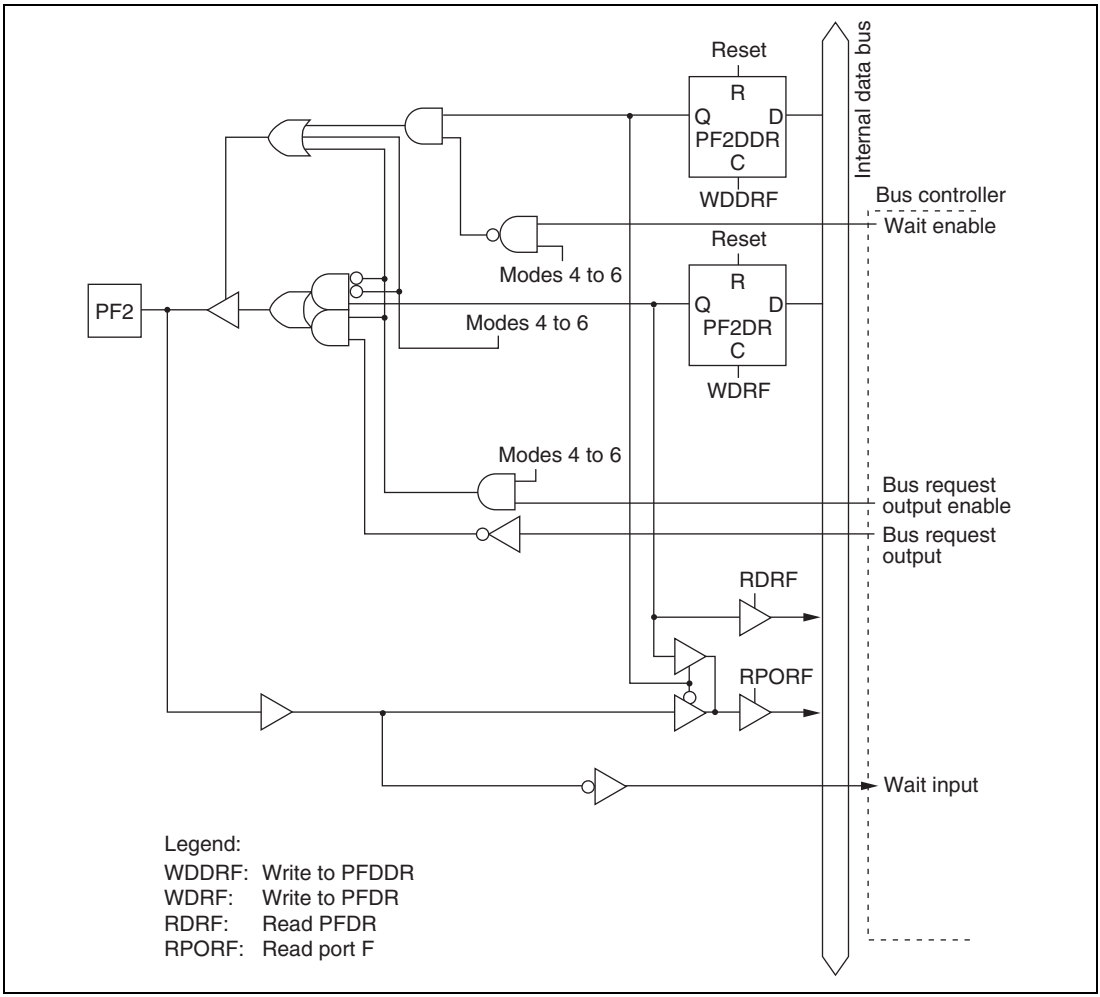



**Figure C.23 (c) Port F Block Diagram (Pin PF2)**