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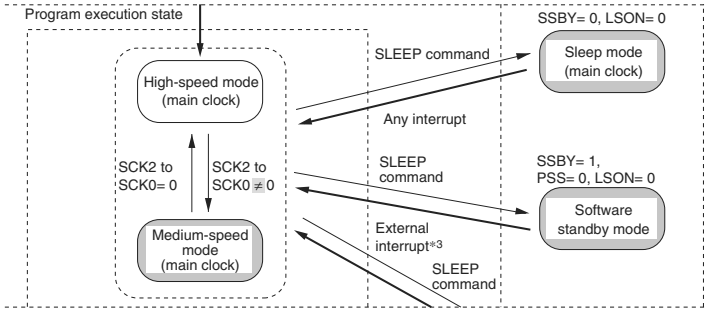
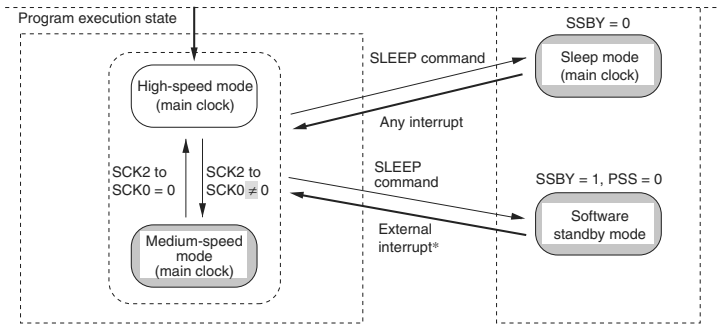
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	25MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	73
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2633te25v

Item	Page	Revision (See Manual for Details)
24.1 Overview Figure 24.1 (a) Mode Transition Diagram (H8S/2633 Group, H8S/2633R)	1019	Figure amended 
Figure 24.1 (b) Mode Transition Diagram (H8S/2695)	1020	Figure amended 
24.8.3 Notes	1041	Description amended (2) Current Consumption when Waiting for Oscillation Stabilization The current consumption increases during stabilization of oscillation.
24.10.3 Usage Notes	—	Description deleted
24.13 Usage Notes	1046	Newly added

Pin No.		Pin Name			
TFP-120	**FP-128B**	**Mode 4**	**Mode 5**	**Mode 6**	**Mode 7**
24	28	PA3/A19/SCK2	PA3/A19/SCK2	PA3/A19/SCK2	PA3/SCK2
25	29	VSS	VSS	VSS	VSS
26	30	P10/PO8/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/PO8/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/PO8/TIOCA0/ $\overline{\text{DACK0}}$/A20	P10/PO8/TIOCA0/ $\overline{\text{DACK0}}$
27	31	P11/PO9/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/PO9/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/PO9/TIOCB0/ $\overline{\text{DACK1}}$/A21	P11/PO9/TIOCB0/ $\overline{\text{DACK1}}$
28	32	P12/PO10/TIOCC0/ TCLKA/A22	P12/PO10/TIOCC0/ TCLKA/A22	P12/PO10/TIOCC0/ TCLKA/A22	P12/PO10/TIOCC0/ TCLKA
29	33	P13/PO11/TIOCD0/ TCLKB/A23	P13/PO11/TIOCD0/ TCLKB/A23	P13/PO11/TIOCD0/ TCLKB/A23	P13/PO11/TIOCD0/ TCLKB
30	34	P14/PO12/TIOCA1/ $\overline{\text{IRQ0}}$	P14/PO12/TIOCA1/ $\overline{\text{IRQ0}}$	P14/PO12/TIOCA1/ $\overline{\text{IRQ0}}$	P14/PO12/TIOCA1/ $\overline{\text{IRQ0}}$
—	35	NC*1	NC*1	NC*1	NC*1
—	36	NC*1	NC*1	NC*1	NC*1
31	37	P15/PO13/TIOCB1/ TCLKC	P15/PO13/TIOCB1/ TCLKC	P15/PO13/TIOCB1/ TCLKC	P15/PO13/TIOCB1/ TCLKC
32	38	P16/PO14/TIOCA2/ PWM2/$\overline{\text{IRQ1}}$	P16/PO14/TIOCA2/ PWM2/$\overline{\text{IRQ1}}$	P16/PO14/TIOCA2/ PWM2/$\overline{\text{IRQ1}}$	P16/PO14/TIOCA2/ PWM2/$\overline{\text{IRQ1}}$
33	39	P17/PO15/TIOCB2/ PWM3/TCLKD	P17/PO15/TIOCB2/ PWM3/TCLKD	P17/PO15/TIOCB2/ PWM3/TCLKD	P17/PO15/TIOCB2/ PWM3/TCLKD
34	40	PE0/D0	PE0/D0	PE0/D0	PE0
35	41	PE1/D1	PE1/D1	PE1/D1	PE1
36	42	PE2/D2	PE2/D2	PE2/D2	PE2
37	43	PE3/D3	PE3/D3	PE3/D3	PE3
38	44	PE4/D4	PE4/D4	PE4/D4	PE4
39	45	PE5/D5	PE5/D5	PE5/D5	PE5
40	46	PE6/D6	PE6/D6	PE6/D6	PE6
41	47	PE7/D7	PE7/D7	PE7/D7	PE7
42	48	VSS	VSS	VSS	VSS
43	49	D8	D8	D8	PD0
44	50	PVCC1	PVCC1	PVCC1	PVCC1
45	51	D9	D9	D9	PD1
46	52	D10	D10	D10	PD2
47	53	D11	D11	D11	PD3

Channel	Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	Description		
1	0	0	0	0	TGR1B is output compare register	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR1B is input capture register	Capture input source is TIOCB1 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges
		1	*	*		Capture input source is TGR0C compare match/ input capture	Input capture at generation of TGR0C compare match/input capture

*: Don't care

Channel	Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	Description		
2	0	0	0	0	TGR2B is output compare register	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	*	0	0	TGR2B is input capture register	Capture input source is TIOCB2 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	*			Input capture at both edges

*: Don't care

Contention between TGR Write and Input Capture: If the input capture signal is generated in the T2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 11.54 shows the timing in this case.

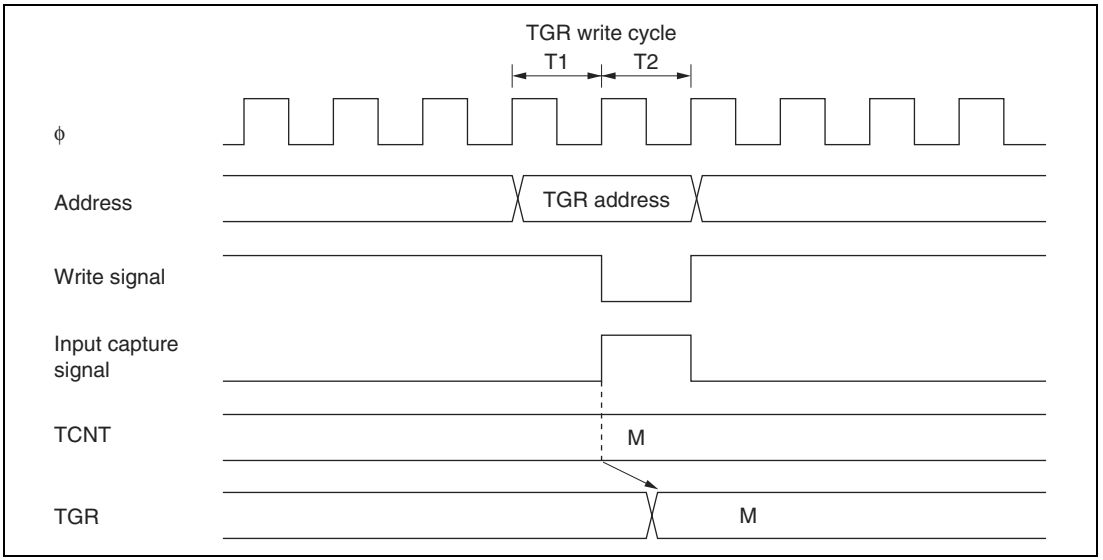


Figure 11.54 Contention between TGR Write and Input Capture

NDERL Bits 7 to 0—Next Data Enable 7 to 0 (NDER7 to NDER0): These bits enable or disable pulse output on a bit-by-bit basis. However, the H8S/2633 Group has no output pins corresponding to NDRL.

Bits 7 to 0

NDER7 to NDER0	Description
0	Pulse outputs PO7 to PO0 are disabled (NDR7 to NDR0 are not transferred to POD7 to POD0) (Initial value)
1	Pulse outputs PO7 to PO0 are enabled (NDR7 to NDR0 are transferred to POD7 to POD0)

12.2.2 Output Data Registers H and L (PODRH, PODRL)

PODRH

Bit	:	7	6	5	4	3	2	1	0
		POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

PODRL

Bit	:	7	6	5	4	3	2	1	0
		POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * A bit that has been set for pulse output by NDER is read-only.

PODRH and PODRL are 8-bit readable/writable registers that store output data for use in pulse output. However, the H8S/2633 Group has no pins corresponding to PODRL.

Table 16.5 shows the maximum bit rate for each frequency in asynchronous mode. Tables 16.6 and 16.7 show the maximum bit rates with external clock input.

Table 16.5 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
2	62500	0	0
2.097152	65536	0	0
2.4576	76800	0	0
3	93750	0	0
3.6864	115200	0	0
4	125000	0	0
4.9152	153600	0	0
5	156250	0	0
6	187500	0	0
6.144	192000	0	0
7.3728	230400	0	0
8	250000	0	0
9.8304	307200	0	0
10	312500	0	0
12	375000	0	0
12.288	384000	0	0
14	437500	0	0
14.7456	460800	0	0
16	500000	0	0
17.2032	537600	0	0
18	562500	0	0
19.6608	614400	0	0
20	625000	0	0
25	781250	0	0
28	875000	0	0

In serial reception, the SCI operates as described below.

[1] The SCI monitors the transmission line, and if a 0 stop bit is detected, performs internal synchronization and starts reception.

[2] The received data is stored in RSR in LSB-to-MSB order.

[3] The parity bit and stop bit are received.

After receiving these bits, the SCI carries out the following checks.

[a] Parity check:

The SCI checks whether the number of 1 bits in the receive data agrees with the parity (even or odd) set in the O/$\overline{E}$ bit in SMR.

[b] Stop bit check:

The SCI checks whether the stop bit is 1.

If there are two stop bits, only the first is checked.

[c] Status check:

The SCI checks whether the RDRF flag is 0, indicating that the receive data can be transferred from RSR to RDR.

If all the above checks are passed, the RDRF flag is set to 1, and the receive data is stored in RDR.

If a receive error* is detected in the error check, the operation is as shown in table 16.11.

Note: * Subsequent receive operations cannot be performed when a receive error has occurred. Also note that the RDRF flag is not set to 1 in reception, and so the error flags must be cleared to 0.

[4] If the RIE bit in SCR is set to 1 when the RDRF flag changes to 1, a receive data full interrupt (RXI) request is generated.

Also, if the RIE bit in SCR is set to 1 when the ORER, PER, or FER flag changes to 1, a receive error interrupt (ERI) request is generated.

As per the standard, the High pulse width is a minimum of 1.41 µs, the maximum is (3/16 + 2.5%) × bit rate, or (3/16 × bit rate) + 1.08 µs. With a 20MHz system clock ϕ, the minimum High pulse width can be set to 1.6 µs, which is greater than the 1.41 µs required by the standard.

When the value of the serial data is "1", no pulse is output.

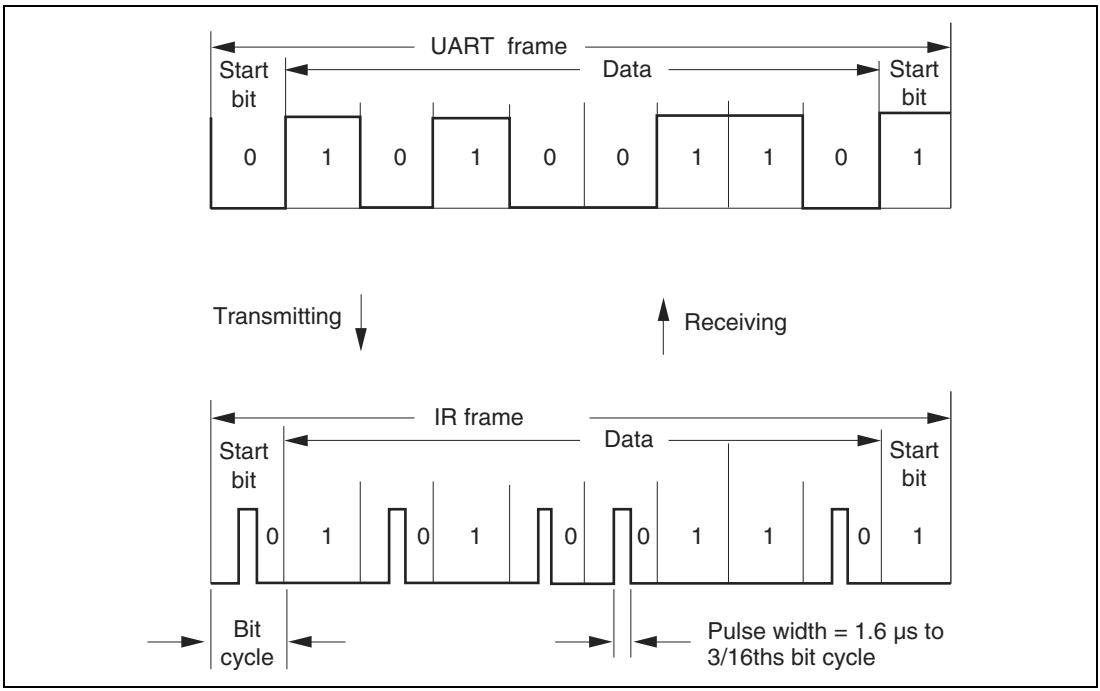


Figure 16.22 IrDA Transmit and Receive Operations

(2) Receiving

When receiving, the IR frame data is converted into UART frames by the IrDA interface and input to the SCI.

When a High pulse is detected, "0" is output. If there is no pulse for the duration of 1 bit, "1" is output. Pulses of less than the minimum pulse width of 1.41 µs are also recognized as "0" data.

(3) Selecting High Pulse Width

Table 16.12 shows the settings of IrCKS2 to IrCKS0 (for the minimum pulse width), at various LSI operating frequencies, and various bit rates to set the pulse width when transmitting with a pulse width less than 3/16ths of the bit rate.

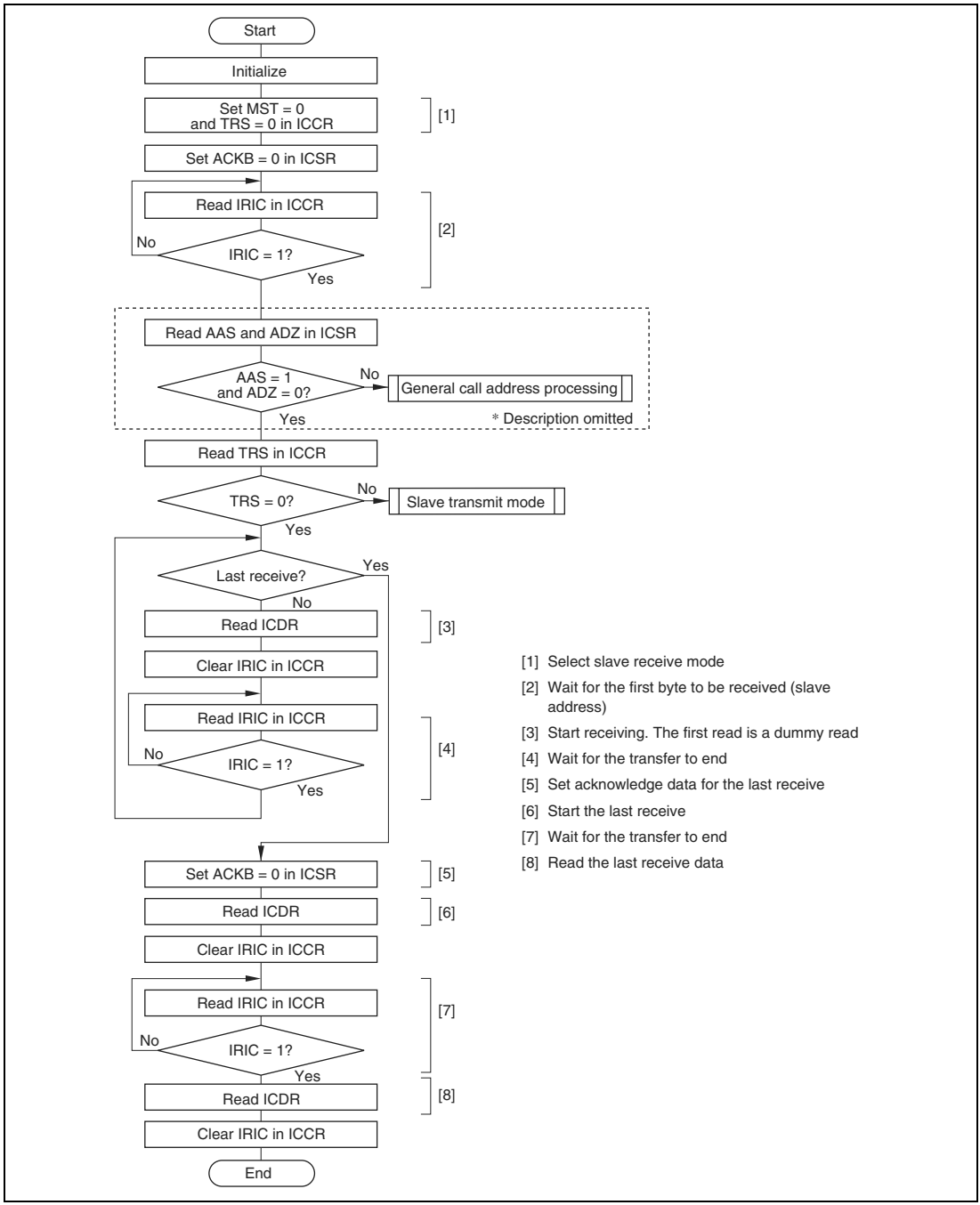


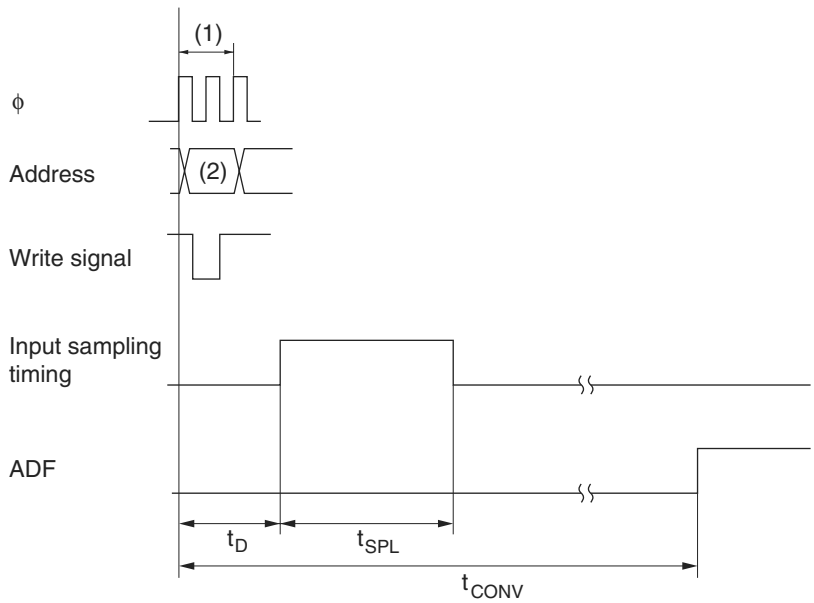
Figure 18.14 Flowchart for Slave Receive Mode (Example)

19.4.3 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit. The A/D converter samples the analog input at a time t_D after the ADST bit is set to 1, then starts conversion. Figure 19.5 shows the A/D conversion timing. Table 19.4 indicates the A/D conversion time.

As indicated in figure 19.5, the A/D conversion time includes t_D and the input sampling time. The length of t_D varies depending on the timing of the write access to ADCSR. The total conversion time therefore varies within the ranges indicated in table 19.4.

In scan mode, the values given in table 19.4 apply to the first conversion time. The values given in table 19.5 apply to the second and subsequent conversions. In both cases, set bits CKS1 and CKS0 in ADCR to give a conversion time of at least 10 µs when $AV_{CC} \geq 4.5$ V, and at least 16 µs when $AV_{CC} < 4.5$ V.



Legend:
(1): ADCSR write cycle
(2): ADCSR address
t_D: A/D conversion start delay
t_{SPL}: Input sampling time
t_{CONV}: A/D conversion time

Figure 19.5 A/D Conversion Timing

Bits 1 and 0—Frequency Multiplication Factor (STC1, STC0): The STC bits specify the frequency multiplication factor of the PLL circuit.

Bit 1	Bit 0		
STC1	**STC0**	**Description**	
0	0	×1	(Initial value)
	1	×2	
1	0	×4	
	1	Setting prohibited	

Note: A system clock frequency multiplied by the multiplication factor (STC1 and STC0) should not exceed the maximum operating frequency defined in sections 26 and 27, Electrical Characteristics.
Current consumption and noise can be reduced by using this function's PLL ×4 setting and lowering the external clock frequency.
The input clock frequency is 2 MHz to 25 MHz. With the H8S/2633R and H8S/2695 PLL must be set to use a multiplier of × 2 or × 4 when operating at frequencies of 25 MHz < ϕ ≤ 28 MHz.

23B.3 Oscillator

Clock pulses can be supplied by connecting a crystal resonator, or by input of an external clock.

23B.3.1 Connecting a Crystal Resonator

Circuit Configuration: A crystal resonator can be connected as shown in the example in figure 23B.2. Select the damping resistance R_d according to table 23B.2. An AT-cut parallel-resonance crystal should be used.

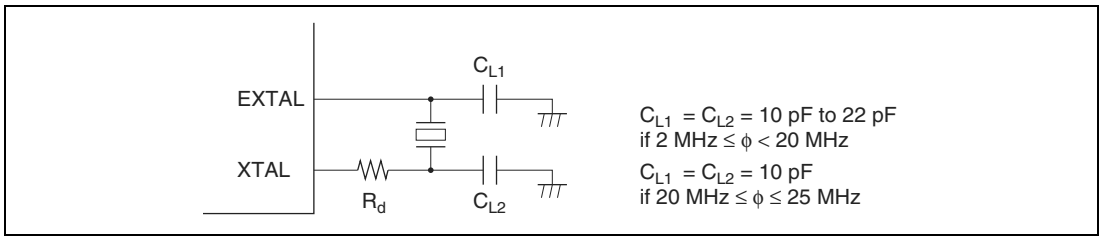


Figure 23B.2 Connection of Crystal Resonator (Example)

26.4 A/D Conversion Characteristics

Table 26.11 lists the A/D conversion characteristics.

Table 26.11 A/D Conversion Characteristics

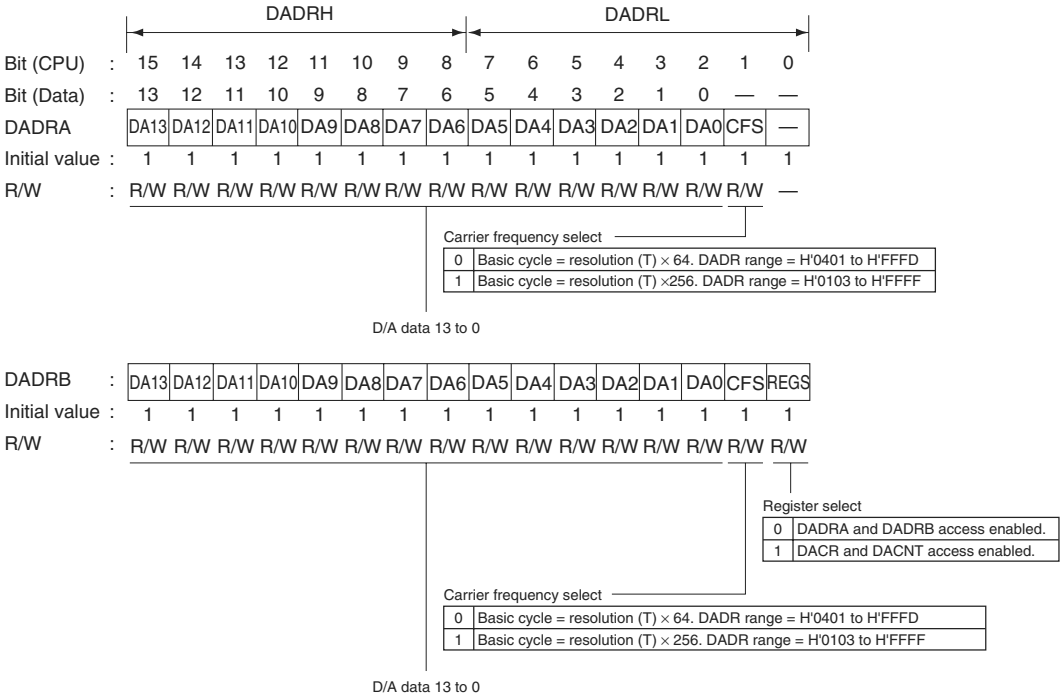
Conditions: PV_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{ref} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = $PLLV_{SS}$ = 0 V, ϕ = 2 to 28 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Min	Typ	Max	Unit
Resolution	10	10	10	bits
Conversion time	10	—	—	µs
Analog input capacitance	—	—	20	pF
Permissible signal-source impedance	—	—	5	kΩ
Nonlinearity error	—	—	±3.5	LSB
Offset error	—	—	±3.5	LSB
Full-scale error	—	—	±3.5	LSB
Quantization	—	±0.5	—	LSB
Absolute accuracy	—	—	±4.0	LSB

Instruction	Mnemonic	Size	Instruction Format									
			1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte	9th byte	10th byte
ROTR	ROTR.B Rd	B	1 3	8 rd								
	ROTR.B #2, Rd	B	1 3	C rd								
	ROTR.W Rd	W	1 3	9 rd								
	ROTR.W #2, Rd	W	1 3	D rd								
	ROTR.L ERd	L	1 3	B 0 erd								
	ROTR.L #2, ERd	L	1 3	F 0 erd								
ROTXL	ROTXL.B Rd	B	1 2	0 rd								
	ROTXL.B #2, Rd	B	1 2	4 rd								
	ROTXL.W Rd	W	1 2	1 rd								
	ROTXL.W #2, Rd	W	1 2	5 rd								
	ROTXL.L ERd	L	1 2	3 0 erd								
	ROTXL.L #2, ERd	L	1 2	7 0 erd								
ROTXR	ROTXR.B Rd	B	1 3	0 rd								
	ROTXR.B #2, Rd	B	1 3	4 rd								
	ROTXR.W Rd	W	1 3	1 rd								
	ROTXR.W #2, Rd	W	1 3	5 rd								
	ROTXR.L ERd	L	1 3	3 0 erd								
	ROTXR.L #2, ERd	L	1 3	7 0 erd								
RTE	RTE	—	5 6	7 0								
RTS	RTS	—	5 4	7 0								
SHAL	SHAL.B Rd	B	1 0	8 rd								
	SHAL.B #2, Rd	B	1 0	C rd								
	SHAL.W Rd	W	1 0	9 rd								
	SHAL.W #2, Rd	W	1 0	D rd								
	SHAL.L ERd	L	1 0	B 0 erd								
	SHAL.L #2, ERd	L	1 0	F 0 erd								

Instruction	Mnemonic	Size	Instruction Format										
			1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte	9th byte	10th byte	
SHAR	SHAR.B Rd	B	1 1	8 rd									
	SHAR.B #2, Rd	B	1 1	C rd									
	SHAR.W Rd	W	1 1	9 rd									
	SHAR.W #2, Rd	W	1 1	D rd									
	SHAR.L ERd	L	1 1	B 0 erd									
	SHAR.L #2, ERd	L	1 1	F 0 erd									
SHLL	SHLL.B Rd	B	1 0	0 rd									
	SHLL.B #2, Rd	B	1 0	4 rd									
	SHLL.W Rd	W	1 0	1 rd									
	SHLL.W #2, Rd	W	1 0	5 rd									
	SHLL.L ERd	L	1 0	3 0 erd									
	SHLL.L #2, ERd	L	1 0	7 0 erd									
SHLR	SHLR.B Rd	B	1 1	0 rd									
	SHLR.B #2, Rd	B	1 1	4 rd									
	SHLR.W Rd	W	1 1	1 rd									
	SHLR.W #2, Rd	W	1 1	5 rd									
	SHLR.L ERd	L	1 1	3 0 erd									
	SHLR.L #2, ERd	L	1 1	7 0 erd									
SLEEP	SLEEP	—	0 1	8 0									
STC	STC.B CCR,Rd	B	0 2	0 rd									
	STC.B EXR,Rd	B	0 2	1 rd									
	STC.W CCR,@ERd	W	0 1	4 0	6 9	1 erd 0							
	STC.W EXR,@ERd	W	0 1	4 1	6 9	1 erd 0							
	STC.W CCR,@(d:16,ERd)	W	0 1	4 0	6 F	1 erd 0	disp						
	STC.W EXR,@(d:16,ERd)	W	0 1	4 1	6 F	1 erd 0	disp						
	STC.W CCR,@(d:32,ERd)	W	0 1	4 0	7 8	0 erd 0	6	B A 0	disp				
	STC.W EXR,@(d:32,ERd)	W	0 1	4 1	7 8	0 erd 0	6	B A 0	disp				
	STC.W CCR,@-ERd	W	0 1	4 0	6 D	1 erd 0							
	STC.W EXR,@-ERd	W	0 1	4 1	6 D	1 erd 0							

DADRAH0—PWM (D/A) Data Register AH0	**H'FDB8**	**PWM0**
DADRAL0—PWM (D/A) Data Register AL0	**H'FDB9**	**PWM0**
DADRBH0—PWM (D/A) Data Register BH0	**H'FDBA**	**PWM0**
DADRBL0—PWM (D/A) Data Register BL0	**H'FDBB**	**PWM0**
DADRAH1—PWM (D/A) Data Register AH1	**H'FDBC**	**PWM1**
DADRAL1—PWM (D/A) Data Register AL1	**H'FDBD**	**PWM1**
DADRBH1—PWM (D/A) Data Register BH1	**H'FDBE**	**PWM1**
DADRBL1—PWM (D/A) Data Register BL1	**H'FDBF**	**PWM1**



NDERH—Next Data Enable Register H H'FE28 PPG
NDERL—Next Data Enable Register L H'FE29 PPG

NDERH

Bit	7	6	5	4	3	2	1	0
	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Next data enable 15 to 8

NDER15 to NDER8	
0	Pulse output PO15 to PO8 disabled (transfer from NDR15-NDR8 to POD15-POD8 disabled).
1	Pulse output PO15 to PO8 enabled (transfer from NDR15-NDR8 to POD15-POD8 enabled).

NDERL

Bit	7	6	5	4	3	2	1	0
	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Next data enable 7 to 0

NDER7 to NDER0	
0	Pulse output PO7 to PO0 disabled (transfer from NDR7-NDR0 to POD7-POD0 disabled).
1	Pulse output PO7 to PO0 enabled (transfer from NDR7-NDR0 to POD7-POD0 enabled).

Short address mode

Bit	7	6	5	4	3	2	1	0
DMACR	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data Transfer Size

0	Byte-size transfer
1	Word-size transfer

Data Transfer Increment/Decrement

0	MAR is incremented after a data transfer • When DTSZ = 0, MAR is incremented by 1 after a transfer • When DTSZ = 1, MAR is incremented by 2 after a transfer
1	MAR is decremented after a data transfer • When DTSZ = 0, MAR is decremented by 1 after a transfer • When DTSZ = 1, MAR is decremented by 2 after a transfer

Data Transfer Factor

				Channel A	Channel B
0	0	0	0	—	
			1	Activated by A/D converter conversion end interrupt	
		1	0	—	Activated by $\overline{\text{DREQ}}$ pin falling edge input
			1	—	Activated by $\overline{\text{DREQ}}$ pin low-level input
	1	0	0	Activated by SCI channel 0 transmit-data-empty interrupt	
			1	Activated by SCI channel 0 reception complete interrupt	
		1	0	Activated by SCI channel 1 transmit-data-empty interrupt	
			1	Activated by SCI channel 1 reception complete interrupt	
1	0	0	0	Activated by TPU channel 0 compare match/input capture A interrupt	
			1	Activated by TPU channel 1 compare match/input capture A interrupt	
		1	0	Activated by TPU channel 2 compare match/input capture A interrupt	
			1	Activated by TPU channel 3 compare match/input capture A interrupt	
	1	0	0	Activated by TPU channel 4 compare match/input capture A interrupt	
			1	Activated by TPU channel 5 compare match/input capture A interrupt	
		1	0	—	
			1	—	

Data Transfer Direction

DMABCR SAE	Bit 4 DTDIR	Description
0	0	Transfer with MAR as source address and IOAR as destination address (initial value)
	1	Transfer with IOAR as source address and MAR as destination address
1	0	Transfer with MAR as source address and $\overline{\text{DACK}}$ pin as write strobe
	1	Transfer with $\overline{\text{DACK}}$ pin as read strobe and MAR as destination address

Repeat Enable

Bit 5 RPE	DMABCR DTIE	Description
0	0	Transfer in sequential mode (no transfer end interrupt) (initial value)
	1	Transfer in sequential mode (with transfer end interrupt)
1	0	Transfer in repeat mode (no transfer end interrupt)
	1	Transfer in idle mode (with transfer end interrupt)

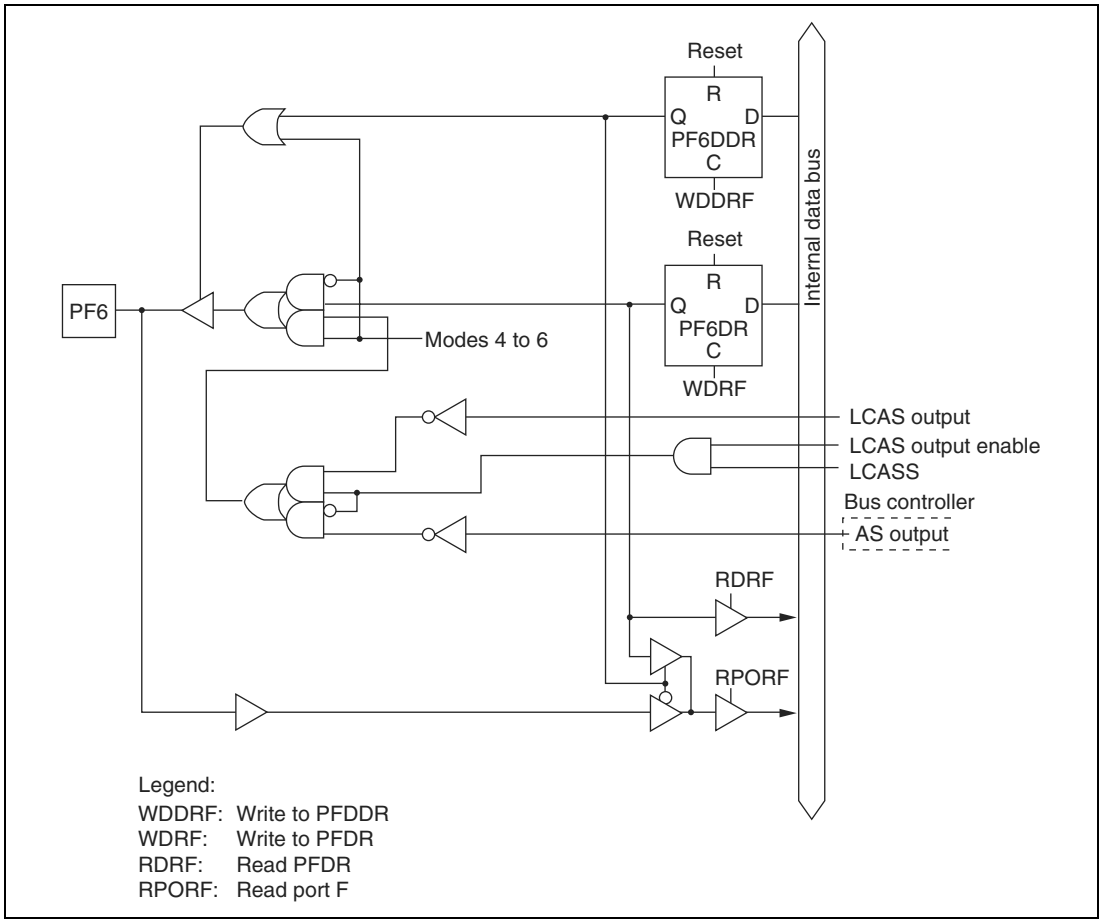


Figure C.11 (g) Port F Block Diagram (Pin PF6)

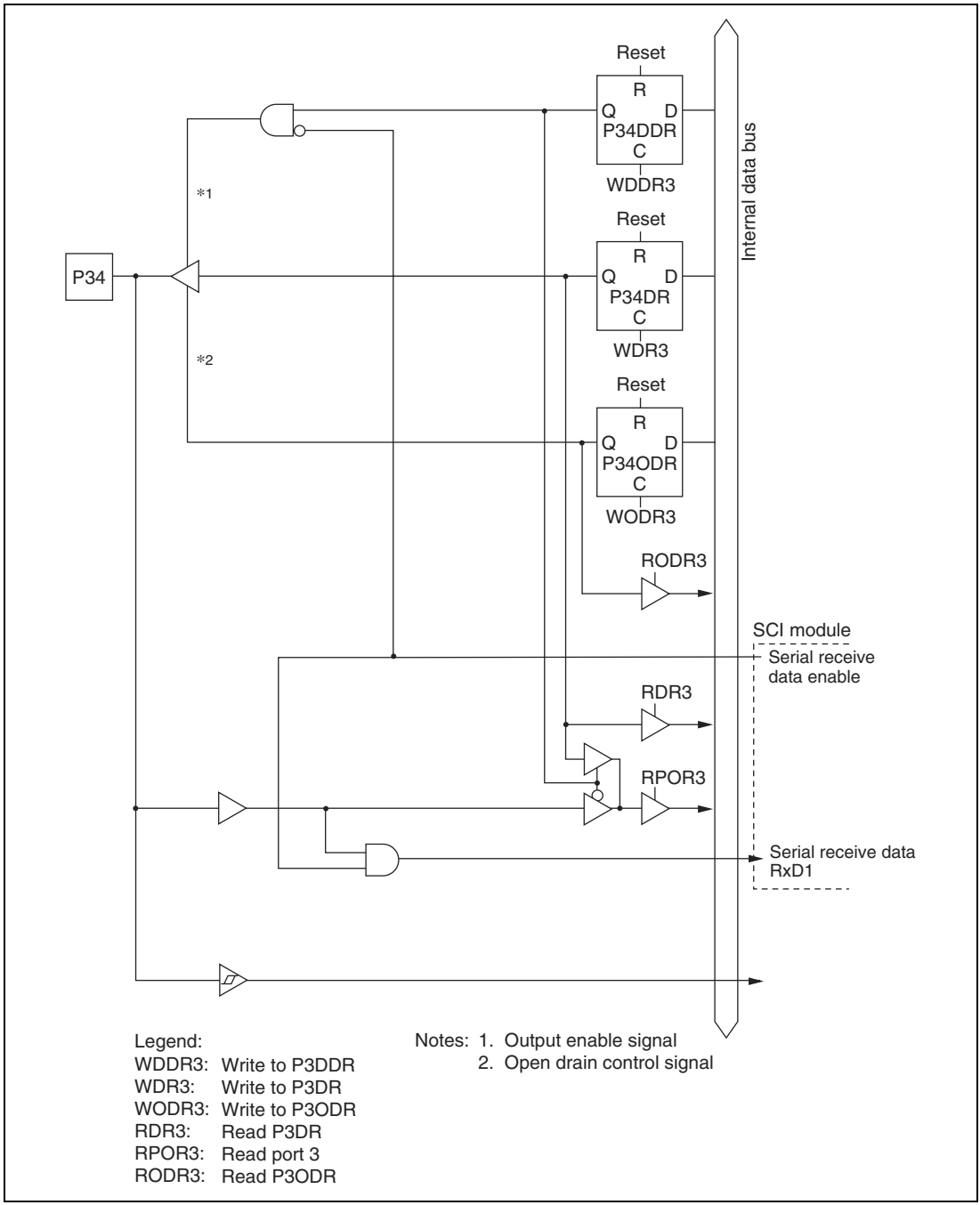


Figure C.14 (e) Port 3 Block Diagram (Pin P34)