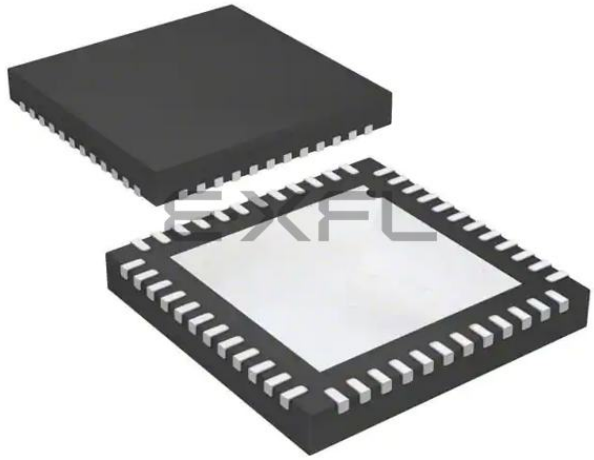

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9867qxa40xuma2

- Overtemperature protection
- Short circuit protection
- Loss of clock detection with fail safe mode entry for low system power consumption
- Temperature Range T_j = -40 °C to +150 °C
- Package VQFN-48 with LTI feature
- Green package (RoHS compliant)
- AEC qualified

Table 5 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

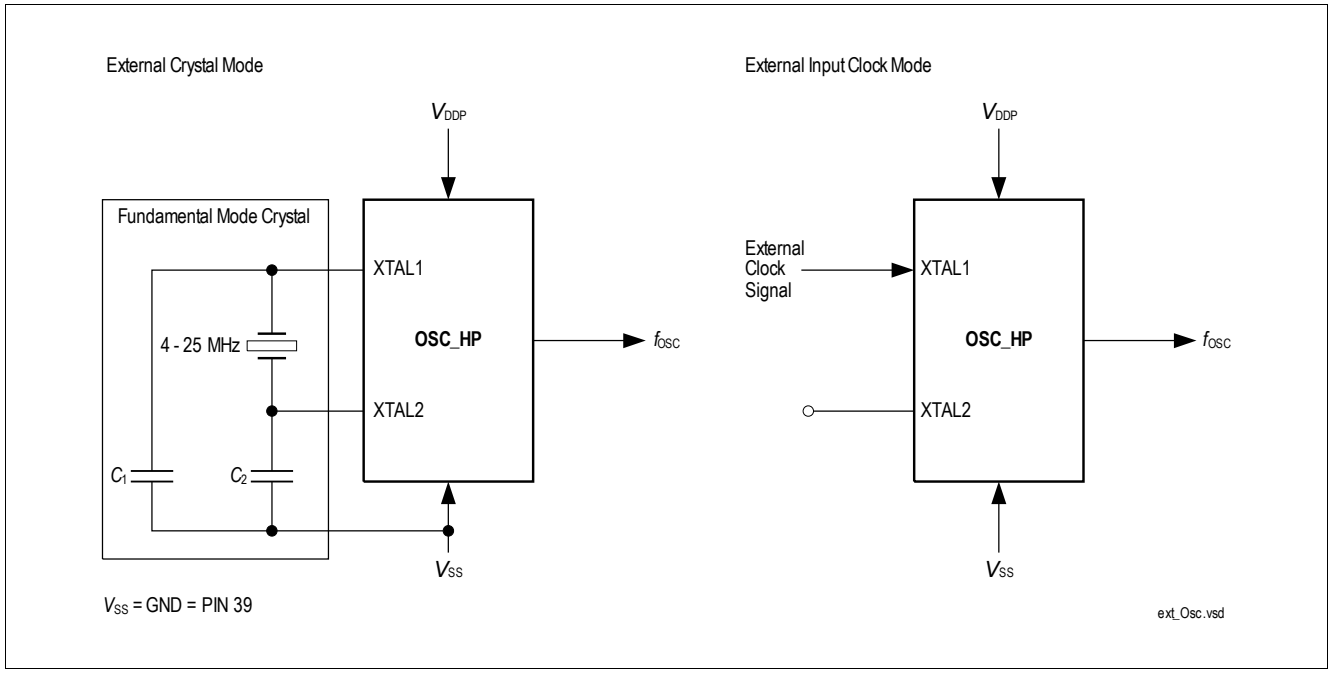

Figure 10 TLE9867QXA40 External Circuitry for the OSC_HP

8.2 Introduction

The ARM Cortex-M3 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex family processors, the Cortex-M3 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex-M3 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 12 shows the functional blocks of the Cortex-M3.

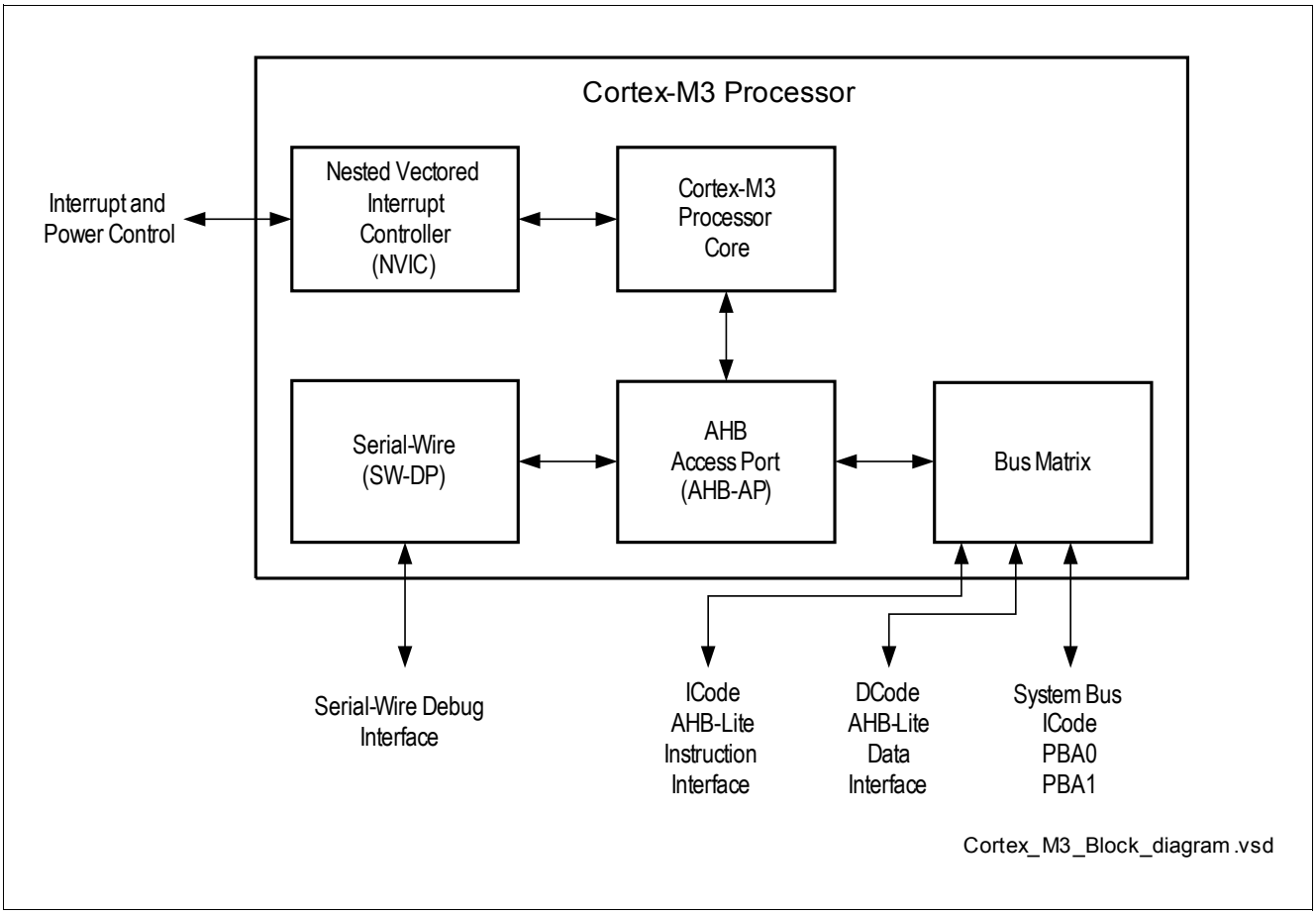

Figure 12 Cortex-M3 Block Diagram

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

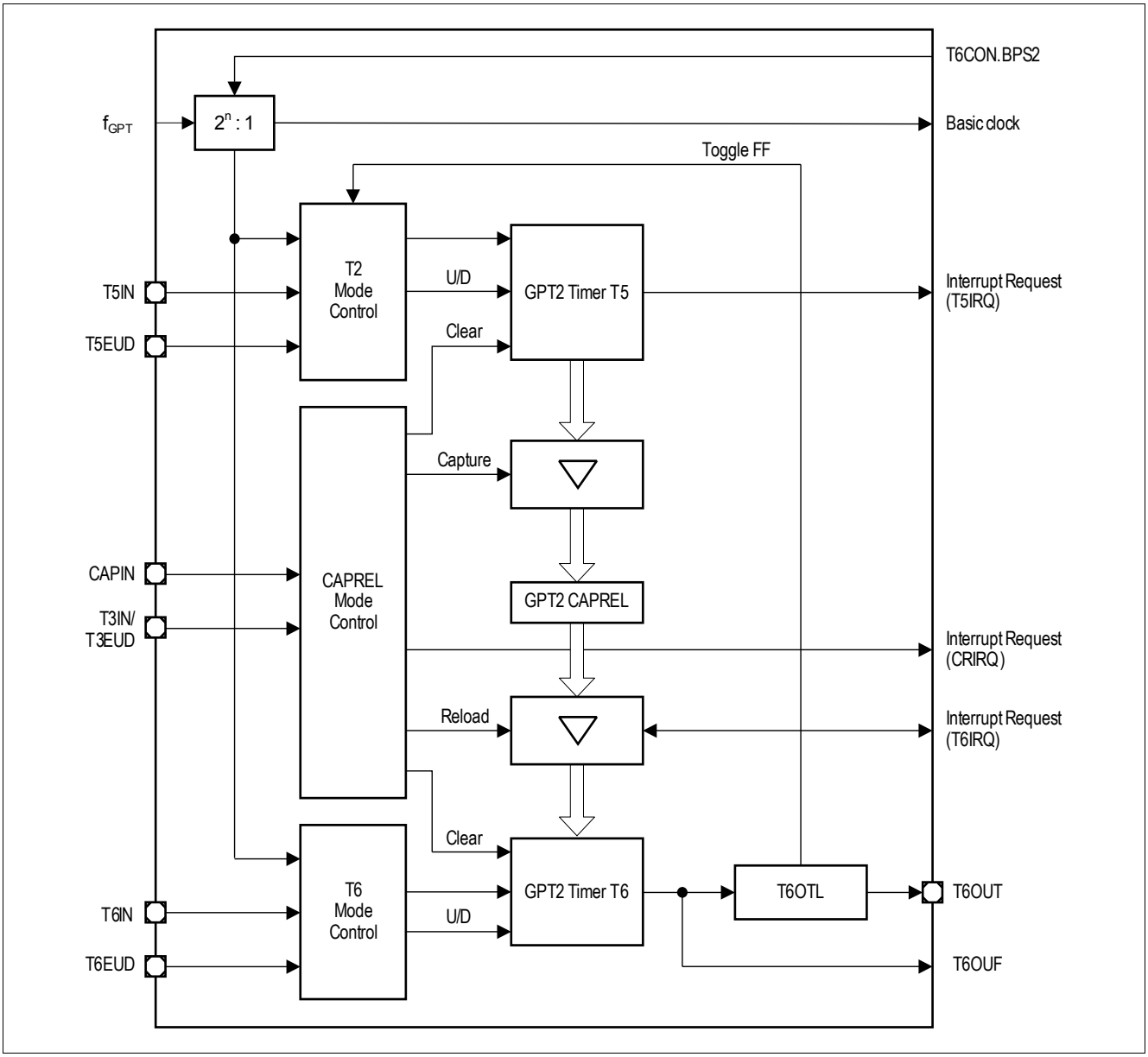

Figure 20 GPT2 Block Diagram (n = 1 … 4)

21 High-Speed Synchronous Serial Interface (SSC1/SSC2)

21.1 Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a “receiver full” condition
  - On an error condition (receive, phase, baud rate, transmission error)

21.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on TXD and RXD lines, which are normally connected to the MTSR (MasterTransmit/Slave Receive) and MRST (Master Receive/Slave Transmit) pins. The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

21.2.1 Block Diagram

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

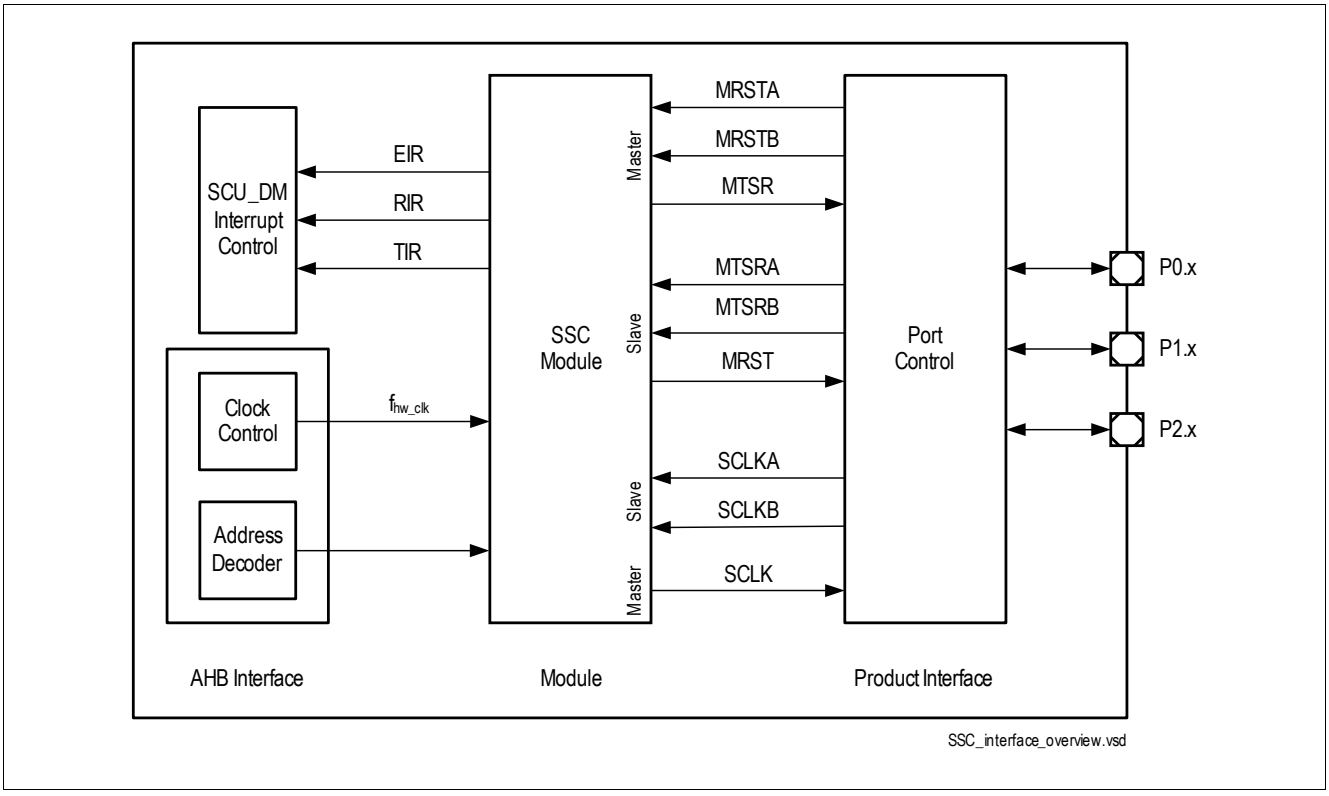

Figure 24 SSC Interface Diagram

22.2.1 Block Diagram

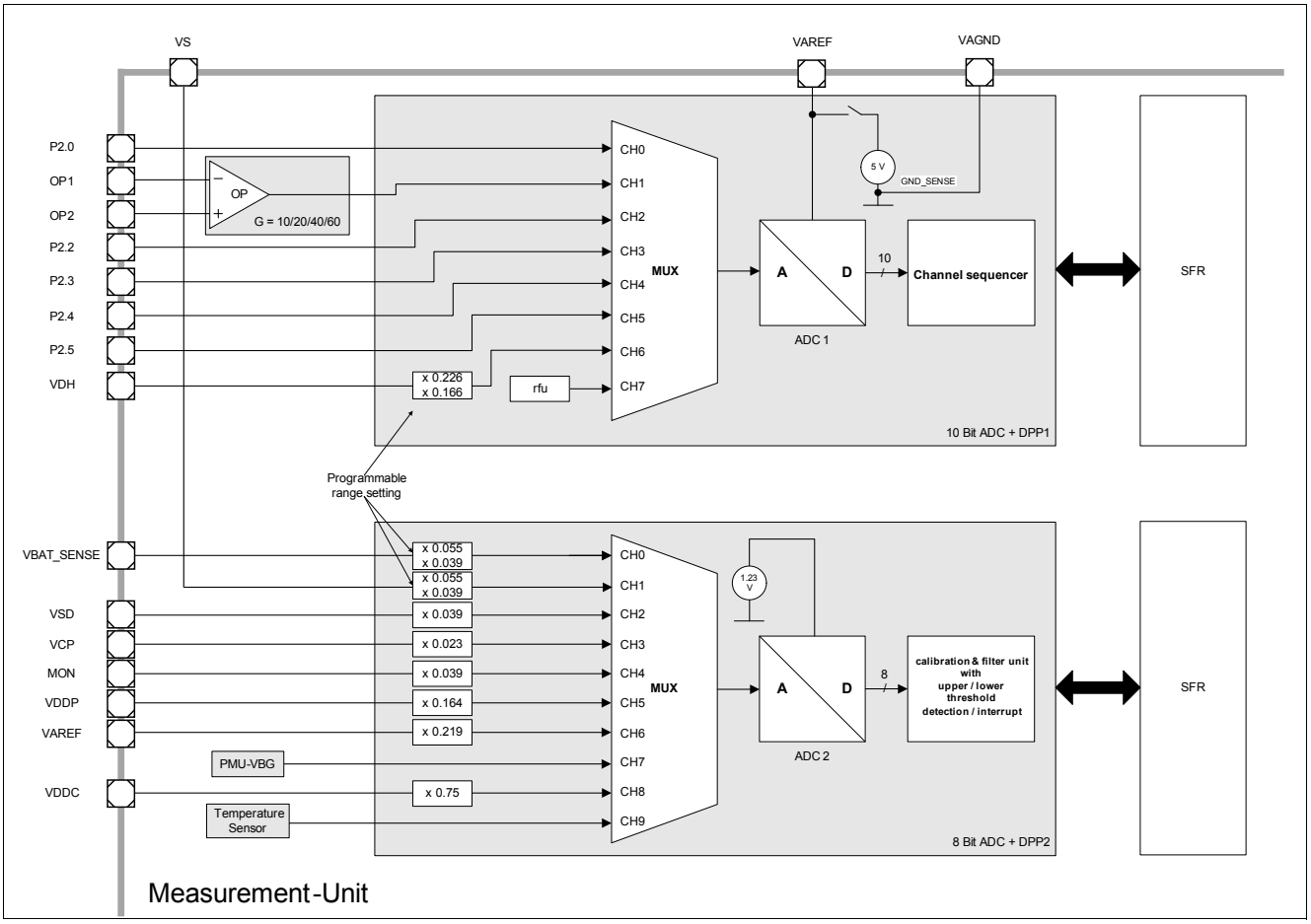

Figure 25 Measurement Unit-Overview (with opamp)

26 Bridge Driver (incl. Charge Pump)

26.1 Features

The MOSFET Driver is intended to drive external normal level NFET transistors in bridge configuration. The driver provides many diagnostic possibilities to detect faults.

Functional Features

- External Power NFET Transistor Driver Stage with driver capability for max. 100 nC gate charge @ 25 kHz switching frequency.
- Implemented adjustable cross conduction protection.
- Supply voltage (VSD) monitoring incl. adjustable over- and undervoltage shutdown with configurable interrupt signalling.
- VSD operating range down to 5.4 V
- VDS comparators for short circuit detection in on- and off-state
- Open-Load detection in off-state

26.2 Introduction

The MOSFET Driver Stage can be used for controlling external Power NFET Transistors (normal level). The module output is controlled by SFR or System PWM Machine (CCU6).

28 Application Information

28.1 H-Bridge Driver

Figure 31 shows the TLE9867QXA40 in an electric drive application setup controlling an H-Bridge motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

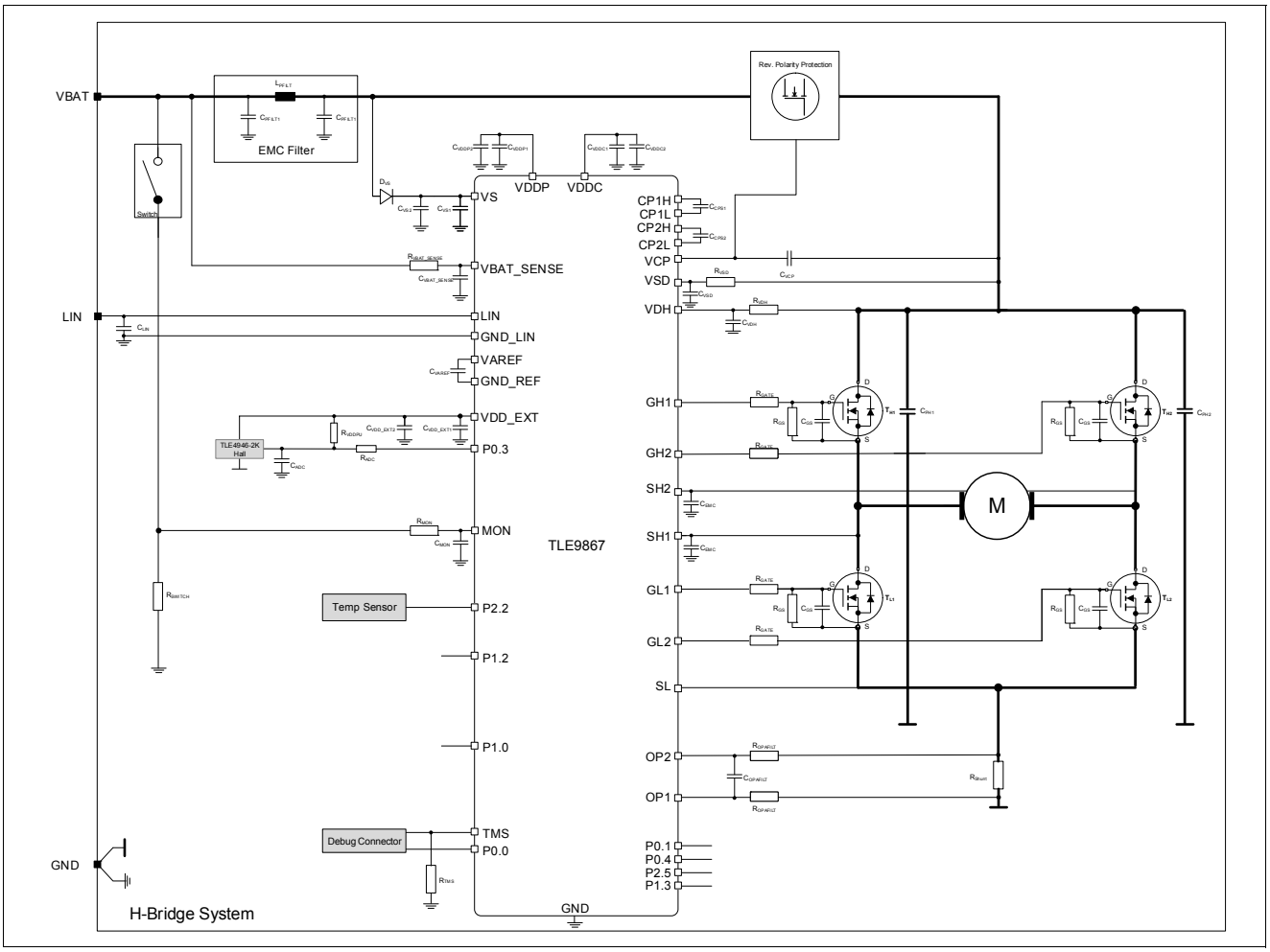

Figure 31 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

Table 15 External Components (BOM)

Symbol	Function	Component
C_{VS1}	Blocking capacitor at VS pin	≥ 100 nF Ceramic, ESR < 1 Ω
C_{VS2}	Blocking capacitor at VS pin	> 2.2 µF Elco[1)]
C_{VDDP}	Blocking capacitor at VDDP pin	470 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VDD_EXT}	Blocking capacitor at VDDEXT pin	100nF, Ceramic ESR < 1 Ω
C_{VDDC}	Blocking capacitor at VDDC pin	470 nF + 100 nF Ceramic, ESR < 1 Ω
C_{VAREF}	Blocking capacitor at VAREF pin	100 nF, Ceramic ESR < 1 Ω
C_{LIN}	Standard C for LIN slave	220 pF
C_{VSD}	Filter C for charge pump end driver	1 µF
C_{CPS1}	Charge pump capacitor	220 nF
C_{CP2S}	Charge pump capacitor	220 nF
C_{VCP}	Charge pump capacitor	470 nF
C_{MON1}	Filter C for ISO pulses	10 nF
C_{VDH}	Capacitor	1 nF
C_{PH1}	Capacitor	220 µF
C_{PH2}	Capacitor	220 µF
$C_{OPAFILT}$	Capacitor	100 nF
C_{EMCP1}	Capacitor	1 nF
C_{EMCP2}	Capacitor	1 nF
C_{PFILT1}, C_{PFILT2}	Capacitor	10 µF
C_{VBAT_SENSE}	Capacitor	10 nF
R_{MON}	Resistor at MON pin	1 kΩ
R_{VSD}	Limitation of reverse current due to transient (-2V, 8ms) max. ratings of the VSD pin has to be met, alternatively the resistor shall be replaced by a diode	2 Ω
R_{VDH}	Resistor	1 kΩ
R_{GATE}	Resistor	2 Ω
$R_{OPAFILT}$	Resistor	12 Ω
R_{VBAT_SENSE}	Resistor	
R_{SH1}	Resistor	optional
R_{SH2}	Resistor	optional
L_{PFILT}		
D_{VS}	Reverse-polarity protection diode	–

1) The capacitor must be dimensioned so as to ensure that flash operations modifying the content of the flash are never interrupted (e.g. in case of power loss).

29 Electrical Characteristics

This chapter includes all relevant electrical characteristics of the product TLE9867QXA40.

29.1 General Characteristics

29.1.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages – Supply Pins							
Supply voltage – VS	V_S	-0.3	–	40	V	Load dump	P_1.1.1
Supply voltage – VSD	V_{SD}	-0.3	–	48	V	–	P_1.1.2
Supply voltage – VSD	$V_{SD\_max\_extend}$	-2.8	–	48	V	Series resistor R_{VSD} = 2.2 Ω, t = 8 ms [2)]	P_1.1.32
Voltage range – VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_1.1.3
Voltage range – VDDP	$V_{DDP\_max\_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≥ 1V/µs; duration: t ≤ 150µs; C_{VDDP} ≤ 570 nF	P_1.1.41
Voltage range – VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_1.1.4
Voltage range – VDDEXT	$V_{DDEXT\_max\_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≥ 1V/µs; duration: t ≤ 150µs; C_{VDDEXT} ≤ 570 nF	P_1.1.42
Voltage range – VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_1.1.5
Voltages – High Voltage Pins							
Battery voltage VBAT_SENSE	V_{BAT_SENSE}	-28	–	40	V	[3)]	P_1.1.6
Input voltage at LIN	V_{LIN}	-28	–	40	V	–	P_1.1.7
Input voltage at MON	$V_{MON\_maxrate}$	-28	–	40	V	[4)]	P_1.1.8
Input voltage at VDH	$V_{VDH\_maxrate}$	-2.8	–	40	V	[5)]	P_1.1.38
Voltage range at GHx	V_{GH}	-8.0	–	48	V	[6)]	P_1.1.9
Voltage range at GHx vs. SHx	V_{GHvsSH}	14	–	–	V	–	P_1.1.44
Voltage range at SHx	V_{SH}	-8.0	–	48	V	–	P_1.1.11
Voltage range at GLx	V_{GL}	-8.0	–	48	V	[7)]–	P_1.1.13
Voltage range at GLx vs. SL	V_{GLvsSL}	14	–	–	V	–	P_1.1.45

29.1.2 Functional Range

Table 18 Functional Range

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended supply voltage in Active Mode	$V_{S\_AM\_extend}$	28	–	40	V	1) Functional with parameter deviation	P_1.2.16
Supply voltage in Active Mode for MOSFET Driver Supply	V_{SD_AM}	5.4	–	28	V		P_1.2.18
Extended supply voltage in Active Mode for MOSFET Driver Supply	$V_{SD\_AM\_extend}$	28	–	32	V	1)3)Functional with parameter deviation	P_1.2.17
Specified supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	5.5	–	18	V	Parameter Specification	P_1.2.2
Extended supply voltage for LIN Transceiver	$V_{S\_AM\_LIN}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.14
Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation)	V_{S_AMmin}	3.0	–	5.5	V	2)	P_1.2.3
Supply voltage in Sleep Mode	V_{S_Sleep}	3.0	–	28	V	–	P_1.2.4
Supply voltage transients slew rate	dV_S/dt	-1	–	1	V/µs	3)	P_1.2.5
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	3)	P_1.2.7
Operating frequency	f_{sys}	5	–	40	MHz	4)	P_1.2.20
Junction temperature	T_j	-40	–	150	°C	–	P_1.2.9

1) This operation voltage range is only allowed for a short duration: t_{max} ≤ 400 ms (continuous operation at this voltage is not allowed), f_{sys} = 24 MHz, I_{VDDP} = 10 mA, I_{VDDEXT} = 5 mA. In addition, the power dissipation caused by the Charge Pump + MOSFET driver have to be considered.

2) Reduced functionality (e.g. cranking pulse) - Parameter deviation possible.

3) Not subject to production test, specified by design.

4) Function not specified when limits are exceeded.

Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	110	µA	T_J = -40°C to 85°C; V_S = 5.5 V to 18V; t_{Cyclic_ON} = 4ms; t_{Cyclic_OFF} = 2048 ms;[2]	P_1.3.4
Current consumption in Stop Mode	I_{Stop}	–	110	160	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_S = 5.5 V to 18V	P_1.3.10
Current consumption in Stop Mode-Extended temperature range 1	I_{Stop_extend}	–	600	1800	µA	System in Stop Mode, microcontroller not clocked, Wake capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40 °C to 150 °C; V_S = 5.5 V to 18 V	P_1.3.20

1) Current on V_S, ADC1/2 active, timer running, LIN active (recessive).

2) Incl. leakage currents form VBAT_SENSE, VDH, VSD and MON

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 35 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-79	–	79	mV	V_S = 5.5V to 18V	P_8.1.48
8-Bit ADC Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	1.01	1.07	1.18	V		P_8.1.73
Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: V_{DDC}	ATT_{VDDC}	–	0.75	–		–	P_8.1.34
Nominal operating input voltage range V_{DDC}	$V_{DDC,range}$	0.8	–	1.64	V	1)	P_8.1.53
Accuracy of V_{DDC} sense after calibration	ΔV_{DDC_SENSE}	-22	–	22	mV	V_S = 5.5 to 18V	P_8.1.6
VDH Input Voltage Measurement $V_{VDH10BITADC}$							
VDH Input to output voltage attenuation:	ATT_{VDH_1}	–	0.166	–		SFR setting 1	P_8.1.64
VDH Input to output voltage attenuation:	ATT_{VDH_2}	–	0.224	–		SFR setting 2	P_8.1.65
VDH Input to output voltage attenuation:	ATT_{VDH_3}	-	0.226	-		1)SFR setting 2 Tj = -40..85°C	P_8.1.75
Nominal operating input voltage range V_{VDH}, Range 1	$V_{VDH,range1}$	–	–	30		SFR setting 1	P_8.1.66
Nominal operating input voltage range V_{VDH}, Range 2	$V_{VDH,range2}$	–	–	20		SFR setting 2	P_8.1.67
V_{VDH} 10-bit ADC, Range 1	$\Delta V_{VDHADC10B}$	-300	–	300	mV	V_{DH}= 5.5 to 17.5V, T_j = -40..150°C	P_8.1.39
V_{VDH} 10-bit ADC, Range 3	$\Delta V_{VDHADC10B}$	-200	–	200	mV	1)VDH= 5.5V to 17.5V, Tj = -40..85°C ATT_{VDH_3}	P_8.1.71

29.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 40 A/D Converter Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	24	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	1)4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	1)	P_9.2.6
Wakeup time from analog powerdown, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wakeup time from analog powerdown, slow mode	t_{WAS}	–	–	15	µs	1)5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	-2	±1	+2	counts	6)7)Reference is internal V_{AREF}	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	-12	±6	+12	counts	7)8)Reference is internal V_{AREF}	P_9.2.22
DNL error	EA_{DNL}	-3	±0.8	+3	counts	–	P_9.2.10
INL error	$EA_{INL\_int\_VAREF}$	-5	±0.8	+5	counts	Reference is internal V_{AREF}	P_9.2.11
Gain error	$EA_{GAIN\_int\_VAREF}$	-10	±0.4	+10	counts	Reference is internal V_{AREF}	P_9.2.12
Offset error	EA_{OFF}	-2	±0.5	+2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	1)5)9)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	1)5)9)	P_9.2.15
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	1)5)9)	P_9.2.16

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.30
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.41
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.42
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.43
Drain source monitoring							
Drain source monitoring threshold	$V_{DSMONVTH}$	–	–	–	V	DRV_CTRL3.DSMONVTH<2:0> xxx	P_12.1.46
		0.07	0.25	0.40		000	
		0.35	0.50	0.650		001	
		0.55	0.75	0.90		010	
		0.65	1.00	1.25		011	
		0.90	1.25	1.45		100	
		1.00	1.5	1.80		101	
		1.20	1.75	2.10		110	
		1.40	2.00	2.40		111	
Open load diagnosis currents							
Pull-up diagnosis current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnosis current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin1}	8.5	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, C_{CP1}, C_{CP2} = 220 nF, Bridge Driver enabled	P_12.1.53
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V ≤ V_{VSD} ≤ 28, I_{CP}=10mA, C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.49

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Turn ON Time	t_{ON_VCP}	10	24	40	us	8 V ≤ V_{VSD} ≤ 28, I_{CP}=2.5mA, (25%) of V_{CP} 1)4), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.59
Rise time	t_{rise_VCP}	20	60	88	us	8 V ≤ V_{VSD} ≤ 28, I_{CP}=2.5mA, (25-75%) of V_{CP} 1)5), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.60

1) Not subject to production test.
2) The condition I_{CP} =2,5 mA emulates anH-Bridge Driver with 4 MOSFET switching at 20 KHz with a C_{Load}=3.3nF. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.
3) This resistance is connected through a diode between SHx and GHx to ground.
4) This time applies when Bit DRV_CP_CTRL_STS.bit.CP_EN is set
5) This time applies when Bit DRV_CP_CLK_CTRL.bit.CPCLK_EN is set

29.13 Operational Amplifier

29.13.1 Electrical Characteristics

Table 43 Electrical Characteristics Operational Amplifier

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Differential gain (uncalibrated)	G	 9.5 19 38 57	 10 20 40 60	 10.5 21 42 63		Gain settings GAIN<1:0>: 00 01 10 11	P_13.1.6
Differential input operating voltage range OP2 - OP1	V_{IX}	-1.5 / G	–	1.5 / G	V	G is the Gain specified below	P_13.1.1
Operating. common mode input voltage range (referred to GND (OP2 - GND) or (OP1 - GND)	V_{CM}	-2.0	–	2.0	V	Input common mode has to be checked in evaluation if it fits the required range	P_13.1.2
Max. input voltage range (referred to GND (OP_2 - GND) or (OP1 - GND)	V_{IX_max}	-7.0	–	7.0	V	Max. rating of operational amplifier inputs, where measurement is not done	P_13.1.3
Single ended output voltage range (linear range)	V_{OUT}	V_{ZERO} - 1.5	–	V_{ZERO} + 1.5	V	[1)2)] typ. output offset voltage 2 V ± 1.5V	P_13.1.4
Linearity error	E_{PWM}	-15	–	15	mV	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.5
Linearity error	$E_{PWM\_\%}$	-1.0	–	1.0	%	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.24
Gain drift		-1	–	1	%	Gain drift after calibration at G = 10.	P_13.1.7
Adjusted output offset voltage	V_{OOS}	-40	10	40	mV	V_{AIP}= V_{AIN} = 0 V and G = 40.	P_13.1.17

Table 43 Electrical Characteristics Operational Amplifier (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
DC input voltage common mode rejection ratio	DC-CMRR	58	80	–	dB	CMRR (in dB)=-20*log (differential mode gain/ common mode gain) V_{CMI}= -2V... 2V, V_{AIP}-V_{AIN}=0V	P_13.1.8
Settling time to 98%	T_{SET}	–	800	1400	ns	Derived from 80 - 20 % rise fall times for ± 2V overload condition (3 Tau value of settling time constant)[2)]	P_13.1.9
Current Sense Amplifier Input Resistance @ OP1, OP2	$R_{in\_OP1\_OP2}$	1	1.25	1.5	kΩ	[2)]–	P_13.1.25