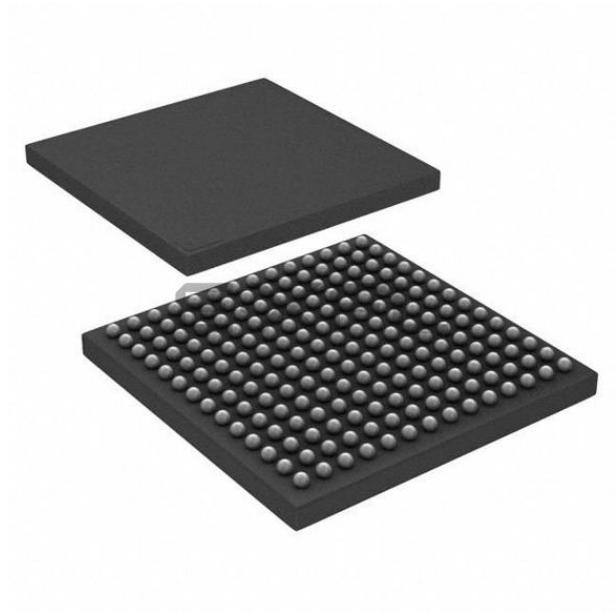

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-TFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d225c-d1m-cu

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2. DDR2-SDRAM Features

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ±0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-directional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Auto-refresh and Self-refresh modes
- Precharged Powerdown and Active Powerdown
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

4. Chip Identifier

Table 4-1. SAMA5D2 SIP Chip ID Registers

Chip Name	CHIPID_CIDR	CHIPID_EXID
SAMA5D225C-D1M	0x8A5C08C2	0x00000053
SAMA5D27C-D5M		0x00000032
SAMA5D27C-D1G		0x00000033
SAMA5D28C-D1G		0x00000013

5. Package and Ballout

The SAMA5D2 SIP is available in the packages listed below.

Important: SAMA5D2 SIP devices are not pin-to-pin compatible with SAMA5D2 devices.

For mechanical characteristics of the TFBGA196, refer to the SAMA5D2 Series Datasheet, ref. no. DS60001476, available via www.microchip.com.

For mechanical characteristics of the TFBGA289, see Mechanical Characteristics.

Table 5-1. Packages

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA196	196	0.75 mm	11 x 11 (mm)
TFBGA289	289	0.8 mm	14 x 14 (mm)

Table 5-2. Ball Description

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
U13	M8	VDDSDMMC	GPIO_EMMC	PA0	I/O	–	–	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
								B	QSPI0_SCK	O	1	
								F	D0	I/O	2	
N7	F7	VDDSDMMC	GPIO_EMMC	PA1	I/O	–	–	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
								B	QSPI0_CS	O	1	
								F	D1	I/O	2	
U14	L8	VDDSDMMC	GPIO_EMMC	PA2	I/O	–	–	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO0	I/O	1	
								F	D2	I/O	2	
T13	G8	VDDSDMMC	GPIO_EMMC	PA3	I/O	–	–	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO1	I/O	1	
								F	D3	I/O	2	
U15	K8	VDDSDMMC	GPIO_EMMC	PA4	I/O	–	–	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO2	I/O	1	
								F	D4	I/O	2	
U16	P9	VDDSDMMC	GGPIO_EMMC	PA5	I/O	–	–	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
								B	QSPI0_IO3	I/O	1	
								F	D5	I/O	2	
U17	P10	VDDSDMMC	GPIO_EMMC	PA6	I/O	–	–	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
								B	QSPI1_SCK	O	1	
								D	TIOA5	I/O	1	
								E	FLEXCOM2_IO0	I/O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
T14	G10	VDDIOP1	GPIO	PA23	I/O	–	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
								B	D1	I/O	1	
								C	TDI	I	4	
								D	SPI1_MOSI	I/O	2	
								F	QSPI0_CS	O	3	
R17	P13	VDDIOP1	GPIO_IO	PA24	I/O	–	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
								B	D2	I/O	1	
								C	TDO	O	4	
								D	SPI1_MISO	I/O	2	
								F	QSPI0_IO0	I/O	3	
R16	H10	VDDIOP1	GPIO_IO	PA25	I/O	–	–	A	FLEXCOM1_IO3	O	1	PIO, I, PU, ST
								B	D3	I/O	1	
								C	TMS	I	4	
								D	SPI1_NPCS0	I/O	2	
								F	QSPI0_IO1	I/O	3	
P17	L10	VDDIOP1	GPIO_IO	PA26	I/O	–	–	A	FLEXCOM1_IO4	O	1	PIO, I, PU, ST
								B	D4	I/O	1	
								C	NTRST	I	4	
								D	SPI1_NPCS1	O	2	
								F	QSPI0_IO2	I/O	3	
R15	P14	VDDIOP1	GPIO_IO	PA27	I/O	–	–	A	TIOA1	I/O	2	PIO, I, PU, ST
								B	D5	I/O	1	
								C	SPI0_NPCS2	O	2	
								D	SPI1_NPCS2	O	2	
								E	SDMMC1_RSTN	O	1	
								F	QSPI0_IO3	I/O	3	
R14	N12	VDDIOP1	GPIO	PA28	I/O	–	–	A	TIOB1	I/O	2	PIO, I, PU, ST
								B	D6	I/O	1	
								C	SPI0_NPCS3	O	2	
								D	SPI1_NPCS3	O	2	
								E	SDMMC1_CMD	I/O	1	
								F	CLASSD_L0	O	1	
P14	M12	VDDIOP1	GPIO	PA29	I/O	–	–	A	TCLK1	I	2	PIO, I, PU, ST
								B	D7	I/O	1	
								C	SPI0_NPCS1	O	2	
								E	SDMMC1_WP	I	1	
								F	CLASSD_L1	O	1	
R13	N11	VDDIOP1	GPIO	PA30	I/O	–	–	B	NWE/NANDWE	O	1	PIO, I, PU, ST
								C	SPI0_NPCS0	I/O	2	
								D	PWMH0	O	1	
								E	SDMMC1_CD	I	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	CLASSD_L2	O	1	
P13	M11	VDDIOP1	GPIO	PA31	I/O	–	–	B	NCS3	O	1	PIO, I, PU, ST
								C	SPI0_MISO	I/O	2	
								D	PWML0	O	1	
								F	CLASSD_L3	O	1	
F5	E6	VDDIOP0	GPIO	PB0	I/O	–	–	B	A21/NANDALE	O	1	PIO, I, PU, ST
								C	SPI0_MOSI	I/O	2	
								D	PWMH1	O	1	
C8	D6	VDDIOP0	GPIO	PB1	I/O	–	–	B	A22/NANDCLE	O	1	PIO, I, PU, ST
								C	SPI0_SPCK	I/O	2	
								D	PWML1	O	1	
								F	CLASSD_R0	O	1	
C7	C6	VDDIOP0	GPIO	PB2	I/O	–	–	B	NRD/NANDOE	O	1	PIO, I, PU, ST
								D	PWMFI0	I	1	
								F	CLASSD_R1	O	1	
B8	C5	VDDIOP0	GPIO	PB3	I/O	–	–	A	URXD4	I	1	PIO, I, PU, ST
								B	D8	I/O	1	
								C	IRQ	I	3	
								D	PWMEXTRG1	I	1	
								F	CLASSD_R2	O	1	
B7	D5	VDDIOP0	GPIO	PB4	I/O	–	–	A	UTXD4	O	1	PIO, I, PU, ST
								B	D9	I/O	1	
								C	FIQ	I	4	
								F	CLASSD_R3	O	1	
A10	D7	VDDIOP0	GPIO_QSPI	PB5	I/O	–	–	A	TCLK2	I	1	PIO, I, PU, ST
								B	D10	I/O	1	
								C	PWMH2	O	1	
								D	QSPI1_SCK	O	2	
								F	GTSUCOMP	O	3	
A9	C8	VDDIOP0	GPIO	PB6	I/O	–	–	A	TIOA2	I/O	1	PIO, I, PU, ST
								B	D11	I/O	1	
								C	PWML2	O	1	
								D	QSPI1_CS	O	2	
								F	GTXER	O	3	
D5	D9	VDDIOP0	GPIO_IO	PB7	I/O	–	–	A	TIOB2	I/O	1	PIO, I, PU, ST
								B	D12	I/O	1	
								C	PWMH3	O	1	
								D	QSPI1_IO0	I/O	2	
								F	GRXCK	I	3	
E5	C7	VDDIOP0	GPIO_IO	PB8	I/O	–	–	A	TCLK3	I	1	PIO, I, PU, ST
								B	D13	I/O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	PWML3	O	1	
								D	QSPI1_IO1	I/O	2	
								F	GCRS	I	3	
C6	C9	VDDIOP0	GPIO_IO	PB9	I/O	–	–	A	TIOA3	I/O	1	PIO, I, PU, ST
								B	D14	I/O	1	
								C	PWMFI1	I	1	
								D	QSPI1_IO2	I/O	2	
								F	GCOL	I	3	
A8	F6	VDDIOP0	GPIO_IO	PB10	I/O	–	–	A	TIOB3	I/O	1	PIO, I, PU, ST
								B	D15	I/O	1	
								C	PWMEXTRG2	I	1	
								D	QSPI1_IO3	I/O	2	
								F	GRX2	I	3	
A7	B9	VDDIOP0	GPIO	PB11	I/O	–	–	A	LCDDAT0	O	1	PIO, I, PU, ST
								B	A0/NBS0	O	1	
								C	URXD3	I	3	
								D	PDMIC_DAT		2	
								F	GRX3	I	3	
B6	B8	VDDIOP0	GPIO	PB12	I/O	–	–	A	LCDDAT1	O	1	PIO, I, PU, ST
								B	A1	O	1	
								C	UTXD3	O	3	
								D	PDMIC_CLK		2	
								F	GTX2	O	3	
C5	B7	VDDIOP0	GPIO	PB13	I/O	–	–	A	LCDDAT2	O	1	PIO, I, PU, ST
								B	A2	O	1	
								C	PCK1	O	3	
								F	GTX3	O	3	
A6	G6	VDDIOP0	GPIO_QSPI	PB14	I/O	–	–	A	LCDDAT3	O	1	PIO, I, PU, ST
								B	A3	O	1	
								C	TK1	I/O	2	
								D	I2SC1_MCK	O	1	
								E	QSPI1_SCK	O	3	
								F	GTXCK	I/O	3	
E4	B5	VDDIOP0	GPIO	PB15	I/O	–	–	A	LCDDAT4	O	1	PIO, I, PU, ST
								B	A4	O	1	
								C	TF1	I/O	2	
								D	I2SC1_CK	I/O	1	
								E	QSPI1_CS	O	3	
								F	GTXEN	O	3	
B5	C4	VDDIOP0	GPIO_IO	PB16	I/O	–	–	A	LCDDAT5	O	1	PIO, I, PU, ST
								B	A5	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								B	A12	O	1	
								C	RD0	I	1	
								D	TIOB2	I/O	2	
								E	FLEXCOM3_IO0	I/O	3	
								F	GMDIO	I/O	3	
E2	E3	VDDIOP0	GPIO	PB24	I/O	–	–	A	LCDDAT13	O	1	PIO, I, PU, ST
								B	A13	O	1	
								C	RK0	I/O	1	
								D	TCLK2	I	2	
								E	FLEXCOM3_IO3	O	3	
								F	ISC_D10	I	3	
A3	E2	VDDIOP0	GPIO	PB25	I/O	–	–	A	LCDDAT14	O	1	PIO, I, PU, ST
								B	A14	O	1	
								C	RF0	I/O	1	
								E	FLEXCOM3_IO4	O	3	
								F	ISC_D11	I	3	
G3	D4	VDDIOP0	GPIO	PB26	I/O	–	–	A	LCDDAT15	O	1	PIO, I, PU, ST
								B	A15	O	1	
								C	URXD0	I	1	
								D	PDMIC_DAT		1	
								F	ISC_D0	I	3	
F4	C3	VDDIOP0	GPIO	PB27	I/O	–	–	A	LCDDAT16	O	1	PIO, I, PU, ST
								B	A16	O	1	
								C	UTXD0	O	1	
								D	PDMIC_CLK		1	
								F	ISC_D1	I	3	
D2	D2	VDDIOP0	GPIO	PB28	I/O	–	–	A	LCDDAT17	O	1	PIO, I, PU, ST
								B	A17	O	1	
								C	FLEXCOM0_IO0	I/O	1	
								D	TIOA5	I/O	2	
								F	ISC_D2	I	3	
G8	B3	VDDIOP0	GPIO	PB29	I/O	–	–	A	LCDDAT18	O	1	PIO, I, PU, ST
								B	A18	O	1	
								C	FLEXCOM0_IO1	I/O	1	
								D	TIOB5	I/O	2	
								F	ISC_D3	I	3	
C2	F3	VDDIOP0	GPIO	PB30	I/O	–	–	A	LCDDAT19	O	1	PIO, I, PU, ST
								B	A19	O	1	
								C	FLEXCOM0_IO2	I/O	1	
								D	TCLK5	I	2	
								F	ISC_D4	I	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
G7	A2	VDDIOP0	GPIO	PB31	I/O	–	–	A	LCDDAT20	O	1	PIO, I, PU, ST
								B	A20	O	1	
								C	FLEXCOM0_IO3	O	1	
								D	TWD0	I/O	1	
								F	ISC_D5	I	3	
N10	L13	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDDAT21	O	1	PIO, I, PU, ST
								B	A23	O	1	
								C	FLEXCOM0_IO4	O	1	
								D	TWCK0	I/O	1	
								F	ISC_D6	I	3	
N11	H11	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDDAT22	O	1	PIO, I, PU, ST
								B	A24	O	1	
								C	CANTX0	O	1	
								D	SPI1_SPCK	I/O	1	
								E	I2SC0_CK	I/O	1	
								F	ISC_D7	I	3	
N9	L11	VDDIOP1	GPIO	PC2	I/O	–	–	A	LCDDAT23	O	1	PIO, I, PU, ST
								B	A25	O	1	
								C	CANRX0	I	1	
								D	SPI1_MOSI	I/O	1	
								E	I2SC0_MCK	O	1	
								F	ISC_D8	I	3	
M10	F13	VDDIOP1	GPIO	PC3	I/O	–	–	A	LCDPWM	O	1	PIO, I, PU, ST
								B	NWAIT	I	1	
								C	TIOA1	I/O	1	
								D	SPI1_MISO	I/O	1	
								E	I2SC0_WS	I/O	1	
								F	ISC_D9	I	3	
N15	G14	VDDIOP1	GPIO	PC4	I/O	–	–	A	LCDDISP	O	1	PIO, I, PU, ST
								B	NWR1/NBS1	O	1	
								C	TIOB1	I/O	1	
								D	SPI1_NPCS0	I/O	1	
								E	I2SC0_DI0	I	1	
								F	ISC_PCK	I	3	
M16	J14	VDDIOP1	GPIO	PC5	I/O	–	–	A	LCDVSYNC	O	1	PIO, I, PU, ST
								B	NCS0	O	1	
								C	TCLK1	I	1	
								D	SPI1_NPCS1	O	1	
								E	I2SC0_DO0	O	1	
								F	ISC_VSYNC	I	3	
L11	J13	VDDIOP1	GPIO	PC6	I/O	–	–	A	LCDHSYNC	O	1	PIO, I, PU, ST

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								E	TF0	I/O	2	
								F	A2	O	2	
G5	–	VDDISC	GPIO	PC14	I/O	–	–	A	LCDDAT6	O	2	PIO, I, PU, ST
								B	GRX0	I	1	
								C	ISC_D5	I	1	
								E	TD0	O	2	
								F	A3	O	2	
G2	–	VDDISC	GPIO	PC15	I/O	–	–	A	LCDDAT7	O	2	PIO, I, PU, ST
								B	GRX1	I	1	
								C	ISC_D6	I	1	
								E	RD0	I	2	
								F	A4	O	2	
G6	–	VDDISC	GPIO	PC16	I/O	–	–	A	LCDDAT10	O	2	PIO, I, PU, ST
								B	GTX0	O	1	
								C	ISC_D7	I	1	
								E	RK0	I/O	2	
								F	A5	O	2	
C1	–	VDDISC	GPIO	PC17	I/O	–	–	A	LCDDAT11	O	2	PIO, I, PU, ST
								B	GTX1	O	1	
								C	ISC_D8	I	1	
								E	RF0	I/O	2	
								F	A6	O	2	
G9	–	VDDISC	GPIO	PC18	I/O	–	–	A	LCDDAT12	O	2	PIO, I, PU, ST
								B	GMDC	O	1	
								C	ISC_D9	I	1	
								E	FLEXCOM3_IO2	I/O	2	
								F	A7	O	2	
D1	–	VDDISC	GPIO	PC19	I/O	–	–	A	LCDDAT13	O	2	PIO, I, PU, ST
								B	GMDIO	I/O	1	
								C	ISC_D10	I	1	
								E	FLEXCOM3_IO1	I/O	2	
								F	A8	O	2	
H4	–	VDDISC	GPIO	PC20	I/O	–	–	A	LCDDAT14	O	2	PIO, I, PU, ST
								B	GRXCK	I	1	
								C	ISC_D11	I	1	
								E	FLEXCOM3_IO0	I/O	2	
								F	A9	O	2	
E1	–	VDDISC	GPIO	PC21	I/O	–	–	A	LCDDAT15	O	2	PIO, I, PU, ST
								B	GTXER	O	1	
								C	ISC_PCK	I	1	
								E	FLEXCOM3_IO3	O	2	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	A10	O	2	
F1	–	VDDISC	GPIO	PC22	I/O	–	–	A	LCDDAT18	O	2	PIO, I, PU, ST
								B	GCRS	I	1	
								C	ISC_VSYNC	I	1	
								E	FLEXCOM3_IO4	O	2	
								F	A11	O	2	
H9	–	VDDISC	GPIO	PC23	I/O	–	–	A	LCDDAT19	O	2	PIO, I, PU, ST
								B	GCOL	I	1	
								C	ISC_HSYNC	I	1	
								F	A12	O	2	
G1	–	VDDISC	GPIO_CLK	PC24	I/O	–	–	A	LCDDAT20	O	2	PIO, I, PU, ST
								B	GRX2	I	1	
								C	ISC_MCK	O	1	
								F	A13	O	2	
H8	–	VDDISC	GPIO	PC25	I/O	–	–	A	LCDDAT21	O	2	PIO, I, PU, ST
								B	GRX3	I	1	
								C	ISC_FIELD	I	1	
								F	A14	O	2	
F7	–	VDDIOP2	GPIO	PC26	I/O	–	–	A	LCDDAT22	O	2	PIO, I, PU, ST
								B	GTX2	O	1	
								D	CANTX1	O	1	
								F	A15	O	2	
B10	–	VDDIOP2	GPIO	PC27	I/O	–	–	A	LCDDAT23	O	2	PIO, I, PU, ST
								B	GTX3	O	1	
								C	PCK1	O	2	
								D	CANRX1	I	1	
								E	TWD0	I/O	2	
								F	A16	O	2	
F6	–	VDDIOP2	GPIO	PC28	I/O	–	–	A	LCDPWM	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO0	I/O	1	
								C	PCK2	O	1	
								E	TWCK0	I/O	2	
								F	A17	O	2	
B9	–	VDDIOP2	GPIO	PC29	I/O	–	–	A	LCDDISP	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO1	I/O	1	
								F	A18	O	2	
E6	–	VDDIOP2	GPIO	PC30	I/O	–	–	A	LCDVSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO2	I/O	1	
								F	A19	O	2	
A11	–	VDDIOP2	GPIO	PC31	I/O	–	–	A	LCDHSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO3	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	URXD3	I	2	
								F	A20	O	2	
E7	–	VDDIOP2	GPIO_CLK	PD0	I/O	–	–	A	LCDPCK	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	1	
								C	UTXD3	O	2	
								D	GTSUCOMP	O	2	
								F	A23	O	2	
C9	–	VDDIOP2	GPIO	PD1	I/O	–	–	A	LCDDEN	O	2	PIO, I, PU, ST
								D	GRXCK	I	2	
								F	A24	O	2	
D8	–	VDDIOP2	GPIO_CLK	PD2	I/O	–	–	A	URXD1	I	1	PIO, I, PU, ST
								D	GTXER	O	2	
								E	ISC_MCK	O	2	
								F	A25	O	2	
J1	–	VDDANA	GPIO_AD	PD3	I/O	–	–	A	UTXD1	O	1	PIO, I, PU, ST
								B	FIQ	I	2	
								D	GCRS	I	2	
								E	ISC_D11	I	2	
								F	NWAIT	I	2	
H7	–	VDDANA	GPIO_AD	PD4	I/O	–	–	A	TWD1	I/O	2	PIO, I, PU, ST
								B	URXD2	I	1	
								D	GCOL	I	2	
								E	ISC_D10	I	2	
								F	NCS0	O	2	
H1	–	VDDANA	GPIO_AD	PD5	I/O	–	–	A	TWCK1	I/O	2	PIO, I, PU, ST
								B	UTXD2	O	1	
								D	GRX2	I	2	
								E	ISC_D9	I	2	
								F	NCS1	O	2	
J2	–	VDDANA	GPIO_AD	PD6	I/O	–	–	A	TCK	I	2	PIO, I, PU, ST
								B	PCK1	O	1	
								D	GRX3	I	2	
								E	ISC_D8	I	2	
								F	NCS2	O	2	
H6	H5	VDDANA	GPIO_AD	PD7	I/O	–	–	A	TDI	I	2	PIO, I, PU, ST
								C	UTMI_RXVAL	O	1	
								D	GTX2	O	2	
								E	ISC_D0	I	2	
								F	NWR1/NBS1	O	2	
K3	J2	VDDANA	GPIO_AD	PD8	I/O	–	–	A	TDO	O	2	PIO, I, PU, ST
								C	UTMI_RXERR	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								D	GTX3	O	2	
								E	ISC_D1	I	2	
								F	NANDRDY	I	2	
J4	G4	VDDANA	GPIO_AD	PD9	I/O	–	–	A	TMS	I	2	PIO, I, PU, ST
								C	UTMI_RXACT	O	1	
								D	GTXCK	I/O	2	
								E	ISC_D2	I	2	
J3	C2	VDDANA	GPIO_AD	PD10	I/O	–	–	A	NTRST	I	2	PIO, I, PU, ST
								C	UTMI_HDIS	O	1	
								D	GTXEN	O	2	
								E	ISC_D3	I	2	
K2	F2	VDDANA	GPIO_AD	PD11	I/O	–	–	A	TIOA1	I/O	3	PIO, I, PU, ST
								B	PCK2	O	2	
								C	UTMI_LS0	O	1	
								D	GRXDV	I	2	
								E	ISC_D4	I	2	
								F	ISC_MCK	O	4	
K9	K4	VDDANA	GPIO_AD	PD12	I/O	–	–	A	TIOB1	I/O	3	PIO, I, PU, ST
								B	FLEXCOM4_IO0	I/O	2	
								C	UTMI_LS1	O	1	
								D	GRXER	I	2	
								E	ISC_D5	I	2	
								F	ISC_D4	I	4	
N1	C1	VDDANA	GPIO_AD	PD13	I/O	–	–	A	TCLK1	I	3	PIO, I, PU, ST
								B	FLEXCOM4_IO1	I/O	2	
								C	UTMI_CDRCPSEL0	I	1	
								D	GRX0	I	2	
								E	ISC_D6	I	2	
								F	ISC_D5	I	4	
K5	H2	VDDANA	GPIO_AD	PD14	I/O	–	–	A	TCK	I	1	A, PU, ST
								B	FLEXCOM4_IO2	I/O	2	
								C	UTMI_CDRCPSEL1	I	1	
								D	GRX1	I	2	
								E	ISC_D7	I	2	
								F	ISC_D6	I	4	
K8	G2	VDDANA	GPIO_AD	PD15	I/O	–	–	A	TDI	I	1	PIO, I, PU, ST
								B	FLEXCOM4_IO3	O	2	
								C	UTMI_CDRCPDIVEN	I	1	
								D	GTX0	O	2	
								E	ISC_PCK	I	2	
								F	ISC_D7	I	4	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
L5	–	VDDANA	GPIO_AD	PD25	I/O	AD6	–	A	SPI1_SPCK	I/O	3	PIO, I, PU, ST
								C	FLEXCOM4_IO4	O	3	
R1	–	VDDANA	GPIO_AD	PD26	I/O	AD7	–	A	SPI1_MOSI	I/O	3	PIO, I, PU, ST
								C	FLEXCOM2_IO0	I/O	2	
L7	–	VDDANA	GPIO_AD	PD27	I/O	AD8	–	A	SPI1_MISO	I/O	3	PIO, I, PU, ST
								B	TCK	I	3	
								C	FLEXCOM2_IO1	I/O	2	
L3	–	VDDANA	GPIO_AD	PD28	I/O	AD9	–	A	SPI1_NPCS0	I/O	3	PIO, I, PU, ST
								B	TDI	I	3	
								C	FLEXCOM2_IO2	I/O	2	
M2	–	VDDANA	GPIO_AD	PD29	I/O	AD10	–	A	SPI1_NPCS1	O	3	PIO, I, PU, ST
								B	TDO	O	3	
								C	FLEXCOM2_IO3	O	2	
								D	TIOA3	I/O	3	
								E	TWD0	I/O	3	
M9	–	VDDANA	GPIO_AD	PD30	I/O	AD11	–	A	SPI1_NPCS2	O	3	PIO, I, PU, ST
								B	TMS	I	3	
								C	FLEXCOM2_IO4	O	2	
								D	TIOB3	I/O	3	
								E	TWCK0	I/O	3	
M8	–	VDDANA	GPIO	PD31	I/O	–	–	A	ADTRG	I	1	PIO, I, PU, ST
								B	NTRST	I	3	
								C	IRQ	I	4	
								D	TCLK3	I	3	
								E	PCK0	O	2	
L9	L1	VDDANA	–	ADVREF	I	–	–	–	–	–	–	–
K4, J5	K3, L2	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
J6, M1	L3, K1	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
J10, F11	K12, F12	VDDIODDR	DDR	DDR_VREF	–	–	–	–	–	–	–	–
L10, L14, J8, H10, G12, E11, E8	F10, E8, E9, E10, G12, H12, J12	VDDIODDR	power	VDDIODDR	I	–	–	–	–	–	–	–
K10, M14, J9, G10, H12, E10, F8	K11, J11, F9, C10, E11, F8, F11, G13, H13	GNDIODDR	ground	GNDIODDR	I	–	–	–	–	–	–	–
H2, U3, P7, L12, E9, D7	G7, H4, D14, E14, L5	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
E12, F12, J11, K11, K6, K7	G11, E12, E13, H3, H7, H8, J3	GNDCORE	ground	GNDCORE	I	–	–	–	–	–	–	–
D4, F3	F4, E4	VDDIOP0	power	VDDIOP0	I	–	–	–	–	–	–	–
E3, F2	E5, F5	GNDIOP0	ground	GNDIOP0	I	–	–	–	–	–	–	–
N12, P12	N9, N10	VDDIOP1	power	VDDIOP1	I	–	–	–	–	–	–	–
M12, P11	M9, M10	GNDIOP1	ground	GNDIOP1	I	–	–	–	–	–	–	–
D9	–	VDDIOP2	power	VDDIOP2	I	–	–	–	–	–	–	–

Table 7-3. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

Table 7-4. 289-ball TFBGA Package Information

Ball Land	0.450 mm ±0.05
Nominal Ball Diameter	0.4 mm
Solder Mask Opening	0.350 mm ±0.05
Solder Mask Definition	SMD
Solder	OSP

7.2 196-ball TFBGA

For mechanical characteristics of the 196-ball TFBGA package, refer to the SAMA5D2 Series Datasheet, ref. no. DS60001476, available via www.microchip.com.

8. Ordering Information

Table 8-1. Ordering Information

Ordering Code	MRL	Package	Carrier Type	Operating Temperature Range
ATSAMA5D225C-D1M-CU	C	BGA196	Tray	-40°C to +85°C
ATSAMA5D225C-D1M-CUR			Tape & Reel	
ATSAMA5D27C-D5M-CU		BGA289	Tray	
ATSAMA5D27C-D5M-CUR			Tape & Reel	
ATSAMA5D27C-D1G-CU			Tray	
ATSAMA5D27C-D1G-CUR			Tape & Reel	
ATSAMA5D28C-D1G-CU			Tray	
ATSAMA5D28C-D1G-CUR			Tape & Reel	

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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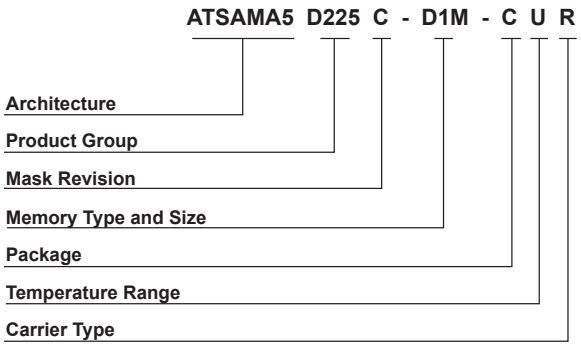

Architecture:	ATSAMA5	= ARM Cortex-A5 CPU
Product Group:	D225	= 196-ball general-purpose microprocessor family
	D27	= 289-ball general-purpose microprocessor family
	D28	
Memory Type and Size:	D1M	= 128-Mbit DDR2 SDRAM
	D5M	= 512-Mbit DDR2 SDRAM
	D1G	= 1-Gigabit DDR2 SDRAM
Mask Revision:	C	
Package:	C	= BGA
Temperature Range:	U	= -40°C to +85°C (Industrial)
Carrier Type:	Blank	= Standard packaging (tray)
	R	= Tape and Reel

Examples:

- ATSAMA5D225C-D1M-CU = ARM Cortex-A5 general-purpose microprocessor, 128-Mbit DDR2 SDRAM, 196-ball, Industrial temperature, BGA Package.

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package

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