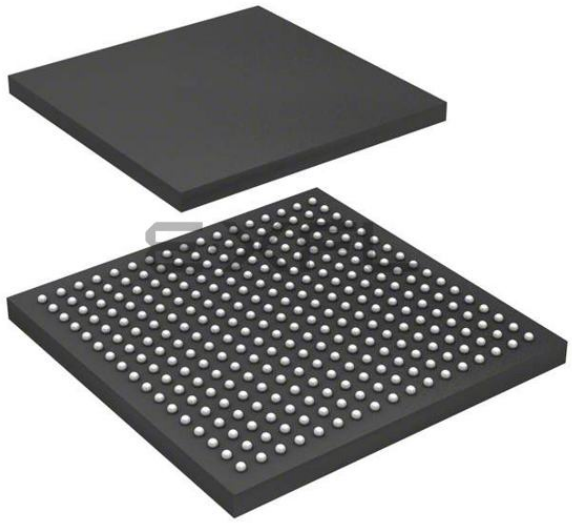

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR1, LPDDR2, LPDDR3, DDR2, DDR3, DDR3L, QSPI
Graphics Acceleration	Yes
Display & Interface Controllers	Keyboard, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + HSIC
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	289-TFBGA
Supplier Device Package	289-TFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsama5d27c-d1g-cu

Table of Contents

  - ITU-R BT. 601/656/1120 Image Sensor Controller (ISC) supporting up to 5 M-pixel sensors with a parallel 12-bit interface for Raw Bayer, YCbCr, Monochrome and JPEG-compressed sensor interface
  - Two Synchronous Serial Controllers (SSC), two Inter-IC Sound Controllers (I2SC), and one Stereo Class D amplifier
  - One Peripheral Touch Controller (PTC) with up to 8 X-lines and 8 Y-lines (64-channel capacitive touch)
  - One Pulse Density Modulation Interface Controller (PDMIC)
  - One USB high-speed device port (UDPHS) and one USB high-speed host port or two USB high-speed host ports (UHPHS)
  - One USB high-speed host port with a High-Speed Inter-Chip (HSIC) interface
  - One 10/100 Ethernet MAC (GMAC)
    - Energy efficiency support (IEEE 802.3az standard)
    - Ethernet AVB support with IEEE802.1AS time stamping
    - IEEE802.1Qav credit-based traffic-shaping hardware support
    - IEEE1588 Precision Time Protocol (PTP)
  - Two high-speed memory card hosts:
    - SDMMC0: SD 3.0, eMMC 4.51, 8 bits
    - SDMMC1: SD 2.0, eMMC 4.41, 4 bits only
  - Two master/slave Serial Peripheral Interfaces (SPI)
  - Two Quad Serial Peripheral Interfaces (QSPI)
  - Five FLEXCOMs (USART, SPI and TWI)
  - Five UARTs
  - Two master CAN-FD (MCAN) controllers with SRAM-based mailboxes, and time- and event-triggered transmission
  - One Rx only UART in backup area (RXLP)
  - One analog comparator (ACC) in backup area
  - Two 2-wire interfaces (TWIHS) up to 400 Kbits/s supporting the I^2C protocol and SMBUS (TWIHS)
  - Two 3-channel 32-bit Timer/Counters (TC), supporting basic PWM modes
  - One full-featured 4-channel 16-bit Pulse Width Modulation (PWM) controller
  - One 12-channel, 12-bit, Analog-to-Digital Converter (ADC) with Resistive TouchScreen capability
- Safety
  - Zero-power Power-On Reset (POR) cells
  - Main crystal clock failure detector
  - Write-protected registers
  - Integrity Check Monitor (ICM) based on SHA256
  - Memory Management Unit
  - Independent watchdog
- Security
  - 5 Kbytes of internal scrambled SRAM:
    - 1 Kbyte non-erasable on tamper detection
    - 4 Kbytes erasable on tamper detection
  - 256 bits of scrambled and erasable registers

  - Up to eight tamper pins for static or dynamic intrusion detections
  - Environmental monitors on specific versions: temperature, voltage, frequency and active die shield(1)
  - Secure Boot Loader(2)
  - On-the-fly AES encryption/decryption on DDR2-SDRAM and QSPI memories (AESB)
  - RTC including time-stamping on security intrusions
  - Programmable fuse box with 544 fuse bits (including JTAG protection and BMS)
- Hardware cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512): compliant with FIPS PUB 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197
  - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
- Up to 128 I/Os
  - Fully programmable through set/clear registers
  - Multiplexing of up to eight peripheral functions per I/O line
  - Each I/O line can be assigned to a peripheral or used as a general purpose I/O
  - PIO controller features a synchronous output providing up to 32 bits of data output in one write operation

Note:

1. For environmental monitors, refer to the document *SAMA5D23 and SAMA5D28 Environmental Monitors* (document no. 44036), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.
2. For secure boot strategies, refer to the document *SAMA5D2 Series Secure Boot Strategy* (document no. 44040), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.

2. DDR2-SDRAM Features

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ±0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-directional, differential data strobes (DQS and DQSN) are transmitted/received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and CLKN)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Auto-refresh and Self-refresh modes
- Precharged Powerdown and Active Powerdown
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								E	FLEXCOM3_IO0	I/O	1	
								F	D10	I/O	2	
M11	H14	VDDIOP1	GPIO_IO	PA16	I/O	–	–	A	SPI0_MISO	I/O	1	PIO, I, PU, ST
								B	TD1	O	1	
								C	QSPI0_IO0	I/O	2	
								D	I2SC1_WS	I/O	2	
								E	FLEXCOM3_IO3	O	1	
								F	D11	I/O	2	
N14	K14	VDDIOP1	GPIO_IO	PA17	I/O	–	–	A	SPI0_NPCS0	I/O	1	PIO, I, PU, ST
								B	RD1	I	1	
								C	QSPI0_IO1	I/O	2	
								D	I2SC1_DI0	I	2	
								E	FLEXCOM3_IO4	O	1	
								F	D12	I/O	2	
T16	L9	VDDIOP1	GPIO_IO	PA18	I/O	–	–	A	SPI0_NPCS1	O	1	PIO, I, PU, ST
								B	RK1	I/O	1	
								C	QSPI0_IO2	I/O	2	
								D	I2SC1_DO0	O	2	
								E	SDMMC1_DAT0	I/O	1	
								F	D13	I/O	2	
T15	P12	VDDIOP1	GPIO_IO	PA19	I/O	–	–	A	SPI0_NPCS2	O	1	PIO, I, PU, ST
								B	RF1	I/O	1	
								C	QSPI0_IO3	I/O	2	
								D	TIOA0	I/O	1	
								E	SDMMC1_DAT1	I/O	1	
								F	D14	I/O	2	
P9	H9	VDDIOP1	GPIO_IO	PA20	I/O	–	–	A	SPI0_NPCS3	O	1	PIO, I, PU, ST
								D	TIOB0	I/O	1	
								E	SDMMC1_DAT2	I/O	1	
								F	D15	I/O	2	
P10	G9	VDDIOP1	GPIO_IO	PA21	I/O	–	–	A	IRQ	I	2	PIO, I, PU, ST
								B	PCK2	O	3	
								D	TCLK0	I	1	
								E	SDMMC1_DAT3	I/O	1	
								F	NANDRDY	I	2	
T17	K10	VDDIOP1	GPIO_QSPI	PA22	I/O	–	–	A	FLEXCOM1_IO2	I/O	1	PIO, I, PU, ST
								B	D0	I/O	1	
								C	TCK	I	4	
								D	SPI1_SPCK	I/O	2	
								E	SDMMC1_CK	I/O	1	
								F	QSPI0_SCK	O	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
T14	G10	VDDIOP1	GPIO	PA23	I/O	–	–	A	FLEXCOM1_IO1	I/O	1	PIO, I, PU, ST
								B	D1	I/O	1	
								C	TDI	I	4	
								D	SPI1_MOSI	I/O	2	
								F	QSPI0_CS	O	3	
R17	P13	VDDIOP1	GPIO_IO	PA24	I/O	–	–	A	FLEXCOM1_IO0	I/O	1	PIO, I, PU, ST
								B	D2	I/O	1	
								C	TDO	O	4	
								D	SPI1_MISO	I/O	2	
								F	QSPI0_IO0	I/O	3	
R16	H10	VDDIOP1	GPIO_IO	PA25	I/O	–	–	A	FLEXCOM1_IO3	O	1	PIO, I, PU, ST
								B	D3	I/O	1	
								C	TMS	I	4	
								D	SPI1_NPCS0	I/O	2	
								F	QSPI0_IO1	I/O	3	
P17	L10	VDDIOP1	GPIO_IO	PA26	I/O	–	–	A	FLEXCOM1_IO4	O	1	PIO, I, PU, ST
								B	D4	I/O	1	
								C	NTRST	I	4	
								D	SPI1_NPCS1	O	2	
								F	QSPI0_IO2	I/O	3	
R15	P14	VDDIOP1	GPIO_IO	PA27	I/O	–	–	A	TIOA1	I/O	2	PIO, I, PU, ST
								B	D5	I/O	1	
								C	SPI0_NPCS2	O	2	
								D	SPI1_NPCS2	O	2	
								E	SDMMC1_RSTN	O	1	
								F	QSPI0_IO3	I/O	3	
R14	N12	VDDIOP1	GPIO	PA28	I/O	–	–	A	TIOB1	I/O	2	PIO, I, PU, ST
								B	D6	I/O	1	
								C	SPI0_NPCS3	O	2	
								D	SPI1_NPCS3	O	2	
								E	SDMMC1_CMD	I/O	1	
								F	CLASSD_L0	O	1	
P14	M12	VDDIOP1	GPIO	PA29	I/O	–	–	A	TCLK1	I	2	PIO, I, PU, ST
								B	D7	I/O	1	
								C	SPI0_NPCS1	O	2	
								E	SDMMC1_WP	I	1	
								F	CLASSD_L1	O	1	
R13	N11	VDDIOP1	GPIO	PA30	I/O	–	–	B	NWE/NANDWE	O	1	PIO, I, PU, ST
								C	SPI0_NPCS0	I/O	2	
								D	PWMH0	O	1	
								E	SDMMC1_CD	I	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	TD1	O	2	
								D	I2SC1_WS	I/O	1	
								E	QSPI1_IO0	I/O	3	
								F	GRXDV	I	3	
C4	A5	VDDIOP0	GPIO_IO	PB17	I/O	–	–	A	LCDDAT6	O	1	PIO, I, PU, ST
								B	A6	O	1	
								C	RD1	I	2	
								D	I2SC1_DI0	I	1	
								E	QSPI1_IO1	I/O	3	
								F	GRXER	I	3	
A5	B4	VDDIOP0	GPIO_IO	PB18	I/O	–	–	A	LCDDAT7	O	1	PIO, I, PU, ST
								B	A7	O	1	
								C	RK1	I/O	2	
								D	I2SC1_DO0	O	1	
								E	QSPI1_IO2	I/O	3	
								F	GRX0	I	3	
B4	A6	VDDIOP0	GPIO_IO	PB19	I/O	–	–	A	LCDDAT8	O	1	PIO, I, PU, ST
								B	A8	O	1	
								C	RF1	I/O	2	
								D	TIOA3	I/O	2	
								E	QSPI1_IO3	I/O	3	
								F	GRX1	I	3	
A4	A4	VDDIOP0	GPIO	PB20	I/O	–	–	A	LCDDAT9	O	1	PIO, I, PU, ST
								B	A9	O	1	
								C	TK0	I/O	1	
								D	TIOB3	I/O	2	
								E	PCK1	O	4	
								F	GTX0	O	3	
D3	A3	VDDIOP0	GPIO	PB21	I/O	–	–	A	LCDDAT10	O	1	PIO, I, PU, ST
								B	A10	O	1	
								C	TF0	I/O	1	
								D	TCLK3	I	2	
								E	FLEXCOM3_IO2	I/O	3	
								F	GTX1	O	3	
C3	D3	VDDIOP0	GPIO	PB22	I/O	–	–	A	LCDDAT11	O	1	PIO, I, PU, ST
								B	A11	O	1	
								C	TD0	O	1	
								D	TIOA2	I/O	2	
								E	FLEXCOM3_IO1	I/O	3	
								F	GMDC	O	3	
B3	B2	VDDIOP0	GPIO	PB23	I/O	–	–	A	LCDDAT12	O	1	PIO, I, PU, ST

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								B	A12	O	1	
								C	RD0	I	1	
								D	TIOB2	I/O	2	
								E	FLEXCOM3_IO0	I/O	3	
								F	GMDIO	I/O	3	
E2	E3	VDDIOP0	GPIO	PB24	I/O	–	–	A	LCDDAT13	O	1	PIO, I, PU, ST
								B	A13	O	1	
								C	RK0	I/O	1	
								D	TCLK2	I	2	
								E	FLEXCOM3_IO3	O	3	
								F	ISC_D10	I	3	
A3	E2	VDDIOP0	GPIO	PB25	I/O	–	–	A	LCDDAT14	O	1	PIO, I, PU, ST
								B	A14	O	1	
								C	RF0	I/O	1	
								E	FLEXCOM3_IO4	O	3	
								F	ISC_D11	I	3	
G3	D4	VDDIOP0	GPIO	PB26	I/O	–	–	A	LCDDAT15	O	1	PIO, I, PU, ST
								B	A15	O	1	
								C	URXD0	I	1	
								D	PDMIC_DAT		1	
								F	ISC_D0	I	3	
F4	C3	VDDIOP0	GPIO	PB27	I/O	–	–	A	LCDDAT16	O	1	PIO, I, PU, ST
								B	A16	O	1	
								C	UTXD0	O	1	
								D	PDMIC_CLK		1	
								F	ISC_D1	I	3	
D2	D2	VDDIOP0	GPIO	PB28	I/O	–	–	A	LCDDAT17	O	1	PIO, I, PU, ST
								B	A17	O	1	
								C	FLEXCOM0_IO0	I/O	1	
								D	TIOA5	I/O	2	
								F	ISC_D2	I	3	
G8	B3	VDDIOP0	GPIO	PB29	I/O	–	–	A	LCDDAT18	O	1	PIO, I, PU, ST
								B	A18	O	1	
								C	FLEXCOM0_IO1	I/O	1	
								D	TIOB5	I/O	2	
								F	ISC_D3	I	3	
C2	F3	VDDIOP0	GPIO	PB30	I/O	–	–	A	LCDDAT19	O	1	PIO, I, PU, ST
								B	A19	O	1	
								C	FLEXCOM0_IO2	I/O	1	
								D	TCLK5	I	2	
								F	ISC_D4	I	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
G7	A2	VDDIOP0	GPIO	PB31	I/O	–	–	A	LCDDAT20	O	1	PIO, I, PU, ST
								B	A20	O	1	
								C	FLEXCOM0_IO3	O	1	
								D	TWD0	I/O	1	
								F	ISC_D5	I	3	
N10	L13	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDDAT21	O	1	PIO, I, PU, ST
								B	A23	O	1	
								C	FLEXCOM0_IO4	O	1	
								D	TWCK0	I/O	1	
								F	ISC_D6	I	3	
N11	H11	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDDAT22	O	1	PIO, I, PU, ST
								B	A24	O	1	
								C	CANTX0	O	1	
								D	SPI1_SPCK	I/O	1	
								E	I2SC0_CK	I/O	1	
								F	ISC_D7	I	3	
N9	L11	VDDIOP1	GPIO	PC2	I/O	–	–	A	LCDDAT23	O	1	PIO, I, PU, ST
								B	A25	O	1	
								C	CANRX0	I	1	
								D	SPI1_MOSI	I/O	1	
								E	I2SC0_MCK	O	1	
								F	ISC_D8	I	3	
M10	F13	VDDIOP1	GPIO	PC3	I/O	–	–	A	LCDPWM	O	1	PIO, I, PU, ST
								B	NWAIT	I	1	
								C	TIOA1	I/O	1	
								D	SPI1_MISO	I/O	1	
								E	I2SC0_WS	I/O	1	
								F	ISC_D9	I	3	
N15	G14	VDDIOP1	GPIO	PC4	I/O	–	–	A	LCDDISP	O	1	PIO, I, PU, ST
								B	NWR1/NBS1	O	1	
								C	TIOB1	I/O	1	
								D	SPI1_NPCS0	I/O	1	
								E	I2SC0_DI0	I	1	
								F	ISC_PCK	I	3	
M16	J14	VDDIOP1	GPIO	PC5	I/O	–	–	A	LCDVSYNC	O	1	PIO, I, PU, ST
								B	NCS0	O	1	
								C	TCLK1	I	1	
								D	SPI1_NPCS1	O	1	
								E	I2SC0_DO0	O	1	
								F	ISC_VSYNC	I	3	
L11	J13	VDDIOP1	GPIO	PC6	I/O	–	–	A	LCDHSYNC	O	1	PIO, I, PU, ST

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								E	TF0	I/O	2	
								F	A2	O	2	
G5	–	VDDISC	GPIO	PC14	I/O	–	–	A	LCDDAT6	O	2	PIO, I, PU, ST
								B	GRX0	I	1	
								C	ISC_D5	I	1	
								E	TD0	O	2	
								F	A3	O	2	
G2	–	VDDISC	GPIO	PC15	I/O	–	–	A	LCDDAT7	O	2	PIO, I, PU, ST
								B	GRX1	I	1	
								C	ISC_D6	I	1	
								E	RD0	I	2	
								F	A4	O	2	
G6	–	VDDISC	GPIO	PC16	I/O	–	–	A	LCDDAT10	O	2	PIO, I, PU, ST
								B	GTX0	O	1	
								C	ISC_D7	I	1	
								E	RK0	I/O	2	
								F	A5	O	2	
C1	–	VDDISC	GPIO	PC17	I/O	–	–	A	LCDDAT11	O	2	PIO, I, PU, ST
								B	GTX1	O	1	
								C	ISC_D8	I	1	
								E	RF0	I/O	2	
								F	A6	O	2	
G9	–	VDDISC	GPIO	PC18	I/O	–	–	A	LCDDAT12	O	2	PIO, I, PU, ST
								B	GMDC	O	1	
								C	ISC_D9	I	1	
								E	FLEXCOM3_IO2	I/O	2	
								F	A7	O	2	
D1	–	VDDISC	GPIO	PC19	I/O	–	–	A	LCDDAT13	O	2	PIO, I, PU, ST
								B	GMDIO	I/O	1	
								C	ISC_D10	I	1	
								E	FLEXCOM3_IO1	I/O	2	
								F	A8	O	2	
H4	–	VDDISC	GPIO	PC20	I/O	–	–	A	LCDDAT14	O	2	PIO, I, PU, ST
								B	GRXCK	I	1	
								C	ISC_D11	I	1	
								E	FLEXCOM3_IO0	I/O	2	
								F	A9	O	2	
E1	–	VDDISC	GPIO	PC21	I/O	–	–	A	LCDDAT15	O	2	PIO, I, PU, ST
								B	GTXER	O	1	
								C	ISC_PCK	I	1	
								E	FLEXCOM3_IO3	O	2	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								F	A10	O	2	
F1	–	VDDISC	GPIO	PC22	I/O	–	–	A	LCDDAT18	O	2	PIO, I, PU, ST
								B	GCRS	I	1	
								C	ISC_VSYNC	I	1	
								E	FLEXCOM3_IO4	O	2	
								F	A11	O	2	
H9	–	VDDISC	GPIO	PC23	I/O	–	–	A	LCDDAT19	O	2	PIO, I, PU, ST
								B	GCOL	I	1	
								C	ISC_HSYNC	I	1	
								F	A12	O	2	
G1	–	VDDISC	GPIO_CLK	PC24	I/O	–	–	A	LCDDAT20	O	2	PIO, I, PU, ST
								B	GRX2	I	1	
								C	ISC_MCK	O	1	
								F	A13	O	2	
H8	–	VDDISC	GPIO	PC25	I/O	–	–	A	LCDDAT21	O	2	PIO, I, PU, ST
								B	GRX3	I	1	
								C	ISC_FIELD	I	1	
								F	A14	O	2	
F7	–	VDDIOP2	GPIO	PC26	I/O	–	–	A	LCDDAT22	O	2	PIO, I, PU, ST
								B	GTX2	O	1	
								D	CANTX1	O	1	
								F	A15	O	2	
B10	–	VDDIOP2	GPIO	PC27	I/O	–	–	A	LCDDAT23	O	2	PIO, I, PU, ST
								B	GTX3	O	1	
								C	PCK1	O	2	
								D	CANRX1	I	1	
								E	TWD0	I/O	2	
								F	A16	O	2	
F6	–	VDDIOP2	GPIO	PC28	I/O	–	–	A	LCDPWM	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO0	I/O	1	
								C	PCK2	O	1	
								E	TWCK0	I/O	2	
								F	A17	O	2	
B9	–	VDDIOP2	GPIO	PC29	I/O	–	–	A	LCDDISP	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO1	I/O	1	
								F	A18	O	2	
E6	–	VDDIOP2	GPIO	PC30	I/O	–	–	A	LCDVSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO2	I/O	1	
								F	A19	O	2	
A11	–	VDDIOP2	GPIO	PC31	I/O	–	–	A	LCDHSYNC	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO3	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
								C	URXD3	I	2	
								F	A20	O	2	
E7	–	VDDIOP2	GPIO_CLK	PD0	I/O	–	–	A	LCDPCK	O	2	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	1	
								C	UTXD3	O	2	
								D	GTSUCOMP	O	2	
								F	A23	O	2	
C9	–	VDDIOP2	GPIO	PD1	I/O	–	–	A	LCDDEN	O	2	PIO, I, PU, ST
								D	GRXCK	I	2	
								F	A24	O	2	
D8	–	VDDIOP2	GPIO_CLK	PD2	I/O	–	–	A	URXD1	I	1	PIO, I, PU, ST
								D	GTXER	O	2	
								E	ISC_MCK	O	2	
								F	A25	O	2	
J1	–	VDDANA	GPIO_AD	PD3	I/O	–	–	A	UTXD1	O	1	PIO, I, PU, ST
								B	FIQ	I	2	
								D	GCRS	I	2	
								E	ISC_D11	I	2	
								F	NWAIT	I	2	
H7	–	VDDANA	GPIO_AD	PD4	I/O	–	–	A	TWD1	I/O	2	PIO, I, PU, ST
								B	URXD2	I	1	
								D	GCOL	I	2	
								E	ISC_D10	I	2	
								F	NCS0	O	2	
H1	–	VDDANA	GPIO_AD	PD5	I/O	–	–	A	TWCK1	I/O	2	PIO, I, PU, ST
								B	UTXD2	O	1	
								D	GRX2	I	2	
								E	ISC_D9	I	2	
								F	NCS1	O	2	
J2	–	VDDANA	GPIO_AD	PD6	I/O	–	–	A	TCK	I	2	PIO, I, PU, ST
								B	PCK1	O	1	
								D	GRX3	I	2	
								E	ISC_D8	I	2	
								F	NCS2	O	2	
H6	H5	VDDANA	GPIO_AD	PD7	I/O	–	–	A	TDI	I	2	PIO, I, PU, ST
								C	UTMI_RXVAL	O	1	
								D	GTX2	O	2	
								E	ISC_D0	I	2	
								F	NWR1/NBS1	O	2	
K3	J2	VDDANA	GPIO_AD	PD8	I/O	–	–	A	TDO	O	2	PIO, I, PU, ST
								C	UTMI_RXERR	O	1	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
L1	J1	VDDANA	GPIO_AD	PD16	I/O	–	–	A	TDO	O	1	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	2	
								C	UTMI_CDRBISTEN	I	1	
								D	GTX1	O	2	
								E	ISC_VSYNC	I	2	
								F	ISC_D8	I	4	
K1	A1	VDDANA	GPIO_AD	PD17	I/O	–	–	A	TMS	I	1	A, PU, ST
								C	UTMI_CDRCPSELDIV	O	1	
								D	GMDC	O	2	
								E	ISC_HSYNC	I	2	
								F	ISC_D9	I	4	
J7	G3	VDDANA	GPIO_AD	PD18	I/O	–	–	A	NTRST	I	1	PIO, I, PU, ST
								D	GMDIO	I/O	2	
								E	ISC_FIELD	I	2	
								F	ISC_D10	I	4	
L8	K2	VDDANA	GPIO_AD	PD19	I/O	AD0	–	A	PCK0	O	1	PIO, I, PU, ST
								B	TWD1	I/O	3	
								C	URXD2	I	3	
								E	I2SC0_CK	I/O	2	
								F	ISC_D11	I	4	
L2	H1	VDDANA	GPIO_AD	PD20	I/O	AD1	–	A	TIOA2	I/O	3	PIO, I, PU, ST
								B	TWCK1	I/O	3	
								C	UTXD2	O	3	
								E	I2SC0_MCK	O	2	
								F	ISC_PCK	I	4	
P1	G1	VDDANA	GPIO_AD	PD21	I/O	AD2	–	A	TIOB2	I/O	3	PIO, I, PU, ST
								B	TWD0	I/O	4	
								C	FLEXCOM4_IO0	I/O	3	
								E	I2SC0_WS	I/O	2	
								F	ISC_VSYNC	I	4	
L6	F1	VDDANA	GPIO_AD	PD22	I/O	AD3	–	A	TCLK2	I	3	PIO, I, PU, ST
								B	TWCK0	I/O	4	
								C	FLEXCOM4_IO1	I/O	3	
								E	I2SC0_DI0	I	2	
								F	ISC_HSYNC	I	4	
T1	E1	VDDANA	GPIO_AD	PD23	I/O	AD4	–	A	URXD2	I	2	PIO, I, PU, ST
								C	FLEXCOM4_IO2	I/O	3	
								E	I2SC0_DO0	O	2	
								F	ISC_FIELD	I	4	
L4	–	VDDANA	GPIO_AD	PD24	I/O	AD5	–	A	UTXD2	O	2	PIO, I, PU, ST
								C	FLEXCOM4_IO3	O	3	

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
L5	–	VDDANA	GPIO_AD	PD25	I/O	AD6	–	A	SPI1_SPCK	I/O	3	PIO, I, PU, ST
								C	FLEXCOM4_IO4	O	3	
R1	–	VDDANA	GPIO_AD	PD26	I/O	AD7	–	A	SPI1_MOSI	I/O	3	PIO, I, PU, ST
								C	FLEXCOM2_IO0	I/O	2	
L7	–	VDDANA	GPIO_AD	PD27	I/O	AD8	–	A	SPI1_MISO	I/O	3	PIO, I, PU, ST
								B	TCK	I	3	
								C	FLEXCOM2_IO1	I/O	2	
L3	–	VDDANA	GPIO_AD	PD28	I/O	AD9	–	A	SPI1_NPCS0	I/O	3	PIO, I, PU, ST
								B	TDI	I	3	
								C	FLEXCOM2_IO2	I/O	2	
M2	–	VDDANA	GPIO_AD	PD29	I/O	AD10	–	A	SPI1_NPCS1	O	3	PIO, I, PU, ST
								B	TDO	O	3	
								C	FLEXCOM2_IO3	O	2	
								D	TIOA3	I/O	3	
								E	TWD0	I/O	3	
M9	–	VDDANA	GPIO_AD	PD30	I/O	AD11	–	A	SPI1_NPCS2	O	3	PIO, I, PU, ST
								B	TMS	I	3	
								C	FLEXCOM2_IO4	O	2	
								D	TIOB3	I/O	3	
								E	TWCK0	I/O	3	
M8	–	VDDANA	GPIO	PD31	I/O	–	–	A	ADTRG	I	1	PIO, I, PU, ST
								B	NTRST	I	3	
								C	IRQ	I	4	
								D	TCLK3	I	3	
								E	PCK0	O	2	
L9	L1	VDDANA	–	ADVREF	I	–	–	–	–	–	–	–
K4, J5	K3, L2	VDDANA	power	VDDANA	I	–	–	–	–	–	–	–
J6, M1	L3, K1	GNDANA	ground	GNDANA	I	–	–	–	–	–	–	–
J10, F11	K12, F12	VDDIODDR	DDR	DDR_VREF	–	–	–	–	–	–	–	–
L10, L14, J8, H10, G12, E11, E8	F10, E8, E9, E10, G12, H12, J12	VDDIODDR	power	VDDIODDR	I	–	–	–	–	–	–	–
K10, M14, J9, G10, H12, E10, F8	K11, J11, F9, C10, E11, F8, F11, G13, H13	GNDIODDR	ground	GNDIODDR	I	–	–	–	–	–	–	–
H2, U3, P7, L12, E9, D7	G7, H4, D14, E14, L5	VDDCORE	power	VDDCORE	I	–	–	–	–	–	–	–
E12, F12, J11, K11, K6, K7	G11, E12, E13, H3, H7, H8, J3	GNDCORE	ground	GNDCORE	I	–	–	–	–	–	–	–
D4, F3	F4, E4	VDDIOP0	power	VDDIOP0	I	–	–	–	–	–	–	–
E3, F2	E5, F5	GNDIOP0	ground	GNDIOP0	I	–	–	–	–	–	–	–
N12, P12	N9, N10	VDDIOP1	power	VDDIOP1	I	–	–	–	–	–	–	–
M12, P11	M9, M10	GNDIOP1	ground	GNDIOP1	I	–	–	–	–	–	–	–
D9	–	VDDIOP2	power	VDDIOP2	I	–	–	–	–	–	–	–

289-ball BGA	196-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State (Signal, Dir, PU, PD, HiZ, ST)[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	IO Set	
N3	–	VDDBU	–	PIOBU7	–	–	–	–	–	–	–	–
U5	K5	VDDBU	power	VDDBU	I	–	–	–	–	–	–	–
U4	N2	GNDBU	ground	GNDBU	I	–	–	–	–	–	–	–
U2	M1	VDDBU	–	XIN32	–	–	–	–	–	–	–	–
U1	M2	VDDBU	–	XOUT32	–	–	–	–	–	–	–	–
U6	P2	VDDBU	–	COMPP	I	–	–	–	–	–	–	–
U7	P3	VDDBU	–	COMPN	I	–	–	–	–	–	–	–
D17	D12	DDRM_VDDQ[2]	–	ODT	I	–	–	–	–	–	–	–
A16, B16, C16, D16, E15, G17, J17, L16	B10, A12, D10, D11	DDRM_VDD	power	DDRM_VDD	I	–	–	–	–	–	–	–
E16	E7	DDRM_VDDL[2]	power	DDRM_VDDL[2]	I	–	–	–	–	–	–	–
F15, G15, H15, J15, K15, L15	A7, A13, A9, A11, B6, C12	DDRM_VDDQ[2]	power	DDRM_VDDQ[2]	–	–	–	–	–	–	–	–
A17, B17, C17, D15, E14, F17, H17, L17	B14, A8, C11, C14, D8	DDRM_VSS	ground	DDRM_VSS	–	–	–	–	–	–	–	–
E17	D13	DDRM_VSSDL	ground	DDRM_VSSDL	I	–	–	–	–	–	–	–
F16, G16, H16, J16, K16, K17	A10, A14, B11, B12, B13, C13	DDRM_VSSQ	ground	DDRM_VSSQ	I	–	–	–	–	–	–	–
A12, A13, A14, A15, B11, B12, B13, B14, B15, C10, C11, C12, C13, C14, C15, D10, D11, D12, D13, D14, E13, F9, F10, F13, F14, G11, G13, G14, H11, H13, H14, J12, J13, J14, K12, K13, K14, L13, R12, T9	–	–	NC	–	–	–	–	–	–	–	–	–

Note:

1. Signal = ‘PIO’ if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Refer to the DDR2-SDRAM datasheet for DDRM_VDDQ and DDRM_VDDL definitions. DDRM_VDDQ/DDRM_VDDL = 1.8V ±0.1V.

6. DDR2-SDRAM Memory

The SAMA5D2 SIP is available with 128 Mbit, 512 Mbit or 1 Gbit DDR2-SDRAM memory options. For the features of these memories, see DDR2-SDRAM Features.

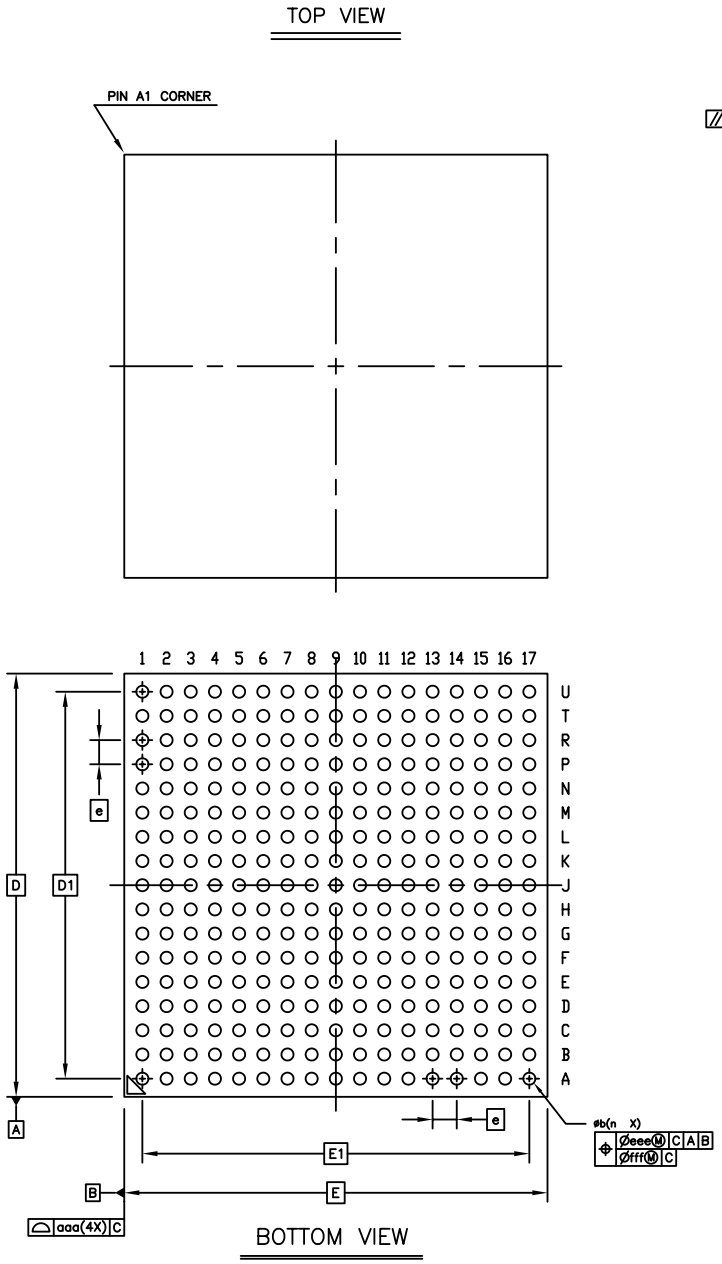
For power consumption, electrical characteristics and timings of these memories, refer to the datasheets referenced below on the manufacturer's website www.winbond.com.

Table 6-1. Memory Datasheet References

Density	Winbond Packaged PN	Datasheet Reference Number
128 Mbit	W9712G6KB25I	W9712G6KB
512 Mbit	W9751G6KB25I	W9751G6KB
1 Gbit	W971GG6SB25I	W971GG6SB

7. Mechanical Characteristics

7.1 289-ball TFBGA



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			SBS TFBGA		
Body Size:	X	E		14.000	
	Y	D		14.000	
Ball Pitch :		e		0.800	
Total Thickness :		A			1.200
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.260 Ref.	
Ball Diameter :				0.400	
Stand Off :		A1	0.270	–	0.370
Ball Width :		b	0.380	–	0.480
Package Edge Tolerance :		aaa		0.150	
Mold Parallelism :		ccc		0.200	
Coplanarity:		ddd		0.120	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		289	
Edge Ball Center to Center :	X	E1		12.800	
	Y	D1		12.800	

Table 7-1. 289-ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 7-2. Device and 289-ball TFBGA Package Weight

445	mg

Table 7-3. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

Table 7-4. 289-ball TFBGA Package Information

Ball Land	0.450 mm ±0.05
Nominal Ball Diameter	0.4 mm
Solder Mask Opening	0.350 mm ±0.05
Solder Mask Definition	SMD
Solder	OSP

7.2 196-ball TFBGA

For mechanical characteristics of the 196-ball TFBGA package, refer to the SAMA5D2 Series Datasheet, ref. no. DS60001476, available via www.microchip.com.

8. Ordering Information

Table 8-1. Ordering Information

Ordering Code	MRL	Package	Carrier Type	Operating Temperature Range
ATSAMA5D225C-D1M-CU	C	BGA196	Tray	-40°C to +85°C
ATSAMA5D225C-D1M-CUR			Tape & Reel	
ATSAMA5D27C-D5M-CU		BGA289	Tray	
ATSAMA5D27C-D5M-CUR			Tape & Reel	
ATSAMA5D27C-D1G-CU			Tray	
ATSAMA5D27C-D1G-CUR			Tape & Reel	
ATSAMA5D28C-D1G-CU			Tray	
ATSAMA5D28C-D1G-CUR			Tape & Reel	

9. Revision History

Table 9-1. SAMA5D2 SIP Datasheet, DS60001484A, September-2017 Revision History

Changes
First issue.