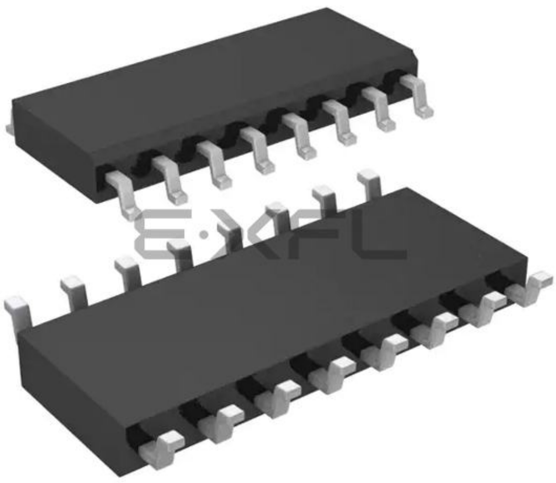

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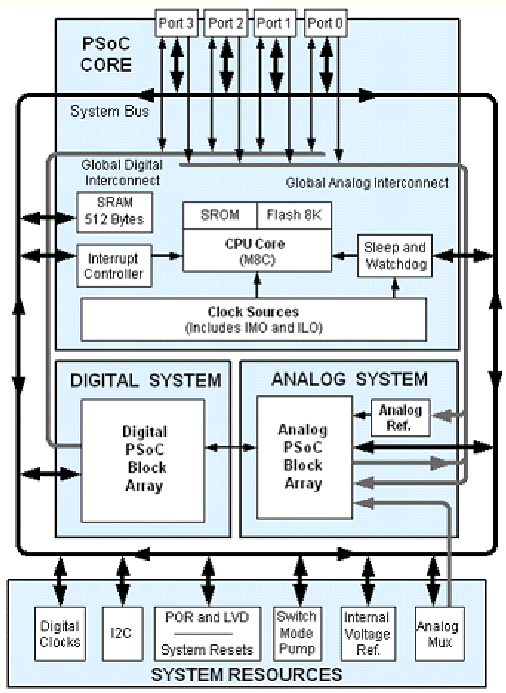
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 28x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21234b-24sxi

Logic Block Diagram



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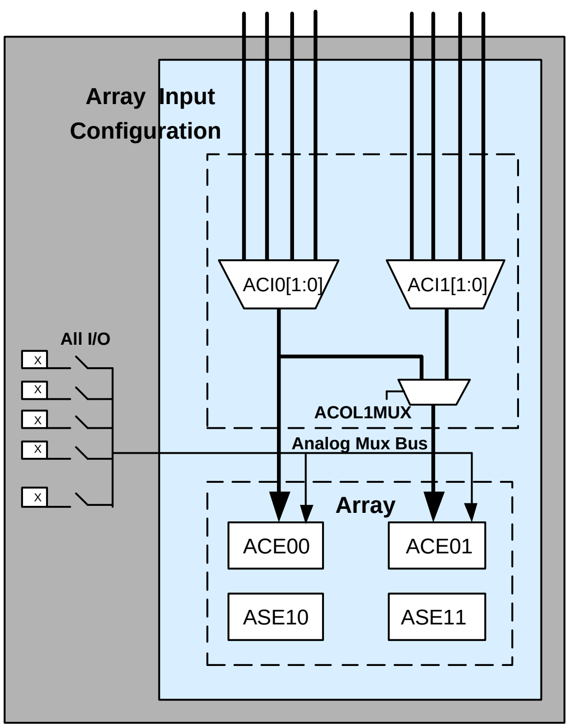
The Analog System

The analog system consists of four configurable blocks that allow for the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to two) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The CY8C21x34B devices provide limited functionality Type E analog blocks. Each column contains one CT Type E block and one SC Type E block. Refer to the *PSoC Technical Reference Manual* for detailed information on the CY8C21x34B's Type E analog blocks.

Figure 3. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins may be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that allows analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch-mode pump, low-voltage detection, and power-on-reset (POR).

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.
- Versatile analog multiplexer system.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SmartSense Enabled
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2K	32K	–
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1K	16K	–
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16K	–
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1K	16K	–
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4K	–
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8K	–
CY8C22x45	up to 38	2	8	up to 38	0	4	6[3]	1 K	16K	–
CY8C21x45	up to 24	1	4	up to 24	0	4	6[3]	512	8K	–
CY8C21x34	up to 28	1	4	up to 28	0	2	4[3]	512	8K	–
CY8C21x34B	up to 28	1	4	up to 28	0	2	4[3]	512	8K	Y
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4K	–
CY8C20x34	up to 28	0	0	up to 28	0	0	3[3,4]	512	8K	–
CY8C20xx6A	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2K	up to 32K	Y

Notes
3. Limited analog functionality.
4. Two analog blocks and one CapSense®.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

SmartSense

A key differentiation between the current offering of CY8C21x34 and CY8C21x34B, is the addition of the SmartSense user module in the 'B' version.

SmartSense is an innovative solution from Cypress that eliminates the manual tuning process from CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

Pin Information

The CY8C21x34B PSoC device is available in a variety of packages which are listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 4. CY8C21234B 16-pin PSoC Device

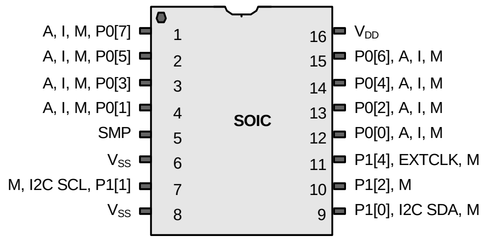


Table 2. Pin Definitions – CY8C21234B 16-pin (SOIC)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		SMP	Switch-mode pump (SMP) connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O	M	P1[1]	I^2C serial clock (SCL), ISSP-SCLK[5]
8	Power		V_{SS}	Ground connection
9	I/O	M	P1[0]	I^2C serial data (SDA), ISSP-SDATA[5]
10	I/O	M	P1[2]	
11	I/O	M	P1[4]	Optional external clock input (EXTCLK)
12	I/O	I, M	P0[0]	Analog column mux input
13	I/O	I, M	P0[2]	Analog column mux input
14	I/O	I, M	P0[4]	Analog column mux input
15	I/O	I, M	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note

5. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

Table 5. Pin Definitions - CY8C21434B/CY8C21634B 32-pin (QFN)[8]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[1]	Analog column mux input, integrating input
2	I/O	M	P2[7]	
3	I/O	M	P2[5]	
4	I/O	M	P2[3]	
5	I/O	M	P2[1]	
6	I/O	M	P3[3]	In CY8C21434B part
6	Power		SMP	SMP connection to required external components in CY8C21634B part
7	I/O	M	P3[1]	In CY8C21434B part
7	Power		V_{SS}	Ground connection in CY8C21634B part
8	I/O	M	P1[7]	I^2C SCL
9	I/O	M	P1[5]	I^2C SDA
10	I/O	M	P1[3]	
11	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK[9]
12	Power		V_{SS}	Ground connection
13	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA[9]
14	I/O	M	P1[2]	
15	I/O	M	P1[4]	Optional external clock input (EXTCLK)
16	I/O	M	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	M	P3[0]	
19	I/O	M	P3[2]	
20	I/O	M	P2[0]	
21	I/O	M	P2[2]	
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage
29	I/O	I, M	P0[7]	Analog column mux input
30	I/O	I, M	P0[5]	Analog column mux input
31	I/O	I, M	P0[3]	Analog column mux input, integrating input
32	Power		V_{SS}	Ground connection

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Notes

8. The center pad on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
9. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

56-pin Part Pinout

The 56-Pin SSOP part is for the CY8C21001 on-chip debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Figure 11. CY8C21001 56-pin PSoC Device

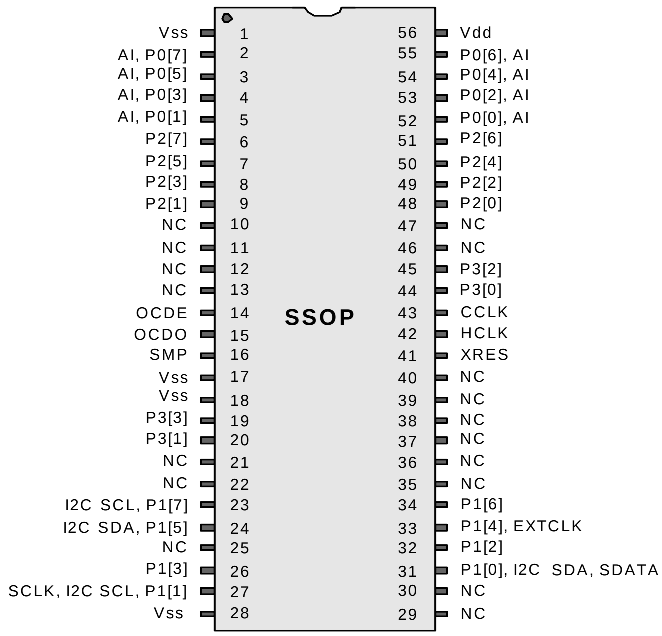


Table 6. Pin Definitions – CY8C21001 56-pin (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection
11			NC	No connection
12			NC	No connection
13			NC	No connection
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	Power		V_{SS}	Ground connection
18	Power		V_{SS}	Ground connection

Register Reference

This chapter lists the registers of the CY8C21x34B PSoC device. For detailed register information, see the *PSoC Technical Reference Manual*.

Register Conventions

The register conventions specific to this section are listed in Table 7.

Table 7. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 9. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed. # Access is bit specific.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. 5 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins 7-to-1)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 16. 3.3 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 17. 2.7 V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

DC Switch Mode Pump Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Figure 14. Basic Switch Mode Pump Circuit

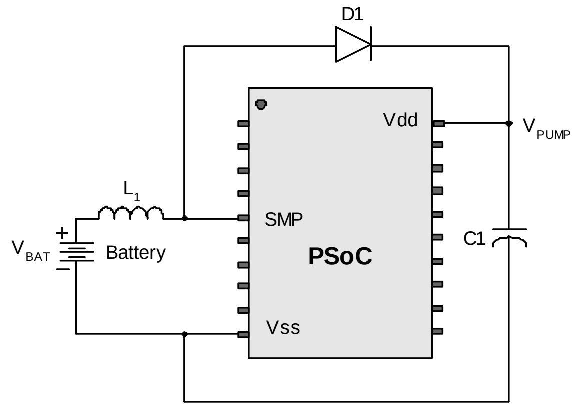


Table 18. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5 V output voltage from pump	4.75	5.0	5.25	V	Configured as in Note 11 Average, neglecting ripple SMP trip voltage is set to 5.0 V
V_{PUMP3V}	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configured as in Note 11 Average, neglecting ripple. SMP trip voltage is set to 3.25 V
V_{PUMP2V}	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configured as in Note 11 Average, neglecting ripple. SMP trip voltage is set to 2.55 V
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configured as in Note 11 SMP trip voltage is set to 5.0 V SMP trip voltage is set to 3.25 V SMP trip voltage is set to 2.55 V
V_{BAT5V}	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 11 SMP trip voltage is set to 5.0 V
V_{BAT3V}	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 11 SMP trip voltage is set to 3.25 V
V_{BAT2V}	Input voltage range from battery	1.0	–	2.8	V	Configured as in Note 11 SMP trip voltage is set to 2.55 V
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configured as in Note 11 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C
ΔV_{PUMP_Line}	Line regulation (over Vi range)	–	5	–	$\%V_O$	Configured as in Note 11 V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 25
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configured as in Note 11 V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 25
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configured as in Note 11 Load is 5 mA

Note

11. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 14.

Table 18. DC Switch Mode Pump (SMP) Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
E_3	Efficiency	35	50	–	%	Configured as in Note 11 Load is 5 mA. SMP trip voltage is set to 3.25 V
E_2	Efficiency	35	80	–	%	For I load = 1mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 µH inductor, 1 µF capacitor, and Schottky diode
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

DC Analog Mux Bus Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, the reset from the XRES pin, or reset from watchdog
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for pump trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5 V and 3.3 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[26]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[26]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[26]	–	–	ns	
	Disable mode	50[26]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[26]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note

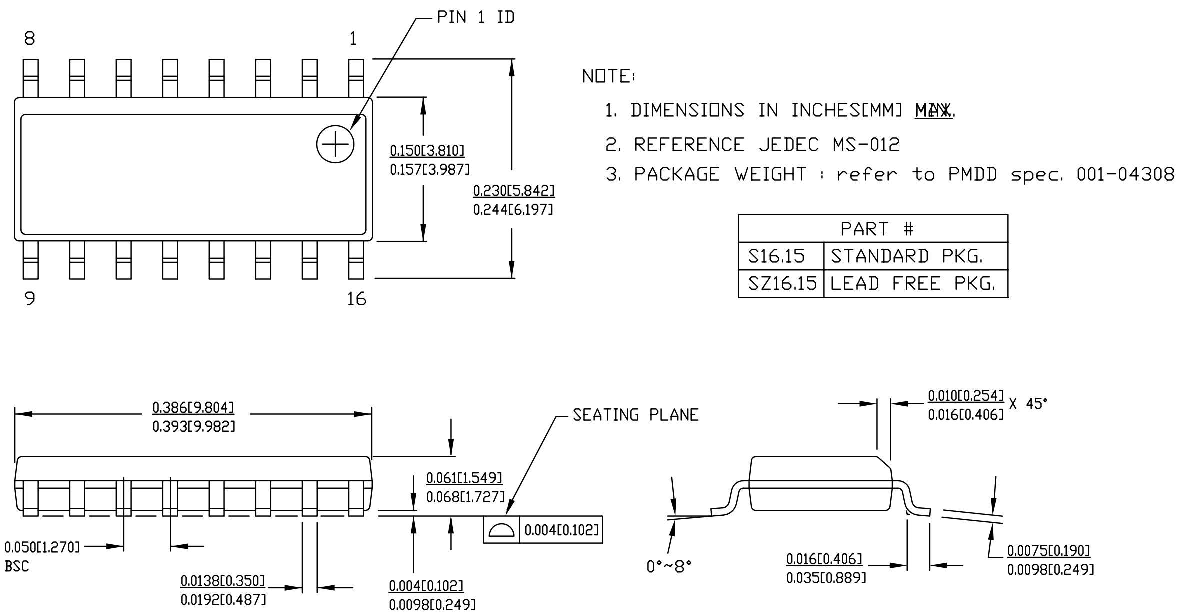
26. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Packaging Information

This section shows the packaging specifications for the CY8C21x34B PSoC device with the thermal impedances for each package.

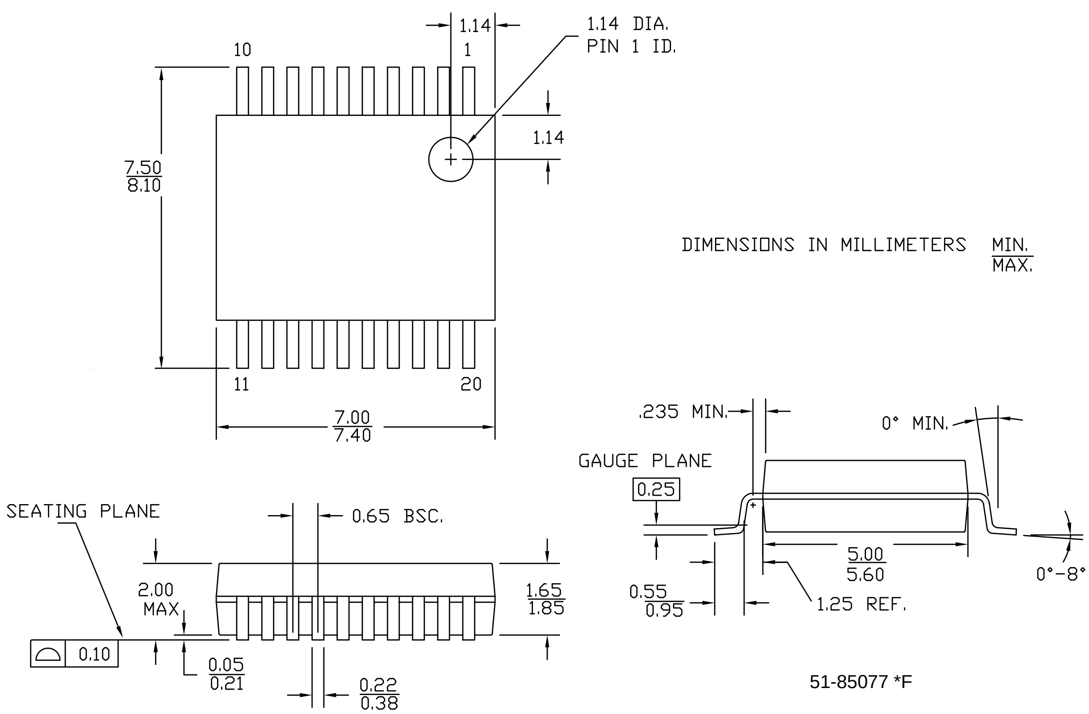
Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 17. 16-pin SOIC (150 Mils) Package Outline, 51-85068



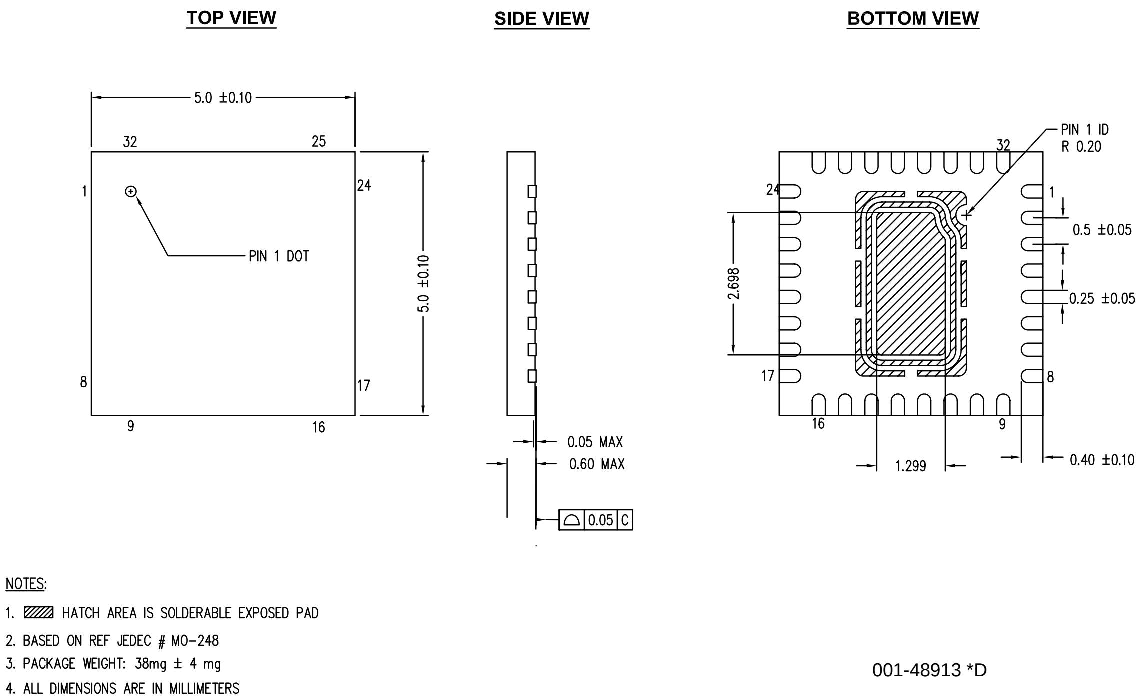
51-85068 *E

Figure 18. 20-pin SSOP (210 Mils) Package Outline, 51-85077



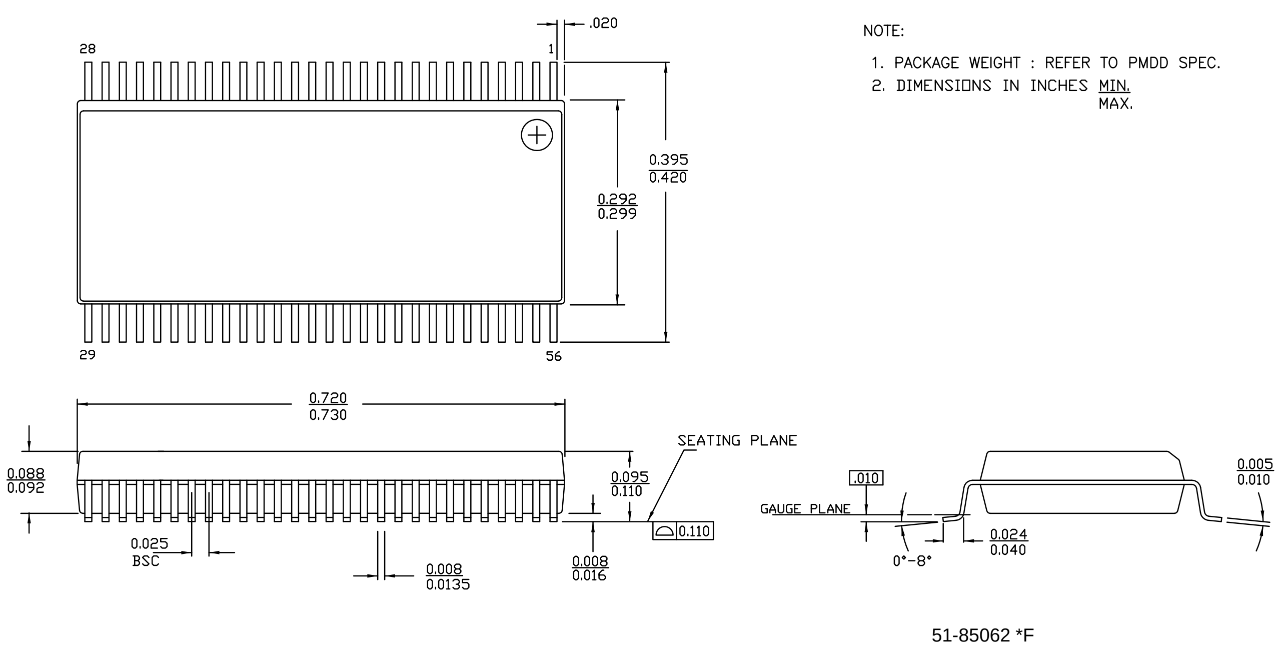
51-85077 *F

Figure 21. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Figure 22. 56-pin SSOP (300 Mils) Package Outline, 51-85062



Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA} [30]	Typical θ_{JC}
16-pin SOIC	123 °C/W	55 °C/W
20-pin SSOP	117 °C/W	41 °C/W
28-pin SSOP	96 °C/W	39 °C/W
32-pin QFN[31] 5 × 5 mm 0.60 Max	27 °C/W	15 °C/W
32-pin QFN[31] 5 × 5 mm 0.93 Max	22 °C/W	12 °C/W
56-pin SSOP	48 °C/W	24 °C/W

Solder Reflow Peak Temperature

Table 37 lists the maximum solder reflow peak temperatures to achieve good solderability. Thermal ramp rate during preheat should be 3 °C/s or lower.

Table 37. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Temperature
16-pin SOIC	260 °C	30 s
20-pin SSOP	260 °C	30 s
28-pin SSOP	260 °C	30 s
32-pin QFN	260 °C	30 s
56-pin SSOP	260 °C	30 s

Notes

30. $T_J = T_A + \text{Power} \times \theta_{JA}$
31. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.
32. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[33]	Foot Kit[34]	Adapter
CY8C21234B-24SXI	16-Pin SOIC	CY3250-21X34	CY3250-16SOIC-FK	Adapters can be found at http://www.emulation.com.
CY8C21334B-24PVXI	20-Pin SSOP	CY3250-21X34	CY3250-20SSOP-FK	
CY8C21534B-24PVXI	28-Pin SSOP	CY3250-21X34	CY3250-28SSOP-FK	

Notes

33. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
34. Foot kit includes surface mount feet that can be soldered to the target PCB.

Acronyms

Table 39 lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch-mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34B, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 (001-72845) available at http://www.cypress.com.

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