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What is "[Embedded - Microcontrollers](#)"?

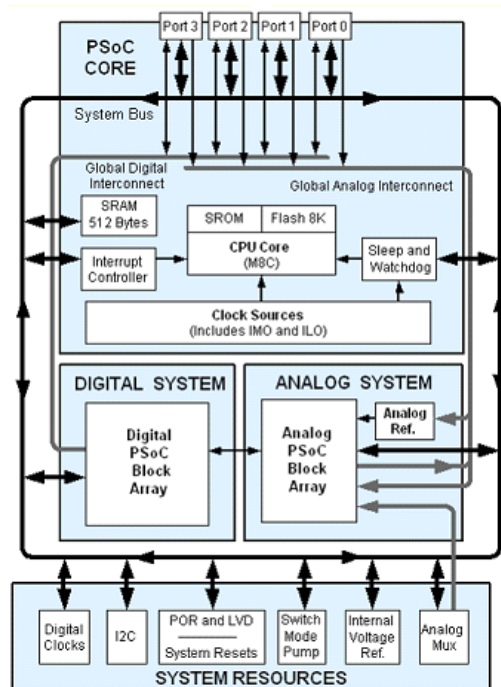
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 28x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-XFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21434b-24lqxi

Logic Block Diagram



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Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality [in-circuit emulator \(ICE\)](#) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

SmartSense

A key differentiation between the current offering of CY8C21x34 and CY8C21x34B, is the addition of the SmartSense user module in the ‘B’ version.

SmartSense is an innovative solution from Cypress that eliminates the manual tuning process from CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

Pin Information

The CY8C21x34B PSoC device is available in a variety of packages which are listed in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O and connection to the common analog bus. However, V_{SS} , V_{DD} , SMP, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 4. CY8C21234B 16-pin PSoC Device

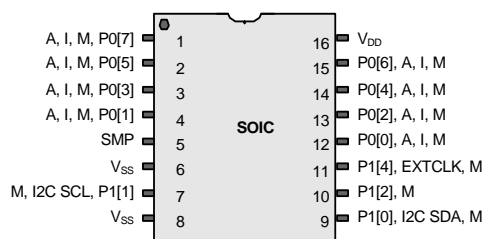


Table 2. Pin Definitions – CY8C21234B 16-pin (SOIC)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		SMP	Switch-mode pump (SMP) connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O	M	P1[1]	I ² C serial clock (SCL), ISSP-SCLK ^[5]
8	Power		V_{SS}	Ground connection
9	I/O	M	P1[0]	I ² C serial data (SDA), ISSP-SDATA ^[5]
10	I/O	M	P1[2]	
11	I/O	M	P1[4]	Optional external clock input (EXTCLK)
12	I/O	I, M	P0[0]	Analog column mux input
13	I/O	I, M	P0[2]	Analog column mux input
14	I/O	I, M	P0[4]	Analog column mux input
15	I/O	I, M	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note

5. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

20-pin Part Pinout

Figure 5. CY8C21334B 20-pin PSoC Device

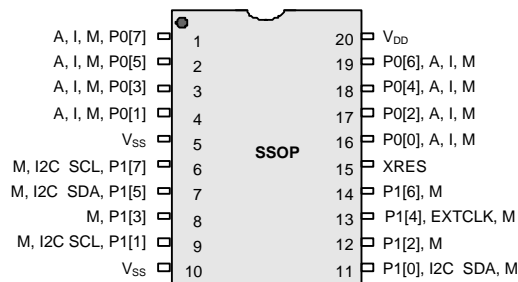


Table 3. Pin Definitions – CY8C21334B 20-pin (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		V _{SS}	Ground connection
6	I/O	M	P1[7]	I ² C SCL
7	I/O	M	P1[5]	I ² C SDA
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	I ² C SCL, ISSP-SCLK ^[6]
10	Power		V _{SS}	Ground connection.
11	I/O	M	P1[0]	I ² C SDA, ISSP-SDATA ^[6]
12	I/O	M	P1[2]	
13	I/O	M	P1[4]	Optional external clock input (EXTCLK)
14	I/O	M	P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I, M	P0[0]	Analog column mux input
17	I/O	I, M	P0[2]	Analog column mux input
18	I/O	I, M	P0[4]	Analog column mux input
19	I/O	I, M	P0[6]	Analog column mux input
20	Power		V _{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note

6. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.

Table 8. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed.

Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x34B PSoC device. For up-to-date electrical specifications, visit the Cypress web site at <http://www.cypress.com>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$ as specified, except where noted.

Refer to [Table 23 on page 27](#) for the electrical specifications for the IMO using SLIMO mode.

Figure 12. Voltage versus CPU Frequency

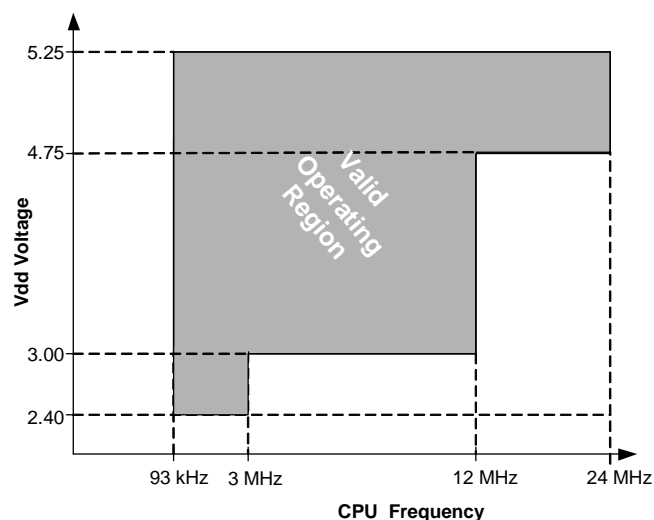
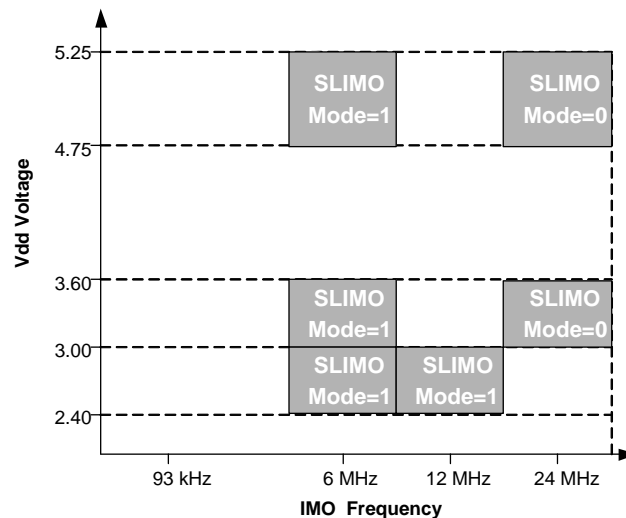


Figure 13. IMO Frequency Trim Options



Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	-55	25	+100	$^{\circ}\text{C}$	Higher storage temperatures reduce data retention time. Recommended storage temperature is $+25\text{ }^{\circ}\text{C} \pm 25\text{ }^{\circ}\text{C}$. Extended duration storage temperatures above $65\text{ }^{\circ}\text{C}$ degrade reliability.
$T_{BAKETEMP}$	Bake temperature	—	125	See package label	$^{\circ}\text{C}$	
$t_{BAKETIME}$	Bake time	See package label	—	72	Hours	
T_A	Ambient temperature with power applied	-40	—	+85	$^{\circ}\text{C}$	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	-0.5	—	+6.0	V	
V_{IO}	DC input voltage	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V	
V_{IOZ}	DC voltage applied to tri-state	$V_{SS} - 0.5$	—	$V_{DD} + 0.5$	V	
I_{MIO}	Maximum current into any port pin	-25	—	+50	mA	
ESD	Electrostatic discharge voltage	2000	—	—	V	Human body model ESD.
LU	Latch-up current	—	—	200	mA	

DC General-Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 13. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
R _{PD}	Pull-down resistor	4	5.6	8	kΩ	
V _{OH}	High output level	V _{DD} – 1.0	–	–	V	I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
V _{OL}	Low output level	–	–	0.75	V	I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I _{OH}	High level source current	10	–	–	mA	V _{OH} = V _{DD} – 1.0 V, see the limitations of the total current in the note for V _{OH}
I _{OL}	Low level sink current	25	–	–	mA	V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL}
V _{IL}	Input low level	–	–	0.8	V	V _{DD} = 3.0 to 5.25
V _{IH}	Input high level	2.1	–	–	V	V _{DD} = 3.0 to 5.25
V _H	Input hysteresis	–	60	–	mV	
I _{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C _{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C _{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

Table 14. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull-up resistor	4	5.6	8	kΩ	
R _{PD}	Pull-down resistor	4	5.6	8	kΩ	
V _{OH}	High output level	V _{DD} – 0.4	–	–	V	I _{OH} = 2.5 mA (6.25 Typ), V _{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I _{OH} budget)
V _{OL}	Low output level	–	–	0.75	V	I _{OL} = 10 mA, V _{DD} = 2.4 to 3.0 V (90 mA maximum combined I _{OL} budget)
I _{OH}	High level source current	2.5	–	–	mA	V _{OH} = V _{DD} – 0.4 V, see the limitations of the total current in the note for V _{OH}
I _{OL}	Low level sink current	10	–	–	mA	V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL}
V _{IL}	Input low level	–	–	0.75	V	V _{DD} = 2.4 to 3.0
V _{IH}	Input high level	2.0	–	–	V	V _{DD} = 2.4 to 3.0
V _H	Input hysteresis	–	90	–	mV	
I _{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C _{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C _{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

AC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25°C and are for design guidance only.

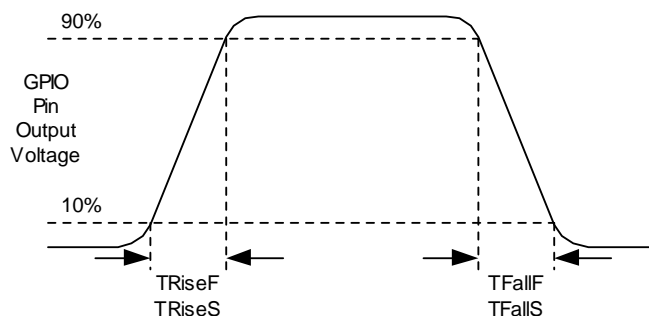
Table 25. 5 V and 3.3 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
T_{RiseF}	Rise time, normal strong mode, $\text{Clload} = 50 \text{ pF}$	3	–	18	ns	$V_{\text{DD}} = 4.5 \text{ to } 5.25 \text{ V}$, 10% to 90%
T_{FallF}	Fall time, normal strong mode, $\text{Clload} = 50 \text{ pF}$	2	–	18	ns	$V_{\text{DD}} = 4.5 \text{ to } 5.25 \text{ V}$, 10% to 90%
T_{RiseS}	Rise time, slow strong mode, $\text{Clload} = 50 \text{ pF}$	7	27	–	ns	$V_{\text{DD}} = 3 \text{ to } 5.25 \text{ V}$, 10% to 90%
T_{FallS}	Fall time, slow strong mode, $\text{Clload} = 50 \text{ pF}$	7	22	–	ns	$V_{\text{DD}} = 3 \text{ to } 5.25 \text{ V}$, 10% to 90%

Table 26. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
T_{RiseF}	Rise time, normal strong mode, $\text{Clload} = 50 \text{ pF}$	6	–	50	ns	$V_{\text{DD}} = 2.4 \text{ to } 3.0 \text{ V}$, 10% to 90%
T_{FallF}	Fall time, normal strong mode, $\text{Clload} = 50 \text{ pF}$	6	–	50	ns	$V_{\text{DD}} = 2.4 \text{ to } 3.0 \text{ V}$, 10% to 90%
T_{RiseS}	Rise time, slow strong mode, $\text{Clload} = 50 \text{ pF}$	18	40	120	ns	$V_{\text{DD}} = 2.4 \text{ to } 3.0 \text{ V}$, 10% to 90%
T_{FallS}	Fall time, slow strong mode, $\text{Clload} = 50 \text{ pF}$	18	40	120	ns	$V_{\text{DD}} = 2.4 \text{ to } 3.0 \text{ V}$, 10% to 90%

Figure 15. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25°C and are for design guidance only.

Table 27. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator mode response time, 50 mV overdrive	–	–	100 200	ns ns	$V_{\text{DD}} \geq 3.0 \text{ V}$ $2.4 \text{ V} < V_{\text{DD}} < 3.0 \text{ V}$

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, 3.0 V to 3.6 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5 V and 3.3 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, $V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	No capture, $V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50 ^[26]	–	–	ns	
Counter	Input clock frequency					
	No enable input, $V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	No enable input, $V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50 ^[26]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50 ^[26]	–	–	ns	
	Disable mode	50 ^[26]	–	–	ns	
	Input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50 ^[26]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75\text{ V}$, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	

Note

26. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

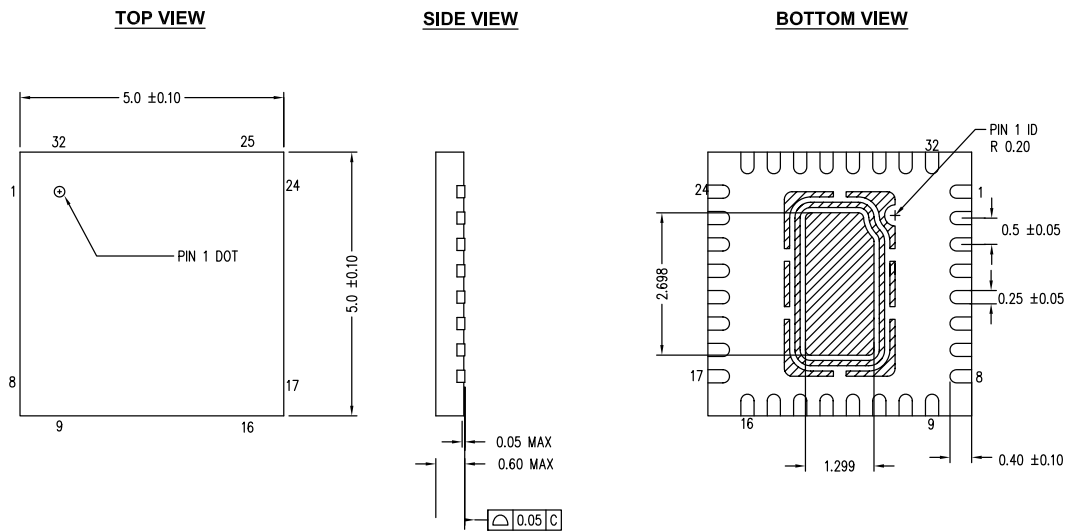
Table 31. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F _{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	


Table 32. 2.7 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F _{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Figure 21. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



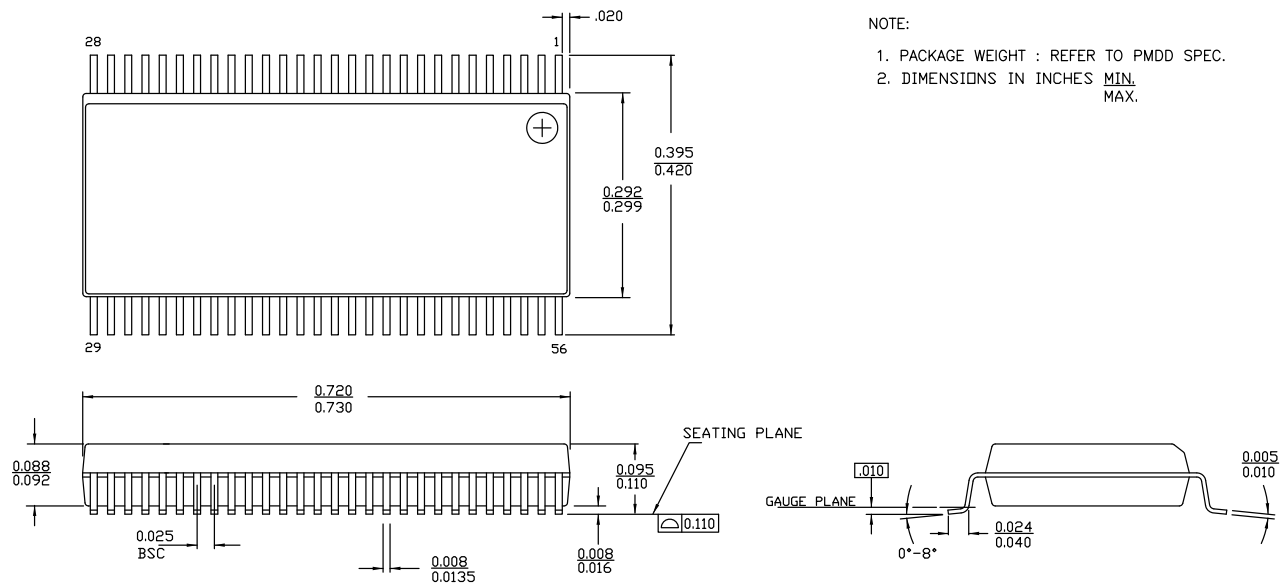
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.

Figure 22. 56-pin SSOP (300 Mils) Package Outline, 51-85062



NOTE:

1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.
MAX.

51-85062 *F

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C21x34B family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of cost at <http://www.cypress.com> and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com>.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3280-BK1 Universal CapSense Controller - Basic Kit 1

The [CY3280-BK1](#) Universal CapSense Controller Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with controller boards for the CY8C20x34 and CY8C21x34 PSoC devices as well as a breadboard module and a button(5) / slider module.

CY3215-DK Basic Development Kit

The [CY3215-DK](#) is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The [CY3210-MiniProg1 kit](#) allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The [CY3210-PSoCEval1 kit](#) features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The [CY3214-PSoCEvalUSB evaluation kit](#) features a development board for the CY8C24794-24LFXI PSoC device. The board includes both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MiniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

Document Conventions

Units of Measure

Table 40 lists the units of measures.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	μH	microhenry
dB	decibels	μs	microsecond
°C	degree Celsius	ms	millisecond
μF	microfarad	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	μV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	μW	microwatts
μA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

Glossary

active high	<ol style="list-style-type: none"> 1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	<ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	<ol style="list-style-type: none"> 1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurement
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	<ol style="list-style-type: none"> 1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	<ol style="list-style-type: none"> 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V _{DD}	A name for a power net meaning 'voltage drain'. The most positive power supply signal. Usually 5 V or 3.3 V.
V _{SS}	A name for a power net meaning 'voltage source'. The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

CY8C21X34 Errata Summary

The following table defines the errata applicability to available CY8C21X34 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C21X34	A	No fix is currently planned.
[2]. I2C Errors	CY8C21X34	A	No fix is currently planned.

1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 °C to 70 °C. This problem does not affect end-product usage between 0 °C and 70 °C.

■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

■ Trigger Condition(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 °C to +70 °C.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

■ Fix Status

No fix is currently planned.

2. I²C Errors

■ Problem Definition

The I²C block exhibits occasional data and bus corruption errors when the I²C master initiates transactions while the device is transitioning in to or out of sleep mode.

■ Parameters Affected

Affects reliability of I²C communication to device, between I²C master, and third party I²C slaves.

■ Trigger Condition(S)

Triggered by transitions into and out of the device's sleep mode.

■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

■ Workaround

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I²C block from the bus prior to going to sleep modes. I²C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I²C transaction

■ Fix Status

Will not be fixed.

Document History Page

Document Title: CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity Document Number: 001-67345				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3169205	YVA	02/16/2011	New data sheet.
*A	3247292	YVA	05/11/2011	Updated Packaging Information . Post to external web.
*B	3846480	SRLI	12/19/2012	Updated Features . Updated Packaging Information : spec 51-85062 – Changed Revision from *D to *F. spec 001-48913 – Changed Revision from *B to *C. spec 001-44368 – Changed Revision from *B to *C. spec 001-30999 – Changed Revision from *C to *D. spec 51-85068 – Changed Revision from *D to *E. Updated Ordering Information (Updated part numbers).
*C	3894458	SRLI	02/09/2013	Updated Document Title to read as “CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity”. Updated Packaging Information (Updated Solder Reflow Peak Temperature (Changed Time at Maximum Temperature from 20 s to 30 s in Table 37)).
*D	4297481	DCHE	03/04/2014	Updated Development Tools : Added hyperlink for “PSoC Designer™”. Updated PSoC Designer Software Subsystems : Updated In-Circuit Emulator : Added hyperlink for “in-circuit emulator” in description. Updated Development Tool Selection : Updated Software : Updated PSoC Designer™ : Updated hyperlinks in description. Updated PSoC Programmer : Updated hyperlinks in description. Updated Development Kits : Updated description. Updated Evaluation Tools : Updated CY3210-MiniProg1 : Updated hyperlinks in description. Updated CY3214-PSoCEvalUSB : Updated hyperlinks in description. Updated Device Programmers : Updated CY3216 Modular Programmer : Updated hyperlinks in description. Updated Packaging Information : spec 001-44368 – Changed Revision from *C to *D. spec 001-48913 – Changed Revision from *C to *D. Updated to new template. Completing Sunset Review.

Document History Page (continued)

Document Title: CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity Document Number: 001-67345				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4476297	DCHE / ASRI	08/28/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added More Information . Added PSoC Designer . Removed “Getting Started”. Updated Electrical Specifications : Updated AC Electrical Characteristics : Updated AC Operational Amplifier Specifications : Updated Table 27 : Replaced V_{CC} with V_{DD} . Updated Packaging Information : Removed spec 001-44368 *D. Updated Development Tool Selection : Updated Device Programmers : Removed “CY3207ISSP In-System Serial Programmer (ISSP)”. Updated Ordering Information (Updated part numbers).
*F	4670626	DCHE	02/25/2015	Added Errata and references to errata items on page 1.
*G	5617615	DCHE	02/03/2017	Updated Packaging Information : spec 51-85077 – Changed Revision from *E to *F. spec 51-85079 – Changed Revision from *E to *F. Updated Reference Documents : Removed spec 001-17397 and spec 001-14503 as both specs are obsolete. Updated to new template. Completing Sunset Review.