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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 28x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21434b-24ltxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

Note: For CY8C21x34B devices related Application note please click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

Note: For CY8C21x34B devices related Development Kits please click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

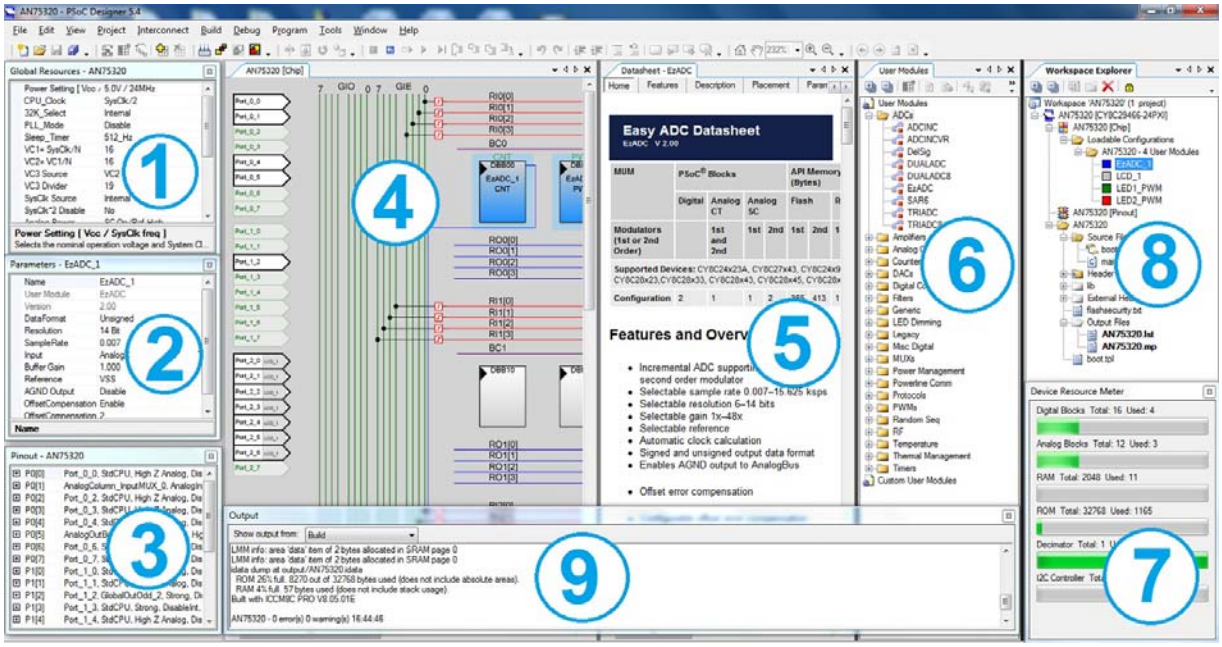
PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to **PSoC® Designer** > **Help** > **Documentation** > **Designer Specific Documents** > **IDE User Guide**.

Figure 1. PSoC Designer Layout



Contents

PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in Figure 2, consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C21x34B PSoC device includes four digital blocks and four analog blocks. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I^2C functionality to implement an I^2C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A SMP that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

The Digital System

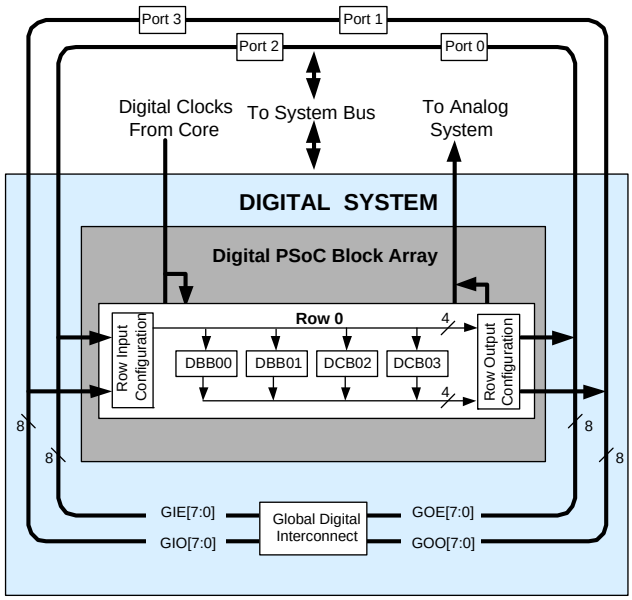
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8- with selectable parity
- Serial peripheral interface (SPI) master and slave
- I^2C slave and multi-master
- CRC/generator (8-bit)
- IrDA
- PRS generators (8-bit to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 7.

Figure 2. Digital System Block Diagram



32-pin Part Pinout

Figure 7. CY8C21434B 32-pin PSoC Device

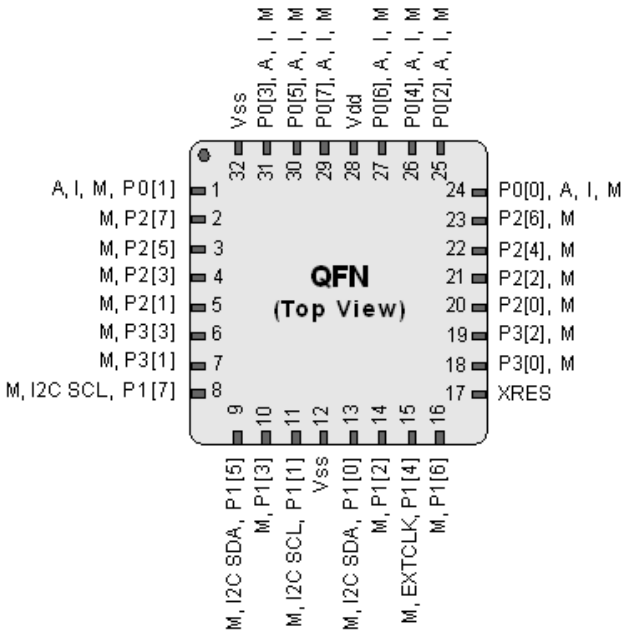


Figure 8. CY8C21634B 32-pin PSoC Device

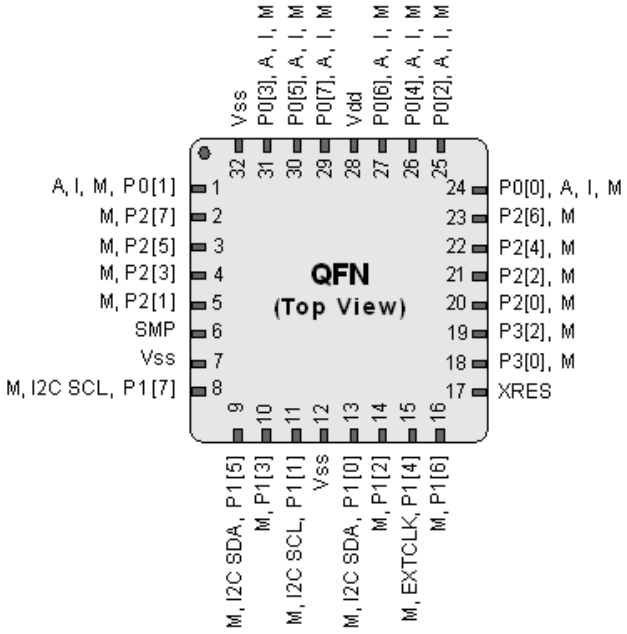


Figure 9. CY8C21434B 32-pin Sawn PSoC Device Sawn

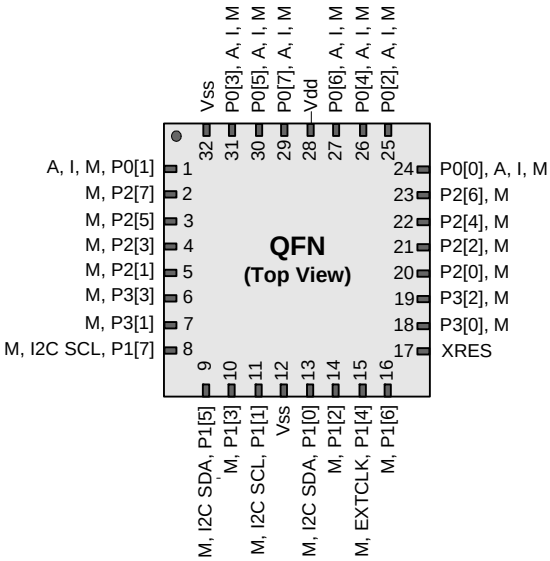
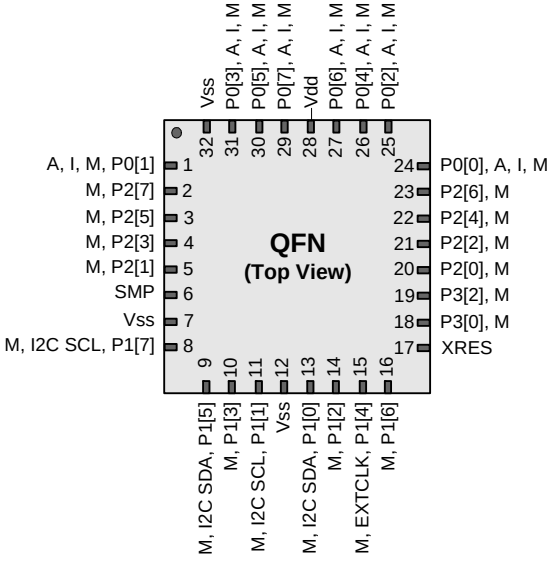


Figure 10. CY8C21634B 32-pin Sawn PSoC Device Sawn



56-pin Part Pinout

The 56-Pin SSOP part is for the CY8C21001 on-chip debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Figure 11. CY8C21001 56-pin PSoC Device

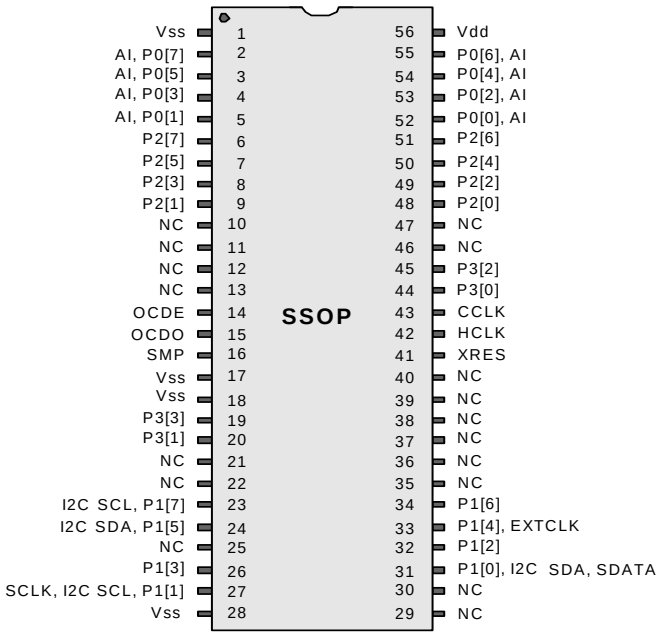


Table 6. Pin Definitions – CY8C21001 56-pin (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection
11			NC	No connection
12			NC	No connection
13			NC	No connection
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	Power		V_{SS}	Ground connection
18	Power		V_{SS}	Ground connection

DC General-Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 13. 5 V and 3.3 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

Table 14. 2.7 V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget)
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget)
I_{OH}	High level source current	2.5	–	–	mA	V_{OH} = V_{DD} – 0.4 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	10	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0
V_H	Input hysteresis	–	90	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

Table 18. DC Switch Mode Pump (SMP) Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
E_3	Efficiency	35	50	–	%	Configured as in Note 11 Load is 5 mA. SMP trip voltage is set to 3.25 V
E_2	Efficiency	35	80	–	%	For I load = 1mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 µH inductor, 1 µF capacitor, and Schottky diode
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

DC Analog Mux Bus Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, the reset from the XRES pin, or reset from watchdog
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for pump trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 23. 5 V and 3.3 V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	IMO frequency for 24 MHz	23.4	24	24.6[19,20]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 13 on page 20. SLIMO mode = 0
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[19,20]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 13 on page 20. SLIMO mode = 1
F_{CPU1}	CPU frequency (5 V nominal)	0.091	24	24.6[19]	MHz	24 MHz only for SLIMO mode = 0
F_{CPU2}	CPU frequency (3.3 V nominal)	0.091	12	12.3[20]	MHz	SLIMO mode = 0
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.2[19,21]	MHz	Refer to AC Digital Block Specifications on page 30
F_{BLK33}	Digital PSoC block frequency (3.3 V nominal)	0	24	24.6[21]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the *PSoC Technical Reference Manual* for details on this timing
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[19,20]	MHz	Trimmed. Using factory trim values
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*
t_{jit_IMO}	24-MHz IMO cycle-to-cycle jitter (RMS)[22]	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS)[22]	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS)[22]	–	100	400	ps	

Notes
19. 4.75 V < V_{DD} < 5.25 V.
20. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
21. See the individual user module datasheets for information on maximum frequencies for user modules.
22. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5 V and 3.3 V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	$V_{DD} \geq 4.75$ V	–	–	49.2	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, $V_{DD} \geq 4.75$ V	–	–	49.2	MHz	
	No capture, $V_{DD} < 4.75$ V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[26]	–	–	ns	
Counter	Input clock frequency					
	No enable input, $V_{DD} \geq 4.75$ V	–	–	49.2	MHz	
	No enable input, $V_{DD} < 4.75$ V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[26]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[26]	–	–	ns	
	Disable mode	50[26]	–	–	ns	
	Input clock frequency					
	$V_{DD} \geq 4.75$ V	–	–	49.2	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	$V_{DD} \geq 4.75$ V	–	–	49.2	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[26]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75$ V, 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75$ V, 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75$ V	–	–	24.6	MHz	

Note
26. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 31. 3.3 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 32. 2.7 V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 35. 2.7 V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	Low period of the SCL clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	High period of the SCL clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated start condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$T_{SUSTOI2C}$	Setup time for stop condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

Figure 16. Definition for Timing for Fast/Standard Mode on the I²C Bus

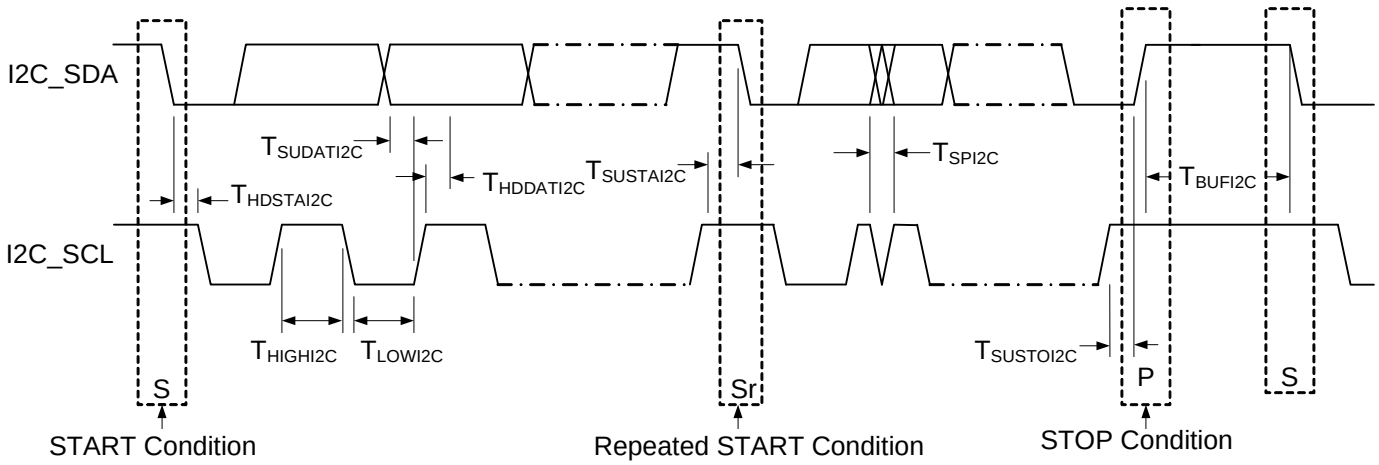
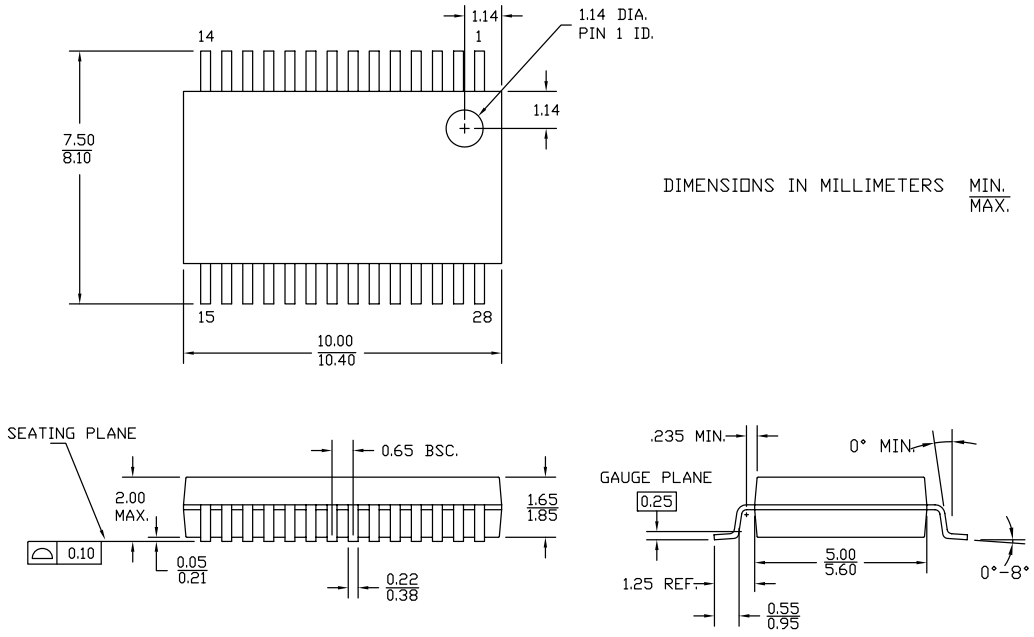
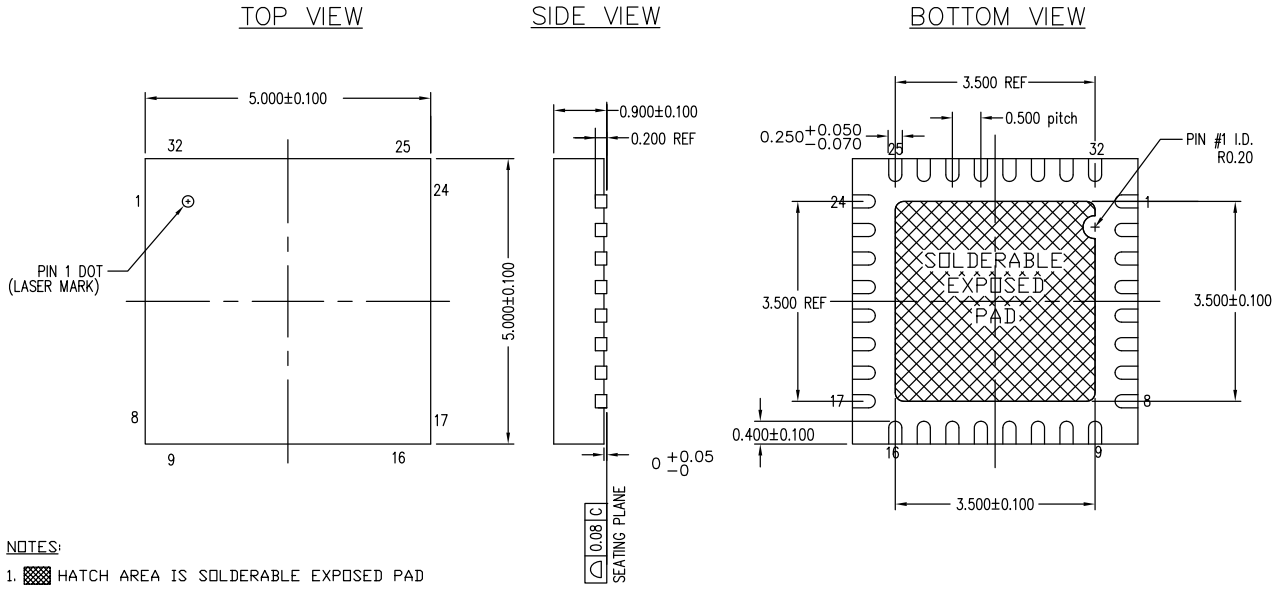


Figure 19. 28-pin SSOP (210 Mils) Package Outline, 51-85079



51-85079 *F

Figure 20. 32-pin QFN (5 × 5 × 1.0 mm) LT32B (3.5 × 3.5) E-Pad (Sawn) Package Outline, 001-30999

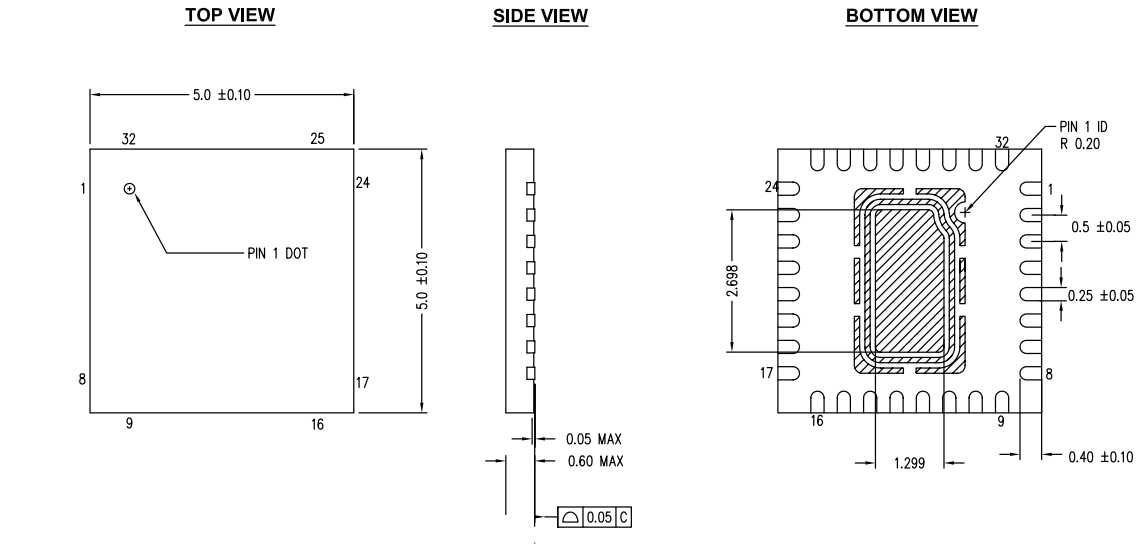


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: SEE CYPRESS PACKAGE MATERIAL DECLARATION DATASHEET (PMDD) POSTED ON THE CYPRESS WEB

001-30999 *D

Figure 21. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913

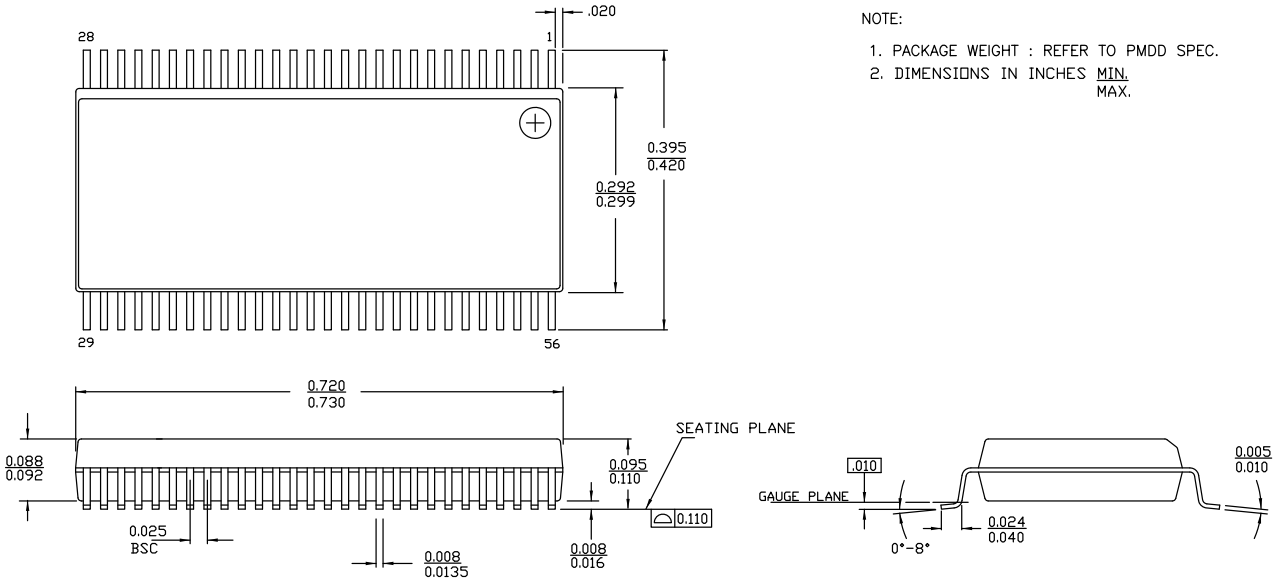


NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Important Note For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

Figure 22. 56-pin SSOP (300 Mils) Package Outline, 51-85062



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN. MAX.

51-85062 *F

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C21x34B family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of cost at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3280-BK1 Universal CapSense Controller - Basic Kit 1

The CY3280-BK1 Universal CapSense Controller Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with controller boards for the CY8C20x34 and CY8C21x34 PSoC devices as well as a breadboard module and a button(5) / slider module.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. The board includes both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

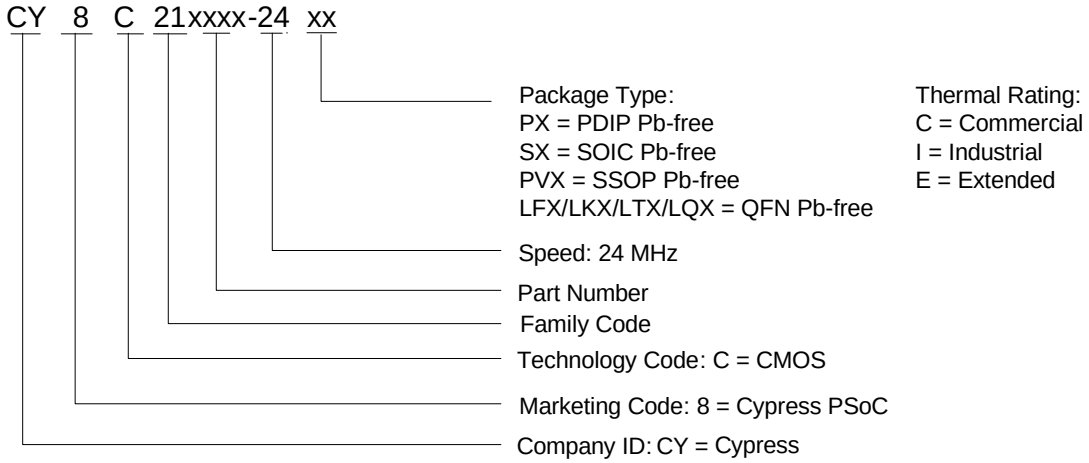
- PSoCEvalUSB board
- LCD module
- MIniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8C21234B-24SXI	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[35]	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21234B-24SXIT	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[35]	0	No
20-Pin (210-Mil) SSOP	CY8C21334B-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	16	16[35]	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21334B-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	16	16[35]	0	Yes
28-Pin (210-Mil) SSOP	CY8C21534B-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	24	24[35]	0	Yes
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21534B-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	24	24[35]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C21434B-24LTXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[35]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [36] (Tape and Reel)	CY8C21434B-24LTXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[35]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN	CY8C21434B-24LQXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[35]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN (Tape and Reel)	CY8C21434B-24LQXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[35]	0	Yes
56-Pin OCD SSOP	CY8C21001-24PVXI	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[35]	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Notes
35. All Digital I/O Pins also connect to the common analog mux.
36. Refer to the section 32-pin Part Pinout on page 13 for pin differences.

Document Conventions

Units of Measure

Table 40 lists the units of measures.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µH	microhenry
dB	decibels	µs	microsecond
°C	degree Celsius	ms	millisecond
µF	microfarad	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning ‘voltage drain’. The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning ‘voltage source’. The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the PSoC® Programmable System-on-Chip CY8C21X34. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21X34	CY8C21234-24SXI
	CY8C21234-24SXIT
	CY8C21334-24PVXI
	CY8C21334-24PVXIT
	CY8C21534-24PVXI
	CY8C21534-24PVXIT
	CY8C21434-24LFXI
	CY8C21434-24LFXIT
	CY8C21434-24LKXI
	CY8C21434-24LKXIT
	CY8C21634-24LFXI
	CY8C21634-24LFXIT
	CY8C21434-24LTXI
	CY8C21434-24LTXIT
	CY8C21434-24LQXI
	CY8C21434-24LQXIT
	CY8C21634-24LTXI
	CY8C21634-24LTXIT
	CY8C21001-24PVXI

CY8C21X34 Qualification Status

Product Status: Production

Document History Page

Document Title: CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity Document Number: 001-67345				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3169205	YVA	02/16/2011	New data sheet.
*A	3247292	YVA	05/11/2011	Updated Packaging Information. Post to external web.
*B	3846480	SRLI	12/19/2012	Updated Features. Updated Packaging Information: spec 51-85062 – Changed Revision from *D to *F. spec 001-48913 – Changed Revision from *B to *C. spec 001-44368 – Changed Revision from *B to *C. spec 001-30999 – Changed Revision from *C to *D. spec 51-85068 – Changed Revision from *D to *E. Updated Ordering Information (Updated part numbers).
*C	3894458	SRLI	02/09/2013	Updated Document Title to read as “CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity”. Updated Packaging Information (Updated Solder Reflow Peak Temperature (Changed Time at Maximum Temperature from 20 s to 30 s in Table 37)).
*D	4297481	DCHE	03/04/2014	Updated Development Tools: Added hyperlink for “PSoC Designer™”. Updated PSoC Designer Software Subsystems: Updated In-Circuit Emulator: Added hyperlink for “in-circuit emulator” in description. Updated Development Tool Selection: Updated Software: Updated PSoC Designer™: Updated hyperlinks in description. Updated PSoC Programmer: Updated hyperlinks in description. Updated Development Kits: Updated description. Updated Evaluation Tools: Updated CY3210-MiniProg1: Updated hyperlinks in description. Updated CY3214-PSoCEvalUSB: Updated hyperlinks in description. Updated Device Programmers: Updated CY3216 Modular Programmer: Updated hyperlinks in description. Updated Packaging Information: spec 001-44368 – Changed Revision from *C to *D. spec 001-48913 – Changed Revision from *C to *D. Updated to new template. Completing Sunset Review.