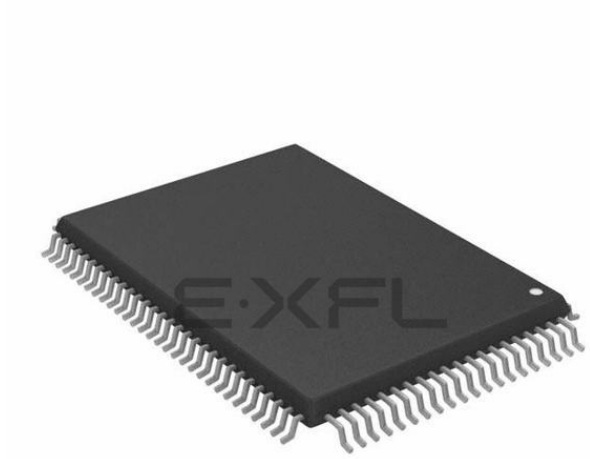

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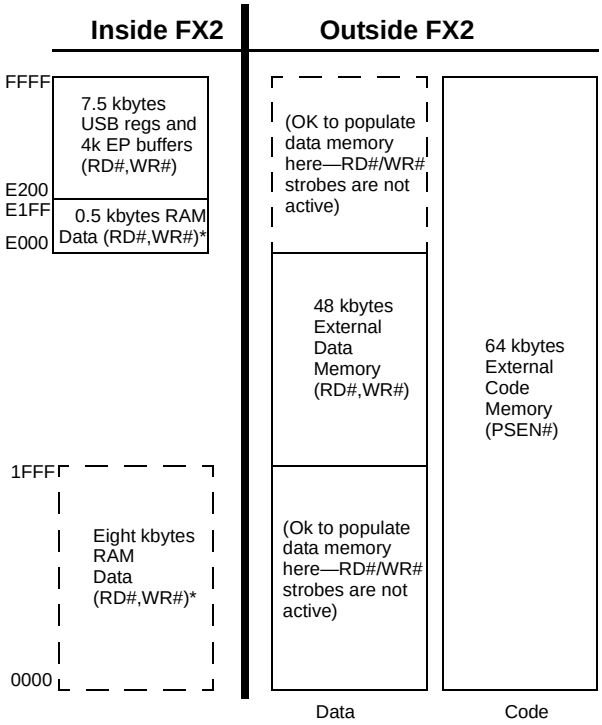
Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	40
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013-100ac

LIST OF FIGURES

3.10.3 External Code Memory, EA = 1

The bottom eight kbytes of program memory is external, and therefore the bottom eight kbytes of internal RAM is accessible only as data memory.



*SUDPTR, USB upload/download, I^2C-compatible interface boot access

Figure 3-2. External Code Memory, EA = 1

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that will be executed to perform the desired data move between the CY7C68013 and the external design.

3.14.1 Six Control OUT Signals

The 100- and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

3.14.2 Six Ready IN Signals

The 100- and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

3.14.3 Nine GPIF Address OUT signals

Nine GPIF address lines are available in the 100- and 128-pin packages, GPIFADR[8..0]. The GPIF address lines allow indexing through up to a 512-byte block of RAM. If more address lines are needed, I/O port pins can be used.

3.14.4 Long Transfer Mode

In master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 4,294,967,296 bytes. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

3.15 USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 8-kbyte RAM and of the internal 512-byte scratch pad RAM via a vendor-specific command. This capability is normally used when “soft” downloading user code and is available only to and from internal RAM, whether the 8051 is held in reset or running. The available RAM spaces are 8 kbytes from 0x0000–0x1FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad RAM).

Note: A “loader” running in internal RAM can be used to transfer downloaded data to external memory.

3.16 Autopointer Access

FX2 provides two identical autopointers. They are similar to the internal 8051 data pointers, but with an additional feature: they can optionally increment a pointer address after every memory access. This capability is available to and from both internal and external RAM. The autopointers are available in external FX2 registers, under control of a mode bit (AUTOPTRSETUP.0). Using the external FX2 autopointer access (at 0xE67B – 0xE67C) allows the autopointer to access all RAM, internal and external to the part. Also, the autopointers can point to any FX2 register or endpoint buffer space. When autopointer access to external memory is enabled, location 0xE67B and 0xE67C in XDATA and PDATA space cannot be used.

3.17 I^2C-compatible Controller

FX2 has one I^2C-compatible port that is driven by two internal controllers, one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051, once running, uses to control external I^2C-compatible devices. The I^2C-compatible port operates in master mode only.

3.17.1 I^2C-compatible Port Pins

The I^2C-compatible pins SCL and SDA must have external 2.2-kΩ pull-up resistors. External EEPROM device address pins must be configured properly. See *Table 3-7* for configuring the device address pins.

Table 3-7. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00[4]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1

3.17.2 I²C-compatible Interface Boot Load Access

At power-on reset the I²C-compatible interface boot loader will load the VID/PID/DID/a configuration byte and up to 8 kbytes of program/data. The available RAM spaces are 8 kbytes from 0x0000–0x1FFF and 512 bytes from 0xE000–0xE1FF. The 8051 will be in reset. I²C-compatible interface boot loads only occur after power-on reset.

3.17.3 I²C-compatible Interface General Purpose Access

The 8051 can control peripherals connected to the I²C-compatible bus using the I2CTL and I2DAT registers. FX2 provides I²C compatible master control only, it is never an I²C-compatible slave.

4.0 Pin Assignments

Figure 4-1 identifies all signals for the four package types. The following pages illustrate the individual pin diagrams, plus a combination diagram showing which of the full set of signals are available in the 128-, 100-, and 56-pin packages.

The 56-pin package is the lowest-cost version. The signals on the left edge of the 56-pin package in *Figure 4-1* are common to all versions in the FX2 family. Three modes are available in all package versions: Port, GPIF master, and Slave FIFO. These modes define the signals on the right edge of the diagram. The 8051 selects the interface mode using the IFCONFIG[1:0] register bits. Port mode is the power-on default configuration.

The 100-pin package adds functionality to the 56-pin package by adding these pins:

- PORTC or alternate GPIFADR[7...0] address signals
- PORTE or alternate GPIFADR8 address signals and 7 more 8051 signals
- 3 GPIF Control signals
- 4 GPIF Ready signals
- Nine 8051 signals (two USARTs, three timer inputs, INT4,and INT5#)
- BKPT, RD#, WR#

The 128-pin package is the full version, adding the 8051 address and data buses plus control signals. Note that two of the required signals, RD# and WR#, are present in the 100-pin version. In the 100-pin and 128-pin versions, an 8051 control bit can be set to pulse the RD# and WR# pins when the 8051 reads from/writes to PORTC.

Note:

4. This EEPROM does not have address pins.

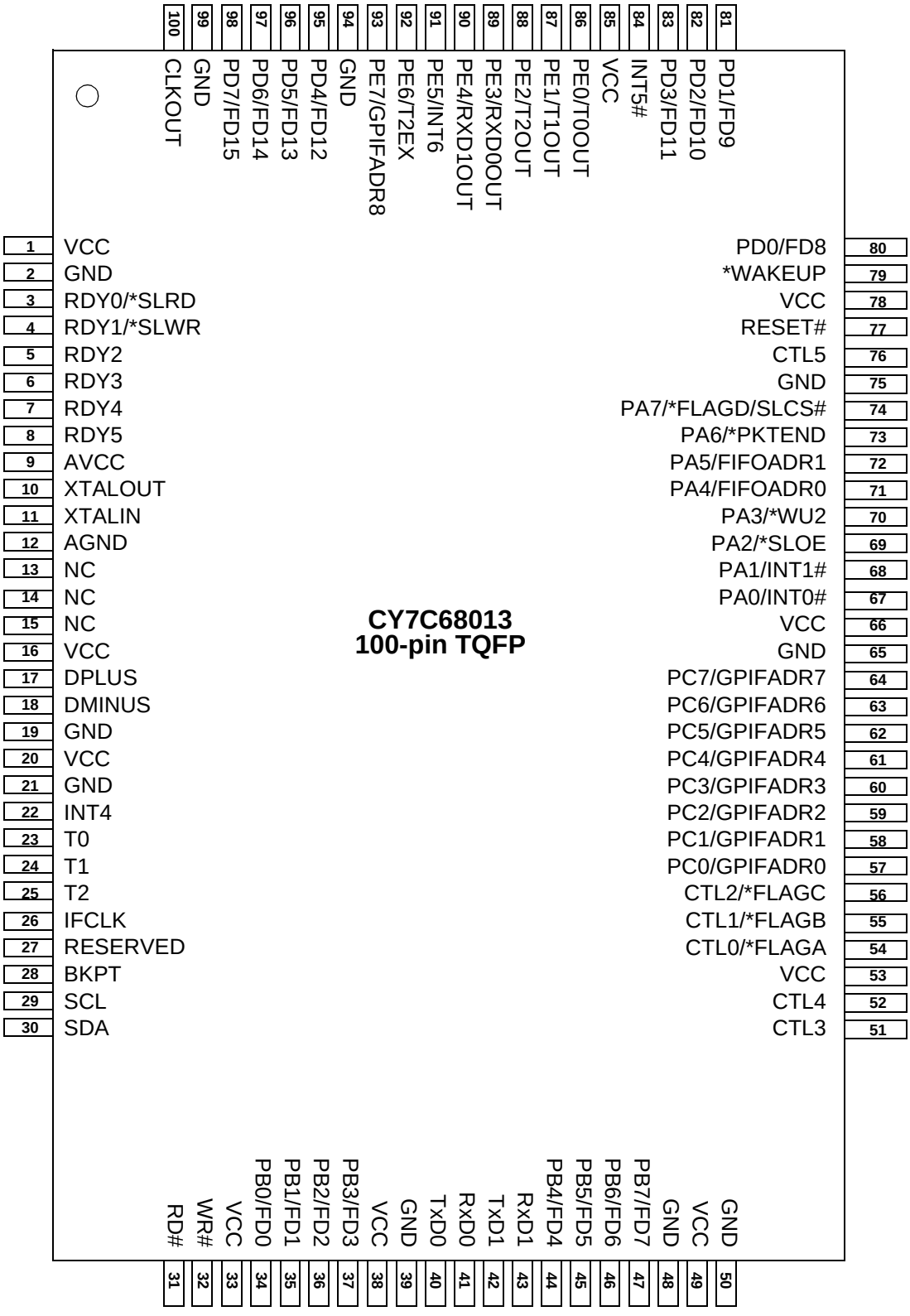


Figure 4-3. CY7C68013 100-pin TQFP Pin Assignment

* denotes programmable polarity

CY7C68013
56-pin SSOP

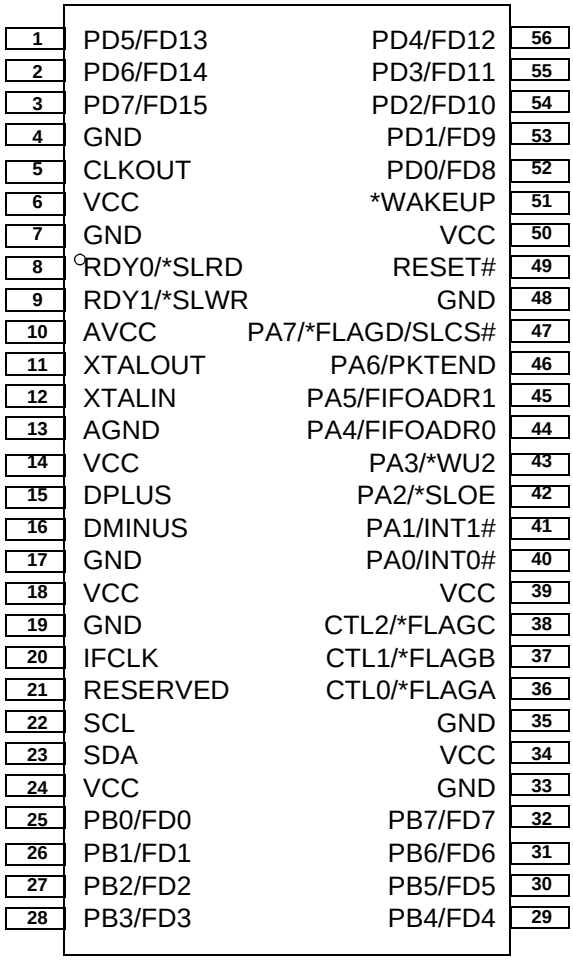


Figure 4-4. CY7C68013 56-pin SSOP Pin Assignment

* denotes programmable polarity

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
35				EA	Input	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x1FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	XTALIN	Input	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24 MHz square wave derived from another clock source.
11	10	11	4	XTALOUT	Output	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	CLKOUT	O/Z	12 MHz	12-, 24- or 48-MHz clock, phase locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may tri-state this output by setting CPUCS.1 = 1.
Port A							
82	67	40	33	PA0 or INT0#	I/O/Z	I (PA0)	Multiplexed pin whose function is selected by: PORTACFG.0 **PA0** is a bidirectional IO port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
83	68	41	34	PA1 or INT1#	I/O/Z	I (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional IO port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0).
84	69	42	35	PA2 or SLOE	I/O/Z	I (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. **PA2** is a bidirectional IO port pin. **SLOE** is an input-only output enable with programmable polarity (FIFOPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0].
85	70	43	36	PA3 or WU2	I/O/Z	I (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 **PA3** is a bidirectional I/O port pin. **WU2** is an alternate source for **USB Wakeup,** enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Asserting this pin inhibits the chip from suspending, if WU2EN=1.
89	71	44	37	PA4 or FIFOADR0	I/O/Z	I (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FIFOADR0** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	PA5 or FIFOADR1	I/O/Z	I (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FIFOADR1** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
91	73	46	39	PA6 or PKTEND	I/O/Z	I (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. **PA6** is a bidirectional I/O port pin. **PKTEND** is an input-only packet end with programmable polarity (FIFOPOLAR.5) for the slave FIFOs connected to FD[7..0] or FD[15..0].

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
92	74	47	40	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. **PA7** is a bidirectional I/O port pin. **FLAGD** is a programmable slave-FIFO output status flag signal. **SLCS#** gates all other slave FIFO enable/strobes
Port B							
44	34	25	18	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **FD[0]** is the bidirectional FIFO/GPIF data bus.
45	35	26	19	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **FD[1]** is the bidirectional FIFO/GPIF data bus.
46	36	27	20	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **FD[2]** is the bidirectional FIFO/GPIF data bus.
47	37	28	21	PB3 or TXD1 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **FD[3]** is the bidirectional FIFO/GPIF data bus.
54	44	29	22	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **FD[4]** is the bidirectional FIFO/GPIF data bus.
55	45	30	23	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **FD[5]** is the bidirectional FIFO/GPIF data bus.
56	46	31	24	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **FD[6]** is the bidirectional FIFO/GPIF data bus.
57	47	32	25	PB7 or FD[7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **FD[7]** is the bidirectional FIFO/GPIF data bus.
PORT C							
72	57			PC0 or GPIFADR0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 **PC0** is a bidirectional I/O port pin. **GPIFADR0** is a GPIF address output pin.
73	58			PC1 or GPIFADR1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 **PC1** is a bidirectional I/O port pin. **GPIFADR1** is a GPIF address output pin.
74	59			PC2 or GPIFADR2	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 **PC2** is a bidirectional I/O port pin. **GPIFADR2** is a GPIF address output pin.
75	60			PC3 or GPIFADR3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 **PC3** is a bidirectional I/O port pin. **GPIFADR3** is a GPIF address output pin.
76	61			PC4 or GPIFADR4	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 **PC4** is a bidirectional I/O port pin. **GPIFADR4** is a GPIF address output pin.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
77	62			PC5 or GPIFADR5	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 **PC5** is a bidirectional I/O port pin. **GPIFADR5** is a GPIF address output pin.
78	63			PC6 or GPIFADR6	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 **PC6** is a bidirectional I/O port pin. **GPIFADR6** is a GPIF address output pin.
79	64			PC7 or GPIFADR7	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 **PC7** is a bidirectional I/O port pin. **GPIFADR7** is a GPIF address output pin.
PORT D							
102	80	52	45	PD0 or FD[8]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	46	PD1 or FD[9]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	47	PD2 or FD[10]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	48	PD3 or FD[11]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	49	PD4 or FD[12]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	50	PD5 or FD[13]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	51	PD6 or FD[14]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	52	PD7 or FD[15]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E							
108	86			PE0 or T0OUT	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87			PE1 or T1OUT	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
40	31			RD#	Output	H	**RD#** is the active-LOW read strobe output for external memory.
38				OE#	Output	H	**OE#** is the active-LOW output enable for external memory.
33	27	21	14	Reserved	Input	N/A	Reserved. Connect to ground.
101	79	51	44	WAKEUP	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB® chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	SCL	OD	Z	**Clock** for the **I^2C-compatible interface.** Connect to V_{CC} with a 2.2K resistor, **even if no I^2C-compatible peripheral is attached**.
37	30	23	16	SDA	OD	Z	**Data** for **I^2C-compatible interface**. Connect to V_{CC} with a 2.2K resistor, **even if no I^2C-compatible peripheral is attached**.
2	1	6	55	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
17	16	14	7	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
26	20	18	11	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
43	33	24	17	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
48	38	34	27	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
64	49	39	32	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
68	53	50	43	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
81	66			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
100	78			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
107	85			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
3	2	4	53	GND	Ground	N/A	Ground.
20	19	7	56	GND	Ground	N/A	Ground.
27	21	17	10	GND	Ground	N/A	Ground.
49	39	19	12	GND	Ground	N/A	Ground.
58	48	33	26	GND	Ground	N/A	Ground.
65	50	35	28	GND	Ground	N/A	Ground.
80	65	48	41	GND	Ground	N/A	Ground.
93	75			GND	Ground	N/A	Ground.
116	94			GND	Ground	N/A	Ground.
125	99			GND	Ground	N/A	Ground.
14	13			NC	N/A	N/A	No-connect. This pin must be left open.
15	14			NC	N/A	N/A	No-connect. This pin must be left open.
16	15			NC	N/A	N/A	No-connect. This pin must be left open.

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E631 F.S	1	EP2FIFOPFL[6]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632 H.S.	1	EP4FIFOPFH[6]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E632 F.S	1	EP4FIFOPFH[6]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E633 H.S.	1	EP4FIFOPFL[6]	Endpoint 4 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E633 F.S	1	EP4FIFOPFL[6]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634 H.S.	1	EP6FIFOPFH[6]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb
E634 F.S	1	EP6FIFOPFH[6]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb
E635 H.S.	1	EP6FIFOPFL[6]	Endpoint 6 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E635 F.S	1	EP6FIFOPFL[6]	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636 H.S.	1	EP8FIFOPFH[6]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E636 F.S	1	EP8FIFOPFH[6]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E637 H.S.	1	EP8FIFOPFL[6]	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E637 F.S	1	EP8FIFOPFL[6]	Endpoint 8 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	reserved											
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
	4	reserved											
E648	1	INPKTEND[6]	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	R/W
E649	7	OUTPKTEND[6]	Force OUT Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
		INTERRUPTS											
E650	1	EP2FIFOIE[6]	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E651	1	EP2FIFOIRQ[6]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E652	1	EP4FIFOIE[6]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ[6]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E654	1	EP6FIFOIE[6]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ[6]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E656	1	EP8FIFOIE[6]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ[6]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxxx	RW
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	NAKIRQ	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	xxxxxxxx	RW
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW
E65D	1	USBIRQ	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	RW
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	xxxxxxxx	RW
E660	1	GPIFIE[6]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ[6]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	xxxx000x	RW
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSETUP	Interrupt 2&4 Setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW

9.0 AC Electrical Characteristics

9.1 USB Transceiver

USB 2.0-certified in full- and high-speed modes.

9.2 Program Memory Read

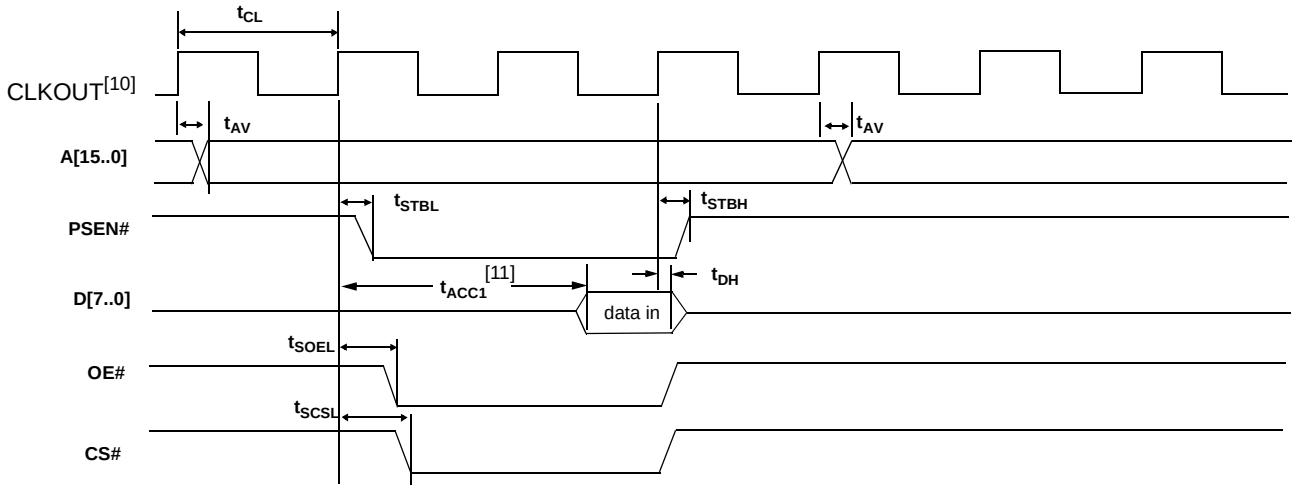


Figure 9-1. Program Memory Read Timing Diagram

Table 9-1. Program Memory Read Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		20.83		ns	48 MHz
			41.66		ns	24 MHz
			83.2		ns	12 MHz
t_{AV}	Delay from Clock to Valid Address	0		10.7	ns	
t_{STBL}	Clock to PSEN Low	0		8	ns	
t_{STBH}	Clock to PSEN High	0		8	ns	
t_{SOEL}	Clock to OE Low			11.1	ns	
t_{SCSL}	Clock to CS Low			13	ns	
t_{DSU}	Data Set-up to Clock	9.6			ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

10. CLKOUT is shown with positive polarity.
11. t_{ACC1} is computed from the above parameters as follows:
    t_{ACC1}(24 MHz) = 3*t_{CL} – t_{AV} –t_{DSU} = 106 ns
    t_{ACC1}(48 MHz) = 3*t_{CL} – t_{AV} – t_{DSU} = 43 ns.

9.5 GPIF Synchronous Signals

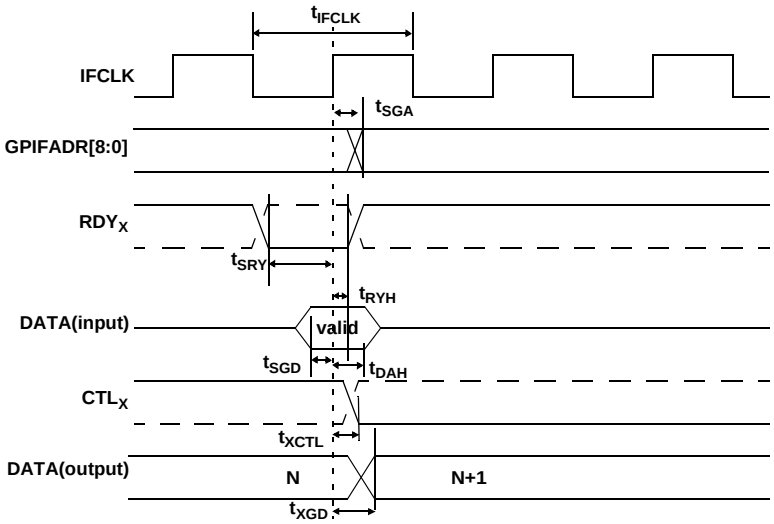


Figure 9-4. GPIF Synchronous Signals Timing Diagram[13]

Table 9-4. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK[14, 15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SRY}	RDY_X to Clock Set-up Time	8.9		ns
t_{RYH}	Clock to RDY_X	0		ns
t_{SGD}	GPIF Data to Clock Set-up Time	9.2		ns
t_{DAH}	GPIF Data Hold Time	0		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		7.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		11	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		6.7	ns

Table 9-5. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK[15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SRY}	RDY_X to Clock Set-up Time	2.9		ns
t_{RYH}	Clock to RDY_X	3.7		ns
t_{SGD}	GPIF Data to Clock Set-up Time	3.2		ns
t_{DAH}	GPIF Data Hold Time	4.5		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		11.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		15	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		10.7	ns

Notes:
13. Dashed lines denote signals with programmable polarity
14. GPIF asynchronous RDY_x signals have a minimum set-up time of 50 ns when using internal 48-MHz IFCLK.
15. IFCLK must not exceed 48 MHz.

9.6 Slave FIFO Synchronous Read

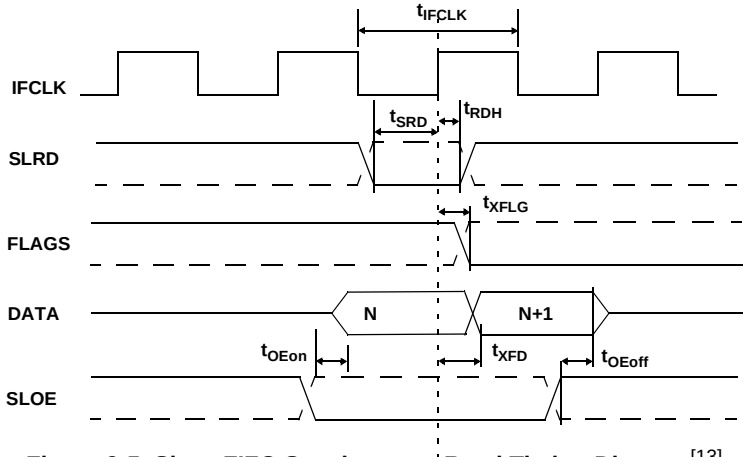


Figure 9-5. Slave FIFO Synchronous Read Timing Diagram[13]

Table 9-6. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK[15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SRD}	SLRD to Clock Set-up Time	18.7		ns
t_{RDH}	Clock to SLRD Hold Time	0		ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid		10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold		10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay		9.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay		11	ns

Table 9-7. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK[15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SRD}	SLRD to Clock Set-up Time	12.7		ns
t_{RDH}	Clock to SLRD Hold Time	3.7		ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid		10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold		10.5	ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay		13.5	ns
t_{XFD}	Clock to FIFO Data Output Propagation Delay		15	ns

9.7 Slave FIFO Asynchronous Read

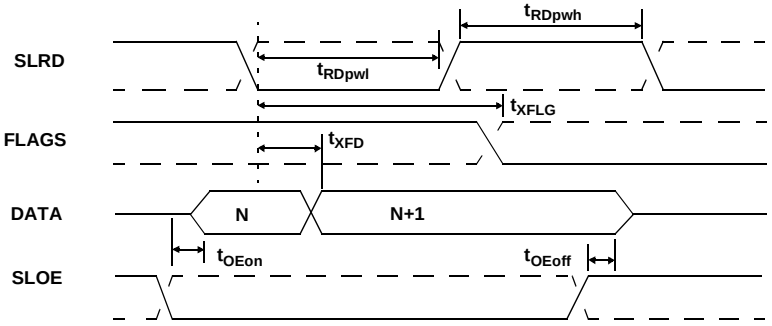


Figure 9-6. Slave FIFO Asynchronous Read Timing Diagram[13]

Table 9-8. Slave FIFO Asynchronous Read Parameters[16]

Parameter	Description	Min.	Max.	Unit
t_{RDpwl}	SLRD Pulse Width LOW	50		ns
t_{RDpwh}	SLRD Pulse Width HIGH	50		ns
t_{XFLG}	SLRD to FLAGS Output Propagation Delay		70	ns
t_{XFD}	SLRD to FIFO Data Output Propagation Delay		15	ns
t_{OEon}	SLOE Turn-on to FIFO Data Valid		10.5	ns
t_{OEoff}	SLOE Turn-off to FIFO Data Hold		10.5	ns

9.8 Slave FIFO Synchronous Write

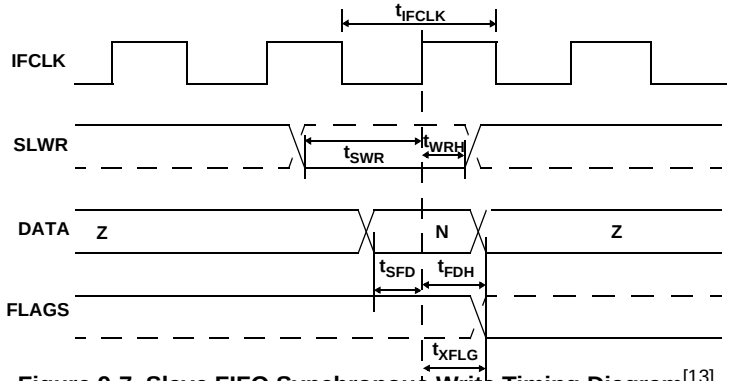


Figure 9-7. Slave FIFO Synchronous Write Timing Diagram[13]

Table 9-9. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK [15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SWR}	SLWR to Clock Set-up Time	18.1		ns
t_{WRH}	Clock to SLWR Hold Time	0		ns
t_{SFD}	FIFO Data to Clock Set-up Time	9.2		ns
t_{FDH}	Clock to FIFO Data Hold Time	0		ns
t_{XFLG}	Clock to FLAGS Output Propagation Time		9.5	ns

Note:
16. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

Table 9-10. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK [15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SWR}	SLWR to Clock Set-up Time	12.1		ns
t_{WRH}	Clock to SLWR Hold Time	3.6		ns
t_{SFD}	FIFO Data to Clock Set-up Time	3.2		ns
t_{FDH}	Clock to FIFO Data Hold Time	4.5		ns
t_{XFLG}	Clock to FLAGS Output Propagation Time		13.5	ns

9.9 Slave FIFO Asynchronous Write

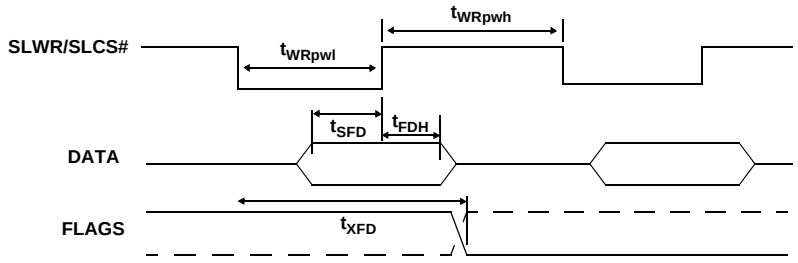


Figure 9-8. Slave FIFO Asynchronous Write Timing Diagram[13]

Table 9-11. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK [16]

Parameter	Description	Min.	Max.	Unit
t_{WRpwl}	SLWR Pulse LOW	50		ns
t_{WRpwh}	SLWR Pulse HIGH	70		ns
t_{SFD}	SLWR to FIFO DATA Set-up Time	10		ns
t_{FDH}	FIFO DATA to SLWR Hold Time	10		ns
t_{XFD}	SLWR to FLAGS Output Propagation Delay		70	ns

9.10 Slave FIFO Synchronous Packet End Strobe

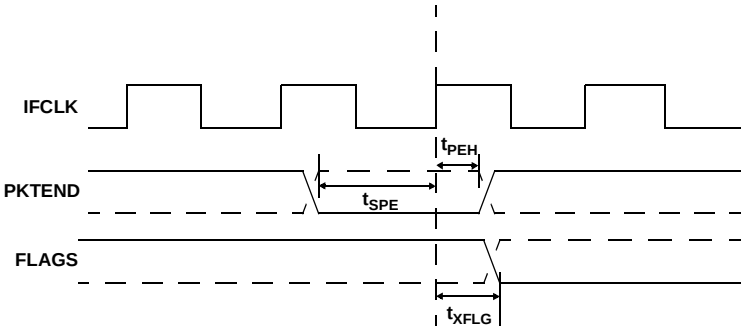


Figure 9-9. Slave FIFO Synchronous Packet End Strobe Timing Diagram[13]

Table 9-12. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK [15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SPE}	PKTEND to Clock Set-up Time	14.6		ns
t_{PEH}	Clock to PKTEND Hold Time	0		ns
t_{XFLG}	Clock to FLAGS Output Propagation Delay		9.5	ns

Table 9-16. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min.	Max.	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS Output Propagation Delay		10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA Output Propagation Delay		14.3	ns

9.14 Slave FIFO Synchronous Address

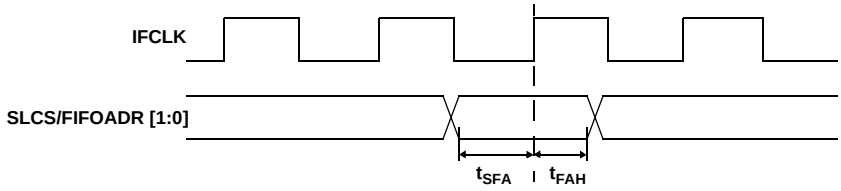


Figure 9-13. Slave FIFO Synchronous Address Timing Diagram

Table 9-17. Slave FIFO Synchronous Address Parameters [15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	Interface Clock Period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to Clock Set-up Time	25		ns
t_{FAH}	Clock to FIFOADR[1:0] Hold Time	10		ns

9.15 Slave FIFO Asynchronous Address

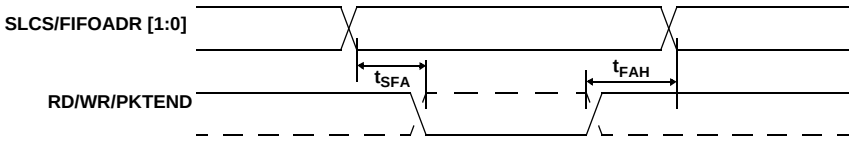


Figure 9-14. Slave FIFO Asynchronous Address Timing Diagram[13]

Table 9-18. Slave FIFO Asynchronous Address Parameters[16]

Parameter	Description	Min.	Max.	Unit
t_{SFA}	FIFOADR[1:0] to RD/WR/PKTEND Set-up Time	10		ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] Hold Time	10		ns

10.0 Ordering Information

Table 10-1. Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address /Data Busses
CY7C68013-128AC	128 TQFP	8K	40	16/8 bit
CY7C68013-100AC	100 TQFP	8K	40	–
CY7C68013-56PVC	56 SSOP	8K	24	–
CY7C68013-56LFC	56 QFN	8K	24	–
CY3681	EZ-USB FX2 Xcelerator Development Kit			

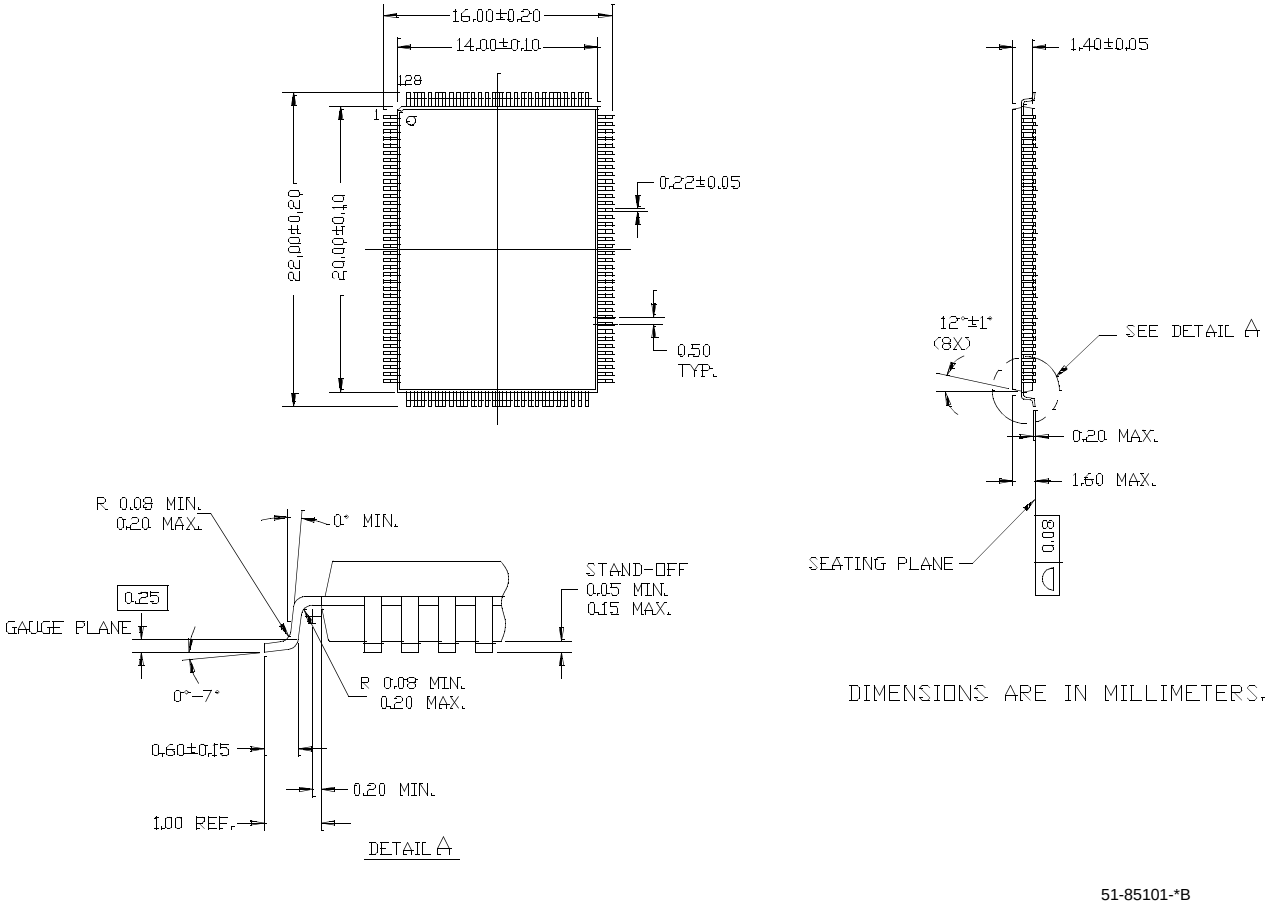


Figure 11-4. 128-Lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128

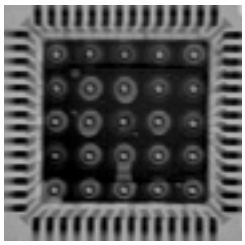


Figure 13-3. X-ray image of the assembly

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