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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	56-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013-56pvc

  - **Three counter/timers**
  - **Expanded interrupt system**
  - **Two data pointers**
- **Supports bus powered applications by using renumeration**
- **3.3V operation**
- **Smart Serial Interface Engine**
- **Vectored USB interrupts**
- **Separate data buffers for the SETUP and DATA portions of a CONTROL transfer**
- **Integrated I^2C-compatible controller, runs at 100 or 400 kHz**
- **48-MHz, 24-MHz, or 12-MHz 8051 operation**
- **Four integrated FIFOs**
  - **Brings glue and FIFOs inside for lower system cost**
  - **Automatic conversion to and from 16-bit buses**
  - **Master or slave operation**
  - **FIFOs can use externally supplied clock or asynchronous strobes**
  - **Easy interface to ASIC and DSP ICs**
- **Special autovectors for FIFO and GPIF interrupts**
- **Up to 40 general purpose I/Os**
- **Four package options—128-pin TQFP, 100-pin TQFP, 56-pin QFN and 56-pin SSOP**.

2.0 Applications

- **DSL modems**
- **ATA interface**
- **Memory card readers**
- **Legacy conversion devices**
- **Cameras**
- **Scanners**
- **Home PNA**
- **Wireless LAN**
- **MP3 players**
- **Networking**.

The “Reference Designs” section of the cypress website provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Please visit http://www.cypress.com for more information.

3.0 Functional Overview

3.1 USB Signaling Speed

FX2 operates at two of the three rates defined in the Universal Serial Bus Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2 does not support the low-speed signaling mode of 1.5 Mbps.

3.2 8051 Microprocessor

The 8051 microprocessor embedded in the FX2 family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

If Autovectoring is enabled (AV2EN = 1 in the INTSETUP register), the FX2 substitutes its INT2VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0044, the automatically-inserted INT2VEC byte at 0x0045 will direct the jump to the correct address out of the 27 addresses within the page.

3.8.3 FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB-interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, like the USB Interrupt, can employ autovectoring. *Table 3-4* shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources

Table 3-4. Individual FIFO/GPIF Interrupt Sources

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 Programmable Flag
2	84	EP4PF	Endpoint 4 Programmable Flag
3	88	EP6PF	Endpoint 6 Programmable Flag
4	8C	EP8PF	Endpoint 8 Programmable Flag
5	90	EP2EF	Endpoint 2 Empty Flag
6	94	EP4EF	Endpoint 4 Empty Flag
7	98	EP6EF	Endpoint 6 Empty Flag
8	9C	EP8EF	Endpoint 8 Empty Flag
9	A0	EP2FF	Endpoint 2 Full Flag
10	A4	EP4FF	Endpoint 4 Full Flag
11	A8	EP6FF	Endpoint 6 Full Flag
12	AC	EP8FF	Endpoint 8 Full Flag
13	B0	GPIFDONE	GPIF Operation Complete
14	B4	GPIFWF	GPIF Waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSETUP register), the FX2 substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically-inserted INT4VEC byte at 0x0055 will direct the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2 pushes the program counter onto its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the ISR Interrupt service routine.

3.9 Reset and Wakeup

3.9.1 Reset Pin

An input pin (RESET#) resets the chip. This pin has hysteresis and is active LOW. The internal PLL stabilizes approximately 200 µs after V_{CC} has reached 3.3V. Typically, an external RC network (R = 100k, C = 0.1 µF) is used to provide the RESET# signal.

3.9.2 Wakeup Pins

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts and after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies whether or not FX2 is connected to the USB.

The FX2 exits the power down (USB suspend) state using one of the following methods:

- USB bus signals resume
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin.

The second wakeup pin, WU2, can also be configured as a general purpose I/O pin. This allows a simple external R-C network to be used as a periodic wakeup source.

3.10 Program/Data RAM

3.10.1 Size

The FX2 has eight kbytes of internal program/data RAM, where PSEN#/RD# signals are internally ORed to allow the 8051 to access it as both program and data memory. No USB control registers appear in this space.

Two memory maps are shown in the following diagrams:

Figure 3-1 Internal Code Memory, EA = 0

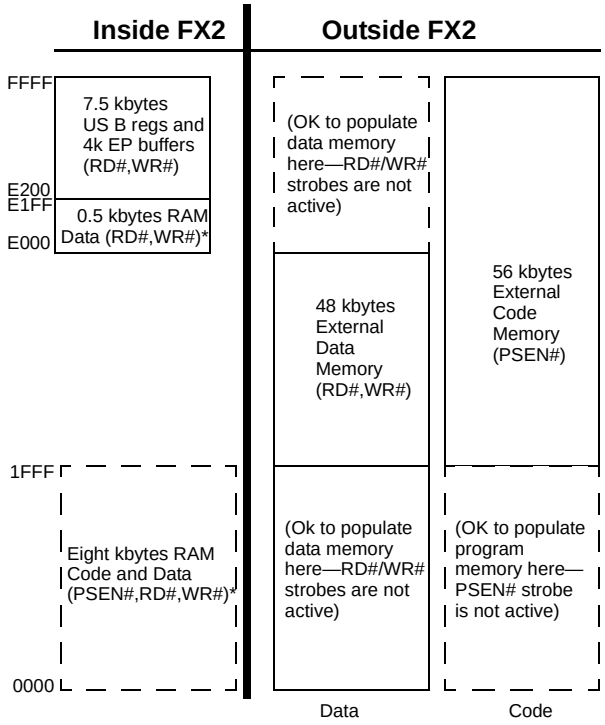
Figure 3-2 External Code Memory, EA = 1.

3.10.2 Internal Code Memory, EA = 0

This mode implements the internal eight-kbyte block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This allows the user to connect a 64-kbyte memory without requiring address decodes to keep clear of internal memory spaces.

Only the **internal** eight kbytes and **scratch pad** 0.5 kbytes RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I^2C-compatible interface boot load.

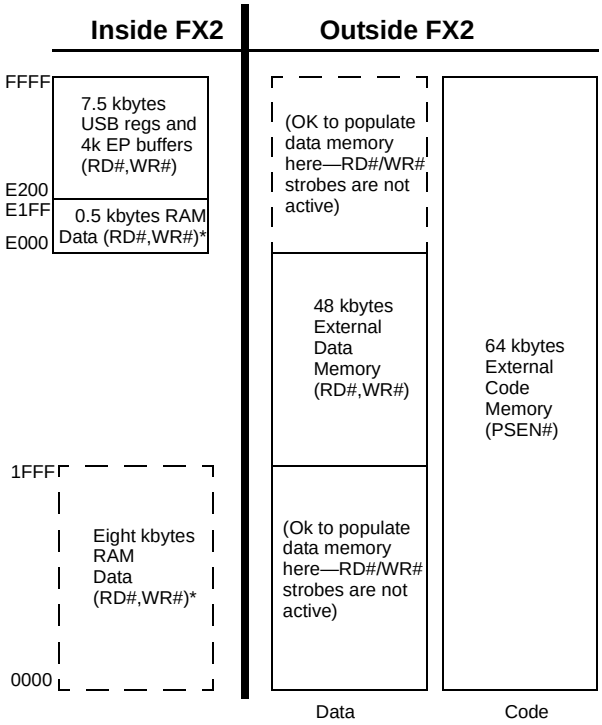


*SUDPTR, USB upload/download, I^2C-compatible interface boot access

Figure 3-1. Internal Code Memory, EA = 0

3.10.3 External Code Memory, EA = 1

The bottom eight kbytes of program memory is external, and therefore the bottom eight kbytes of internal RAM is accessible only as data memory.



*SUDPTR, USB upload/download, I^2C-compatible interface boot access

Figure 3-2. External Code Memory, EA = 1

3.12.4 Endpoint Configurations (High-speed Mode)

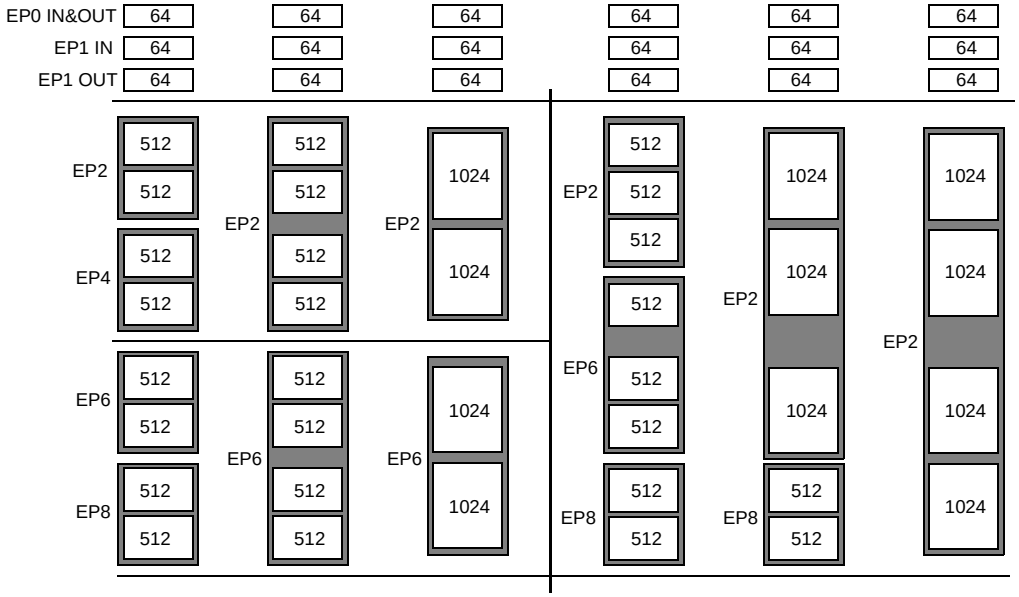


Figure 3-3. Endpoint Configuration

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT. To the left of the vertical line, the user may pick different configurations for EP2&4 and EP6&8, since none of the 512-byte buffers are combined between these endpoint groups. An example endpoint configuration would be:

EP2—1024 double buffered; EP6—512 quad buffered.

To the right of the vertical line, buffers are shared between EP2–8, and therefore only entire columns may be chosen.

3.12.5 Default Full-Speed Alternate Settings

Table 3-5. Default Full-Speed Alternate Settings[1, 2]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2×)	64 int out (2×)	64 iso out (2×)
ep4	0	64 bulk out (2×)	64 bulk out (2×)	64 bulk out (2×)
ep6	0	64 bulk in (2×)	64 int in (2×)	64 iso in (2×)
ep8	0	64 bulk in (2×)	64 bulk in (2×)	64 bulk in (2×)

Notes:
1. “0” means “not implemented.”
2. “2x” means “double buffered.”

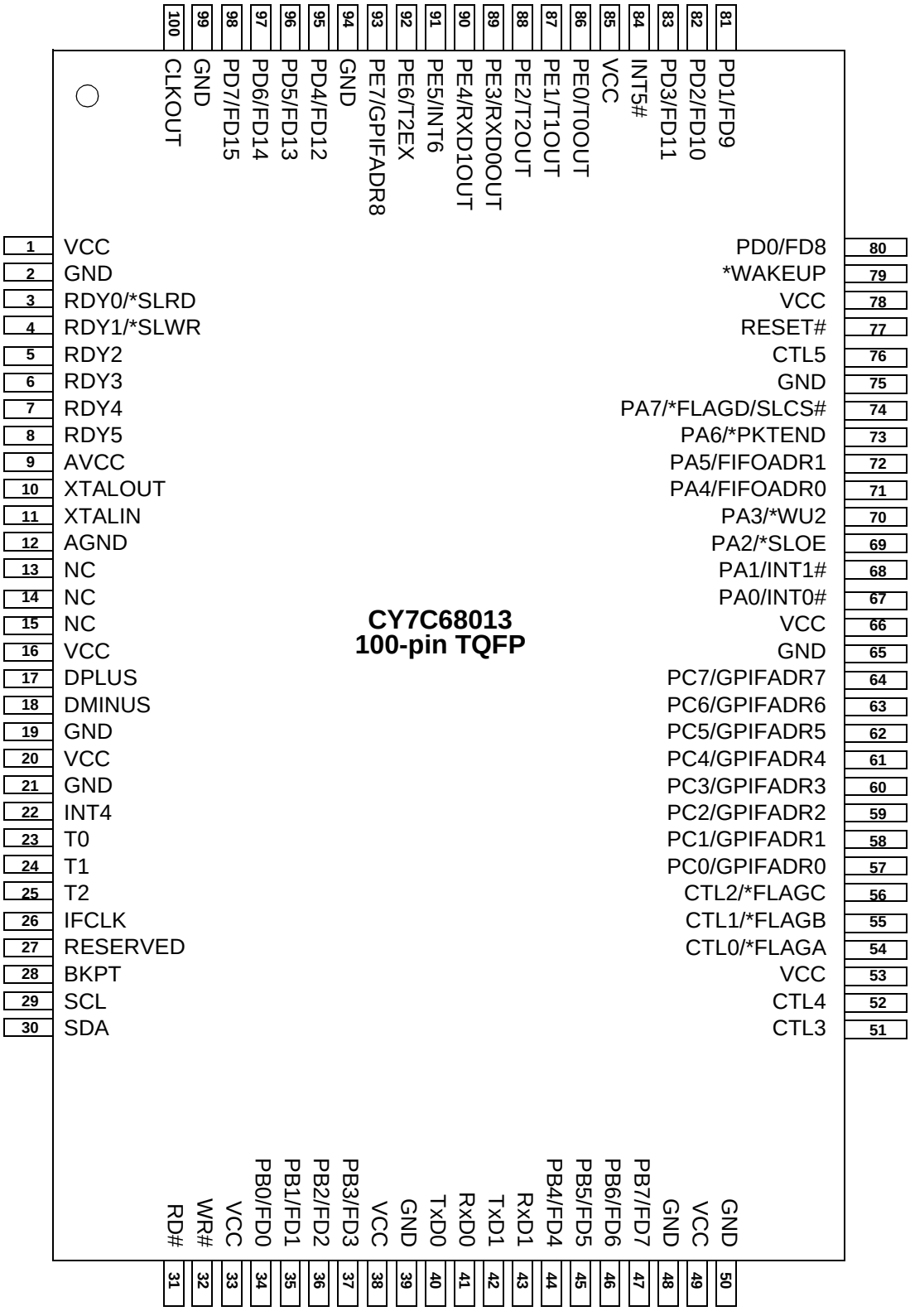


Figure 4-3. CY7C68013 100-pin TQFP Pin Assignment

* denotes programmable polarity

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
92	74	47	40	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. **PA7** is a bidirectional I/O port pin. **FLAGD** is a programmable slave-FIFO output status flag signal. **SLCS#** gates all other slave FIFO enable/strobes
Port B							
44	34	25	18	PB0 or FD[0]	I/O/Z	I (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **FD[0]** is the bidirectional FIFO/GPIF data bus.
45	35	26	19	PB1 or FD[1]	I/O/Z	I (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **FD[1]** is the bidirectional FIFO/GPIF data bus.
46	36	27	20	PB2 or FD[2]	I/O/Z	I (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **FD[2]** is the bidirectional FIFO/GPIF data bus.
47	37	28	21	PB3 or TXD1 or FD[3]	I/O/Z	I (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **FD[3]** is the bidirectional FIFO/GPIF data bus.
54	44	29	22	PB4 or FD[4]	I/O/Z	I (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **FD[4]** is the bidirectional FIFO/GPIF data bus.
55	45	30	23	PB5 or FD[5]	I/O/Z	I (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **FD[5]** is the bidirectional FIFO/GPIF data bus.
56	46	31	24	PB6 or FD[6]	I/O/Z	I (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **FD[6]** is the bidirectional FIFO/GPIF data bus.
57	47	32	25	PB7 or FD[7]	I/O/Z	I (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **FD[7]** is the bidirectional FIFO/GPIF data bus.
PORT C							
72	57			PC0 or GPIFADR0	I/O/Z	I (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 **PC0** is a bidirectional I/O port pin. **GPIFADR0** is a GPIF address output pin.
73	58			PC1 or GPIFADR1	I/O/Z	I (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 **PC1** is a bidirectional I/O port pin. **GPIFADR1** is a GPIF address output pin.
74	59			PC2 or GPIFADR2	I/O/Z	I (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 **PC2** is a bidirectional I/O port pin. **GPIFADR2** is a GPIF address output pin.
75	60			PC3 or GPIFADR3	I/O/Z	I (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 **PC3** is a bidirectional I/O port pin. **GPIFADR3** is a GPIF address output pin.
76	61			PC4 or GPIFADR4	I/O/Z	I (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 **PC4** is a bidirectional I/O port pin. **GPIFADR4** is a GPIF address output pin.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
77	62			PC5 or GPIFADR5	I/O/Z	I (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 **PC5** is a bidirectional I/O port pin. **GPIFADR5** is a GPIF address output pin.
78	63			PC6 or GPIFADR6	I/O/Z	I (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 **PC6** is a bidirectional I/O port pin. **GPIFADR6** is a GPIF address output pin.
79	64			PC7 or GPIFADR7	I/O/Z	I (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 **PC7** is a bidirectional I/O port pin. **GPIFADR7** is a GPIF address output pin.
PORT D							
102	80	52	45	PD0 or FD[8]	I/O/Z	I (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	46	PD1 or FD[9]	I/O/Z	I (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	47	PD2 or FD[10]	I/O/Z	I (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	48	PD3 or FD[11]	I/O/Z	I (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	49	PD4 or FD[12]	I/O/Z	I (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	50	PD5 or FD[13]	I/O/Z	I (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	51	PD6 or FD[14]	I/O/Z	I (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	52	PD7 or FD[15]	I/O/Z	I (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E							
108	86			PE0 or T0OUT	I/O/Z	I (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87			PE1 or T1OUT	I/O/Z	I (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
110	88			PE2 or T2OUT	I/O/Z	I (PE2)	Multiplexed pin whose function is selected by the PORTECFG.2 bit. **PE2** is a bidirectional I/O port pin. **T2OUT** is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.
111	89			PE3 or RXD0OUT	I/O/Z	I (PE3)	Multiplexed pin whose function is selected by the PORTECFG.3 bit. **PE3** is a bidirectional I/O port pin. **RXD0OUT** is an active-HIGH signal from 8051 UART0. If RXD0OUT is selected and UART0 is in Mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
112	90			PE4 or RXD1OUT	I/O/Z	I (PE4)	Multiplexed pin whose function is selected by the PORTECFG.4 bit. **PE4** is a bidirectional I/O port pin. **RXD1OUT** is an active-HIGH output from 8051 UART1. When RXD1OUT is selected and UART1 is in Mode 0, this pin provides the output data for UART1 only when it is in sync mode. In Modes 1, 2, and 3, this pin is HIGH.
113	91			PE5 or INT6	I/O/Z	I (PE5)	Multiplexed pin whose function is selected by the PORTECFG.5 bit. **PE5** is a bidirectional I/O port pin. **INT6** is the 8051 INT5 interrupt request input signal. The INT6 pin is edge-sensitive, active HIGH.
114	92			PE6 or T2EX	I/O/Z	I (PE6)	Multiplexed pin whose function is selected by the PORTECFG.6 bit. **PE6** is a bidirectional I/O port pin. **T2EX** is an active-high input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
115	93			PE7 or GPIFADR8	I/O/Z	I (PE7)	Multiplexed pin whose function is selected by the PORTECFG.7 bit. **PE7** is a bidirectional I/O port pin. **GPIFADR8** is a GPIF address output pin.
4	3	8	1	RDY0 or SLRD	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY0** is a GPIF input signal. **SLRD** is the input-only read strobe with programmable polarity (FIFOPOLAR.3) for the slave FIFOs connected to FDI[7..0] or FDI[15..0].
5	4	9	2	RDY1 or SLWR	Input	N/A	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **RDY1** is a GPIF input signal. **SLWR** is the input-only write strobe with programmable polarity (FIFOPOLAR.2) for the slave FIFOs connected to FDI[7..0] or FDI[15..0].
6	5			RDY2	Input	N/A	**RDY2** is a GPIF input signal.
7	6			RDY3	Input	N/A	**RDY3** is a GPIF input signal.
8	7			RDY4	Input	N/A	**RDY4** is a GPIF input signal.
9	8			RDY5	Input	N/A	**RDY5** is a GPIF input signal.

Table 4-1. FX2 Pin Descriptions (continued)[5]

128 TQFP	100 TQFP	56 SSOP	56 QFN	Name	Type	Default	Description
40	31			RD#	Output	H	**RD#** is the active-LOW read strobe output for external memory.
38				OE#	Output	H	**OE#** is the active-LOW output enable for external memory.
33	27	21	14	Reserved	Input	N/A	Reserved. Connect to ground.
101	79	51	44	WAKEUP	Input	N/A	**USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to allow it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB® chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	SCL	OD	Z	**Clock** for the **I^2C-compatible interface.** Connect to V_{CC} with a 2.2K resistor, **even if no I^2C-compatible peripheral is attached**.
37	30	23	16	SDA	OD	Z	**Data** for **I^2C-compatible interface**. Connect to V_{CC} with a 2.2K resistor, **even if no I^2C-compatible peripheral is attached**.
2	1	6	55	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
17	16	14	7	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
26	20	18	11	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
43	33	24	17	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
48	38	34	27	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
64	49	39	32	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
68	53	50	43	V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
81	66			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
100	78			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
107	85			V_{CC}	Power	N/A	V_{CC}. Connect to 3.3V power source.
3	2	4	53	GND	Ground	N/A	Ground.
20	19	7	56	GND	Ground	N/A	Ground.
27	21	17	10	GND	Ground	N/A	Ground.
49	39	19	12	GND	Ground	N/A	Ground.
58	48	33	26	GND	Ground	N/A	Ground.
65	50	35	28	GND	Ground	N/A	Ground.
80	65	48	41	GND	Ground	N/A	Ground.
93	75			GND	Ground	N/A	Ground.
116	94			GND	Ground	N/A	Ground.
125	99			GND	Ground	N/A	Ground.
14	13			NC	N/A	N/A	No-connect. This pin must be left open.
15	14			NC	N/A	N/A	No-connect. This pin must be left open.
16	15			NC	N/A	N/A	No-connect. This pin must be left open.

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E631 F.S	1	EP2FIFOPFL[6]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632 H.S.	1	EP4FIFOPFH[6]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E632 F.S	1	EP4FIFOPFH[6]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E633 H.S.	1	EP4FIFOPFL[6]	Endpoint 4 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E633 F.S	1	EP4FIFOPFL[6]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634 H.S.	1	EP6FIFOPFH[6]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb
E634 F.S	1	EP6FIFOPFH[6]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb
E635 H.S.	1	EP6FIFOPFL[6]	Endpoint 6 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E635 F.S	1	EP6FIFOPFL[6]	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636 H.S.	1	EP8FIFOPFH[6]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E636 F.S	1	EP8FIFOPFH[6]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E637 H.S.	1	EP8FIFOPFL[6]	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E637 F.S	1	EP8FIFOPFL[6]	Endpoint 8 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	reserved											
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	0	0	0	0	0	0	INPPF1	INPPF0	00000001	rrrrrrbb
	4	reserved											
E648	1	INPKTEND[6]	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	R/W
E649	7	OUTPKTEND[6]	Force OUT Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
		INTERRUPTS											
E650	1	EP2FIFOIE[6]	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E651	1	EP2FIFOIRQ[6]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E652	1	EP4FIFOIE[6]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ[6]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E654	1	EP6FIFOIE[6]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ[6]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E656	1	EP8FIFOIE[6]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ[6]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000xxx	RW
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxxx	RW
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	NAKIRQ	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	xxxxxxxx	RW
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW
E65D	1	USBIRQ	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	RW
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	xxxxxxxx	RW
E660	1	GPIFIE[6]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ[6]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	xxxx000x	RW
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSETUP	Interrupt 2&4 Setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E669	7	reserved											
		INPUT / OUTPUT											
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW
E673	5	reserved											
E678	1	I2CS	I²C-Compatible Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr
E679	1	I2DAT	I²C-Compatible Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW
E67A	1	I2CTL	I²C-Compatible Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW
E67B	1	XAUTODAT1	Autoptr1 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67C	1	XAUTODAT2	Autoptr2 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
		UDMA CRC											
E67D	1	UDMACRCH[6]	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW
E67E	1	UDMACRCL[6]	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNAL2	QSIGNAL1	QSIGNAL0	00000000	brrrbbbb
		USB CONTROL											
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DISCON	NOSYNSOF	RENUM	SIGRSUME	x0000000	rrrrbbbb
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrbbb
E683	1	TOGCTL	Toggle Control	Q	S	R	IO	EP3	EP2	EP1	EP0	xxxxxxxx	rbbbbbbb
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	00000xxx	R
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxxx	R
E688	2	reserved											
		ENDPOINTS											
E68A	1	EP0BCH[6]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW
E68B	1	EP0BCL[6]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E690	1	EP2BCH[6]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E691	1	EP2BCL[6]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH[6]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW
E695	1	EP4BCL[6]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH[6]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E699	1	EP6BCL[6]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH[6]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW
E69D	1	EP8BCL[6]	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69E	2	reserved											
E6A0	1	EP0CS	Endpoint 0 Control and Status	HSNAK	0	0	0	0	0	BUSY	STALL	10000000	bbbbbbrb
E6A1	1	EP1OUTCS	Endpoint 1 OUT Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb
E6A2	1	EP1INCS	Endpoint 1 IN Control and Status	0	0	0	0	0	0	BUSY	STALL	00000000	bbbbbbrb
E6A3	1	EP2CS	Endpoint 2 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb
E6A4	1	EP4CS	Endpoint 4 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00101000	rrrrrrrb
E6A5	1	EP6CS	Endpoint 6 Control and Status	0	NPAK2	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb
E6A6	1	EP8CS	Endpoint 8 Control and Status	0	0	NPAK1	NPAK0	FULL	EMPTY	0	STALL	00000100	rrrrrrrb
E6A7	1	EP2FIFOFLGS	Endpoint 2 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R
E6A8	1	EP4FIFOFLGS	Endpoint 4 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000010	R
E6A9	1	EP6FIFOFLGS	Endpoint 6 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AA	1	EP8FIFOFLGS	Endpoint 8 slave FIFO Flags	0	0	0	0	0	PF	EF	FF	00000110	R
E6AB	1	EP2FIFOBCH	Endpoint 2 slave FIFO total byte count H	0	0	0	BC12	BC11	BC10	BC9	BC8	00000000	R

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6AC	1	EP2FIFOBCL	Endpoint 2 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AD	1	EP4FIFOBCH	Endpoint 4 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R
E6AE	1	EP4FIFOBCL	Endpoint 4 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6AF	1	EP6FIFOBCH	Endpoint 6 slave FIFO total byte count H	0	0	0	0	BC11	BC10	BC9	BC8	00000000	R
E6B0	1	EP6FIFOBCL	Endpoint 6 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B1	1	EP8FIFOBCH	Endpoint 8 slave FIFO total byte count H	0	0	0	0	0	BC10	BC9	BC8	00000000	R
E6B2	1	EP8FIFOBCL	Endpoint 8 slave FIFO total byte count L	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0	00000000	R
E6B3	1	SUDPTRH	Setup Data Pointer high address byte	A15	A14	A13	A12	A11	A10	A9	A8	xxxxxxxx	RW
E6B4	1	SUDPTRL	Setup Data Pointer low address byte	A7	A6	A5	A4	A3	A2	A1	0	xxxxxxx0	bbbbbbbr
E6B5	1	SUDPTRCTL	Setup Data Pointer Auto Mode	0	0	0	0	0	0	0	SDPAUTO	00000001	RW
	2	reserved											
E6B8	8	SETUPDAT	8 bytes of SETUP data	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
			SETUPDAT[0] = bmRequestType										
			SETUPDAT[1] = bmRequest										
			SETUPDAT[2:3] = wValue										
			SETUPDAT[4:5] = wIndex										
			SETUPDAT[6:7] = wLength										
		GPIF											
E6C0	1	GPIFWFSELECT	Waveform Selector	SINGLEWR1	SINGLEWR0	SINGLERD1	SINGLERD0	FIFOWR1	FIFOWR0	FIFORD1	FIFORD0	11100100	RW
E6C1	1	GPIFIDLECS	GPIF Done, GPIF IDLE drive mode	DONE	0	0	0	0	0	0	IDLEDRV	10000000	RW
E6C2	1	GPIFIDLECTL	Inactive Bus, CTL states	0	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	11111111	RW
E6C3	1	GPIFCTLCFG	CTL Drive Type	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C4	1	GPIFADRH[6]	GPIF Address H	0	0	0	0	0	0	0	GPIFA8	00000000	RW
E6C5	1	GPIFADRL[6]	GPIF Address L	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
		FLOWSTATE											
E6C6	1	FLOWSTATE	Flowstate Enable and Selector	FSE	0	0	0	0	FS2	FS1	FS0	00000000	brrrrbbb
E6C7	1	FLOWLOGIC	Flowstate Logic	LFUNC1	LFUNC0	TERMA2	TERMA1	TERMA0	TERMB2	TERMB1	TERMB0	00000000	RW
E6C8	1	FLOWEQ0CTL	CTL-Pin States in Flowstate (when Logic = 0)	CTL0E3	CTL0E2	CTL0E1/ CTL5	CTL0E0/ CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6C9	1	FLOWEQ1CTL	CTL-Pin States in Flowstate (when Logic = 1)	CTL0E3	CTL0E2	CTL0E1/ CTL5	CTL0E0/ CTL4	CTL3	CTL2	CTL1	CTL0	00000000	RW
E6CA	1	FLOWHOLDOFF	Holdoff Configuration	HOPERIOD3	HOPERIOD2	HOPERIOD1	HOPERIOD0	HOSTATE	HOCTL2	HOCTL1	HOCTL0	00010010	RW
E6CB	1	FLOWSTB	Flowstate Strobe Configuration	SLAVE	RDYASYNC	CTLTOGL	SUSTAIN	0	MSTB2	MSTB1	MSTB0	00100000	RW
E6CC	1	FLOWSTBEDGE	Flowstate Rising/Falling Edge Configuration	0	0	0	0	0	0	FALLING	RISING	00000001	rrrrrrbb
E6CD	1	FLOWSTBPERIOD	Master-Strobe Half-Period	D7	D6	D5	D4	D3	D2	D1	D0	00000010	RW
E6CE	1	GPIFTCB3[6]	GPIF Transaction Count Byte 3	TC31	TC30	TC29	TC28	TC27	TC26	TC25	TC24	00000000	RW
E6CF	1	GPIFTCB2[6]	GPIF Transaction Count Byte 2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW
E6D0	1	GPIFTCB1[6]	GPIF Transaction Count Byte 1	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6D1	1	GPIFTCB0[6]	GPIF Transaction Count Byte 0	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000001	RW
	2	reserved										00000000	RW
		reserved											
		reserved											
E6D2	1	EP2GPIFFLGSEL[6]	Endpoint 2 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6D3	1	EP2GPIFPFSTOP	Endpoint 2 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO2FLAG	00000000	RW
E6D4	1	EP2GPIFTRIG[6]	Endpoint 2 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6DA	1	EP4GPIFFLGSEL[6]	Endpoint 4 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6DB	1	EP4GPIFPFSTOP	Endpoint 4 GPIF stop transaction on GPIF Flag	0	0	0	0	0	0	0	FIFO4FLAG	00000000	RW
E6DC	1	EP4GPIFTRIG[6]	Endpoint 4 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
		reserved											
		reserved											
E6E2	1	EP6GPIFFLGSEL[6]	Endpoint 6 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6E3	1	EP6GPIFPFSTOP	Endpoint 6 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO6FLAG	00000000	RW
E6E4	1	EP6GPIFTRIG[6]	Endpoint 6 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6EA	1	EP8GPIFFLGSEL[6]	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW
E6EC	1	EP8GPIFTRIG[6]	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxxx	W
	3	reserved											
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
E6F1	1	XGPIFSGLDATLX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E6F2	1	XGPIFSGLDATL-NOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
E6F3	1	GPIFREADYCFG	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbrrrrr
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxxx	R
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxxx	W
E6F6	2	reserved											
		ENDPOINT BUFFERS											
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
	2048	reserved											RW
F000	1024	EP2FIFOBUF	512/1024-byte EP 2 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F400	512	EP4FIFOBUF	512 byte EP 4 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
F600	512	reserved											
F800	1024	EP6FIFOBUF	512/1024-byte EP 6 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FC00	512	EP8FIFOBUF	512 byte EP 8 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
FE00	512	reserved											
xxxx		**I²C Compatible Configuration Byte**		0	DISCON	0	0	0	0	0	400KHZ	xxxxxxxx[8]	n/a
		Special Function Registers (SFRs)											
80	1	IOA[7]	Port A (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
81	1	SP	Stack Pointer	D7	D6	D5	D4	D3	D2	D1	D0	00000111	RW
82	1	DPL0	Data Pointer 0 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
83	1	DPH0	Data Pointer 0 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
84	1	DPL1[7]	Data Pointer 1 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
85	1	DPH1[7]	Data Pointer 1 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
86	1	DPS[7]	Data Pointer 0/1 select	0	0	0	0	0	0	0	SEL	00000000	RW
87	1	PCON	Power Control	SMOD0	x	1	1	GF1	GF0	STOP	IDLE	00110000	RW
88	1	TCON	Timer/Counter Control (bit addressable)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000	RW
89	1	TMOD	Timer/Counter Mode Control	GATE	CT	M1	M0	GATE	CT	M1	M0	00000000	RW
8A	1	TL0	Timer 0 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8B	1	TL1	Timer 1 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8C	1	TH0	Timer 0 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8D	1	TH1	Timer 1 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8E	1	CKCON[7]	Clock Control	x	x	T2M	T1M	T0M	MD2	MD1	MD0	00000001	RW
8F	1	reserved											
90	1	IOB[7]	Port B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
91	1	EXIF[7]	External Interrupt Flag(s)	IE5	IE4	I²CINT	USBNT	1	0	0	0	00001000	RW
92	1	MPAGE[7]	Upper Addr Byte of MOVX using @R0 / @R1	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
93	5	reserved											
98	1	SCON0	Serial Port 0 Control (bit addressable)	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00000000	RW
99	1	SBUF0	Serial Port 0 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW

Notes:

7. SFRs not part of the standard 8051 architecture.
8. If no EEPROM is detected by the SIE then the default is 00000000.

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

Table 5-1. FX2 Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
9A	1	AUTOPTRH1[7]	Autopointer 1 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9B	1	AUTOPTRL1[7]	Autopointer 1 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9C	1	reserved											
9D	1	AUTOPTRH2[7]	Autopointer 2 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9E	1	AUTOPTRL2[7]	Autopointer 2 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9F	1	reserved											
A0	1	IOC[7]	Port C (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
A1	1	INT2CLR[7]	Interrupt 2 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A2	1	INT4CLR[7]	Interrupt 4 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A3	5	reserved											
A8	1	IE	Interrupt Enable (bit addressable)	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00000000	RW
A9	1	reserved											
AA	1	EP2468STAT[7]	Endpoint 2,4,6,8 status flags	EP8F	EP8E	EP6F	EP6E	EP4F	EP4E	EP2F	EP2E	01011010	R
AB	1	EP24FIFOFLGS[7]	Endpoint 2,4 slave FIFO status flags	0	EP4PF	EP4EF	EP4FF	0	EP2PF	EP2EF	EP2FF	00100010	R
AC	1	EP68FIFOFLGS[7]	Endpoint 6,8 slave FIFO status flags	0	EP8PF	EP8EF	EP8FF	0	EP6PF	EP6EF	EP6FF	01100110	R
AD	2	reserved											
AF	1	AUTOPTRSETUP[7]	Autopointer 1&2 Setup	0	0	0	0	0	APTR2INC	APTR1INC	APTREN	00000110	RW
B0	1	IOD[7]	Port D (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B1	1	IOE[7]	Port E (NOT bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B2	1	OEA[7]	Port A Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B3	1	OEB[7]	Port B Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B4	1	OEC[7]	Port C Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B5	1	OED[7]	Port D Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B6	1	OEE[7]	Port E Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B7	1	reserved											
B8	1	IP	Interrupt Priority (bit addressable)	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	10000000	RW
B9	1	reserved											
BA	1	EP01STAT[7]	Endpoint 0&1 Status	0	0	0	0	0	EP1INBSY	EP1OUTBSY	EP0BSY	00000000	R
BB	1	GPIFTRIG[7] [6]	Endpoint 2,4,6,8 GPIF slave FIFO Trigger	DONE	0	0	0	0	RW	EP1	EP0	10000xxx	brrrrbbb
BC	1	reserved											
BD	1	GPIFSGLDATH[7]	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW
BE	1	GPIFSGLDATLX[7]	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
BF	1	GPIFSGLDATLNOX[7]	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
C0	1	SCON1[7]	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1[7]	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON[7]	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
E1	7	reserved											
E8	1	EIE[7]	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI²C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP[7]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI²C	PUSB	11100000	RW
F9	7	reserved											

9.3 Data Memory Read

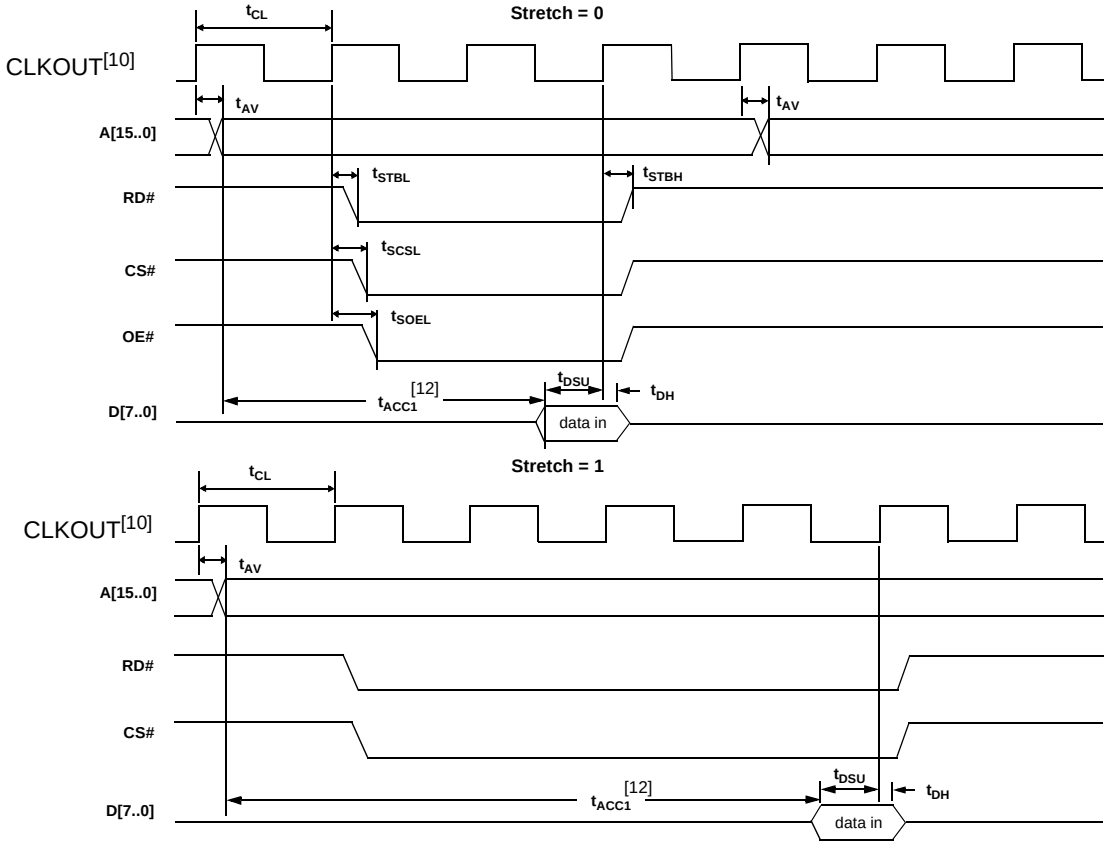


Figure 9-2. Data Memory Read Timing Diagram

Table 9-2. Data Memory Read Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		20.83		ns	48 MHz
			41.66		ns	24 MHz
			83.2		ns	12 MHz
t_{AV}	Delay from Clock to Valid Address			10.7	ns	
t_{STBL}	Clock to RD LOW			11	ns	
t_{STBH}	Clock to RD HIGH			11	ns	
t_{SCSL}	Clock to CS LOW			13	ns	
t_{SOEL}	Clock to OE LOW			11.1	ns	
t_{DSU}	Data Set-up to Clock	9.6			ns	
t_{DH}	Data Hold Time	0			ns	

Note:

12. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:
$t_{ACC2}(24\ MHz) = 3*t_{CL} - t_{AV} - t_{DSU} = 106$ ns
$t_{ACC2}(48\ MHz) = 3*t_{CL} - t_{AV} - t_{DSU} = 43$ ns

$t_{ACC3}(24\ MHz) = 5*t_{CL} - t_{AV} - t_{DSU} = 190$ ns
$t_{ACC3}(48\ MHz) = 5*t_{CL} - t_{AV} - t_{DSU} = 86$ ns.

9.5 GPIF Synchronous Signals

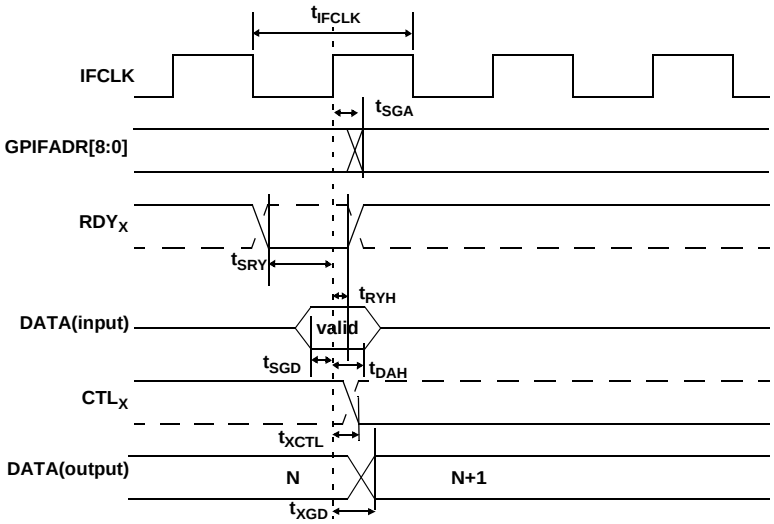


Figure 9-4. GPIF Synchronous Signals Timing Diagram[13]

Table 9-4. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK[14, 15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83		ns
t_{SRY}	RDY_X to Clock Set-up Time	8.9		ns
t_{RYH}	Clock to RDY_X	0		ns
t_{SGD}	GPIF Data to Clock Set-up Time	9.2		ns
t_{DAH}	GPIF Data Hold Time	0		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		7.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		11	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		6.7	ns

Table 9-5. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK[15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SRY}	RDY_X to Clock Set-up Time	2.9		ns
t_{RYH}	Clock to RDY_X	3.7		ns
t_{SGD}	GPIF Data to Clock Set-up Time	3.2		ns
t_{DAH}	GPIF Data Hold Time	4.5		ns
t_{SGA}	Clock to GPIF Address Propagation Delay		11.5	ns
t_{XGD}	Clock to GPIF Data Output Propagation Delay		15	ns
t_{XCTL}	Clock to CTL_X Output Propagation Delay		10.7	ns

Notes:
13. Dashed lines denote signals with programmable polarity
14. GPIF asynchronous RDY_x signals have a minimum set-up time of 50 ns when using internal 48-MHz IFCLK.
15. IFCLK must not exceed 48 MHz.

Table 9-16. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min.	Max.	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS Output Propagation Delay		10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA Output Propagation Delay		14.3	ns

9.14 Slave FIFO Synchronous Address

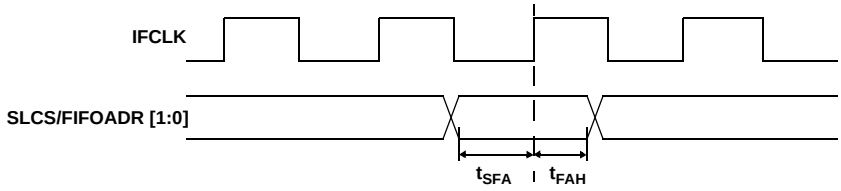


Figure 9-13. Slave FIFO Synchronous Address Timing Diagram

Table 9-17. Slave FIFO Synchronous Address Parameters [15]

Parameter	Description	Min.	Max.	Unit
t_{IFCLK}	Interface Clock Period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to Clock Set-up Time	25		ns
t_{FAH}	Clock to FIFOADR[1:0] Hold Time	10		ns

9.15 Slave FIFO Asynchronous Address

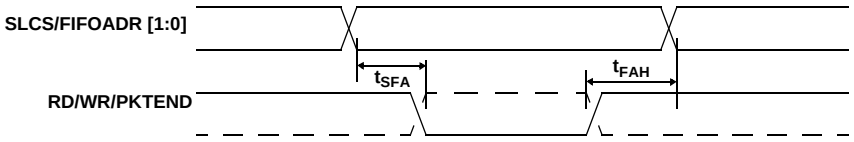


Figure 9-14. Slave FIFO Asynchronous Address Timing Diagram[13]

Table 9-18. Slave FIFO Asynchronous Address Parameters[16]

Parameter	Description	Min.	Max.	Unit
t_{SFA}	FIFOADR[1:0] to RD/WR/PKTEND Set-up Time	10		ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] Hold Time	10		ns

10.0 Ordering Information

Table 10-1. Ordering Information

Ordering Code	Package Type	RAM Size	# Prog I/Os	8051 Address /Data Busses
CY7C68013-128AC	128 TQFP	8K	40	16/8 bit
CY7C68013-100AC	100 TQFP	8K	40	–
CY7C68013-56PVC	56 SSOP	8K	24	–
CY7C68013-56LFC	56 QFN	8K	24	–
CY3681	EZ-USB FX2 Xcelerator Development Kit			

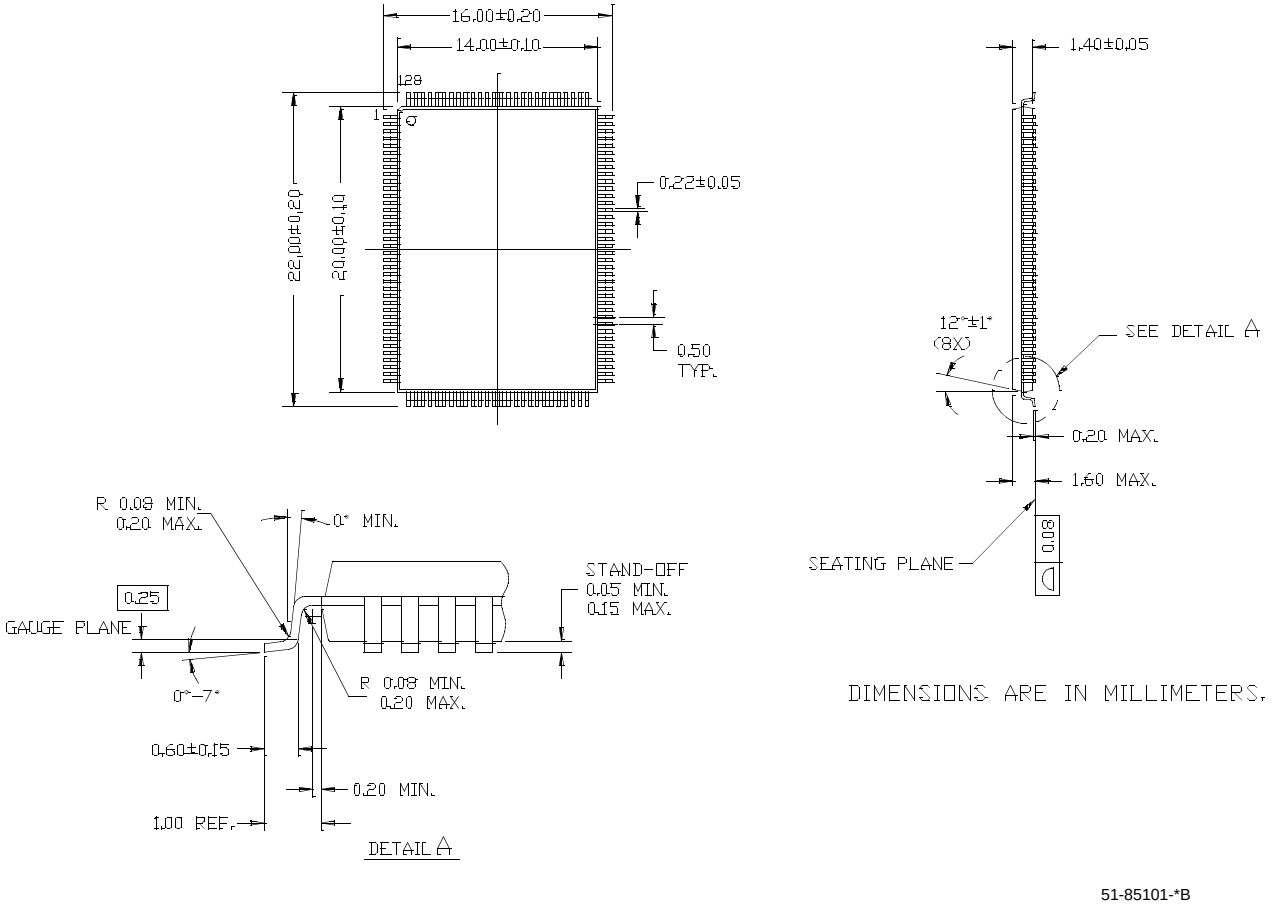


Figure 11-4. 128-Lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128

Document History Page

Document Title: CY7C68013 EZ-USB FX2™ USB Microcontroller High-speed USB Peripheral Controller Document Number: 38-08012				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111753	11/15/01	DSG	Change from Spec number: 38-00929 to 38-08012
*A	111802	02/20/02	KKU	Update functional changes between revision D part and revision E part. Changed timing data from simulation data to revision E characterization data.
*B	115480	06/26/02	KKU	Added new 56-pin Quad Flatpack No Lead package and pinout. Revised pin description table to reflect new package. Corrected *Figure 9-8* by moving tsfd parameter location. Corrected labels on Dplus and Dminus in *Table 4-1*. Removed Preliminary from spec title.
*C	120776	01/06/03	KKU	Added bus powered references and PCB layout recommendations and QFN package design notes. Updated QFN package drawing 51-85144 to current revision.