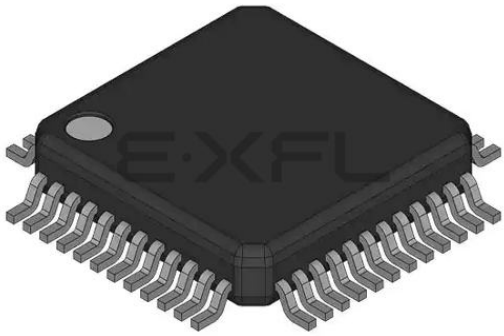

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf164kpmc-g-jne2

VBAT
The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

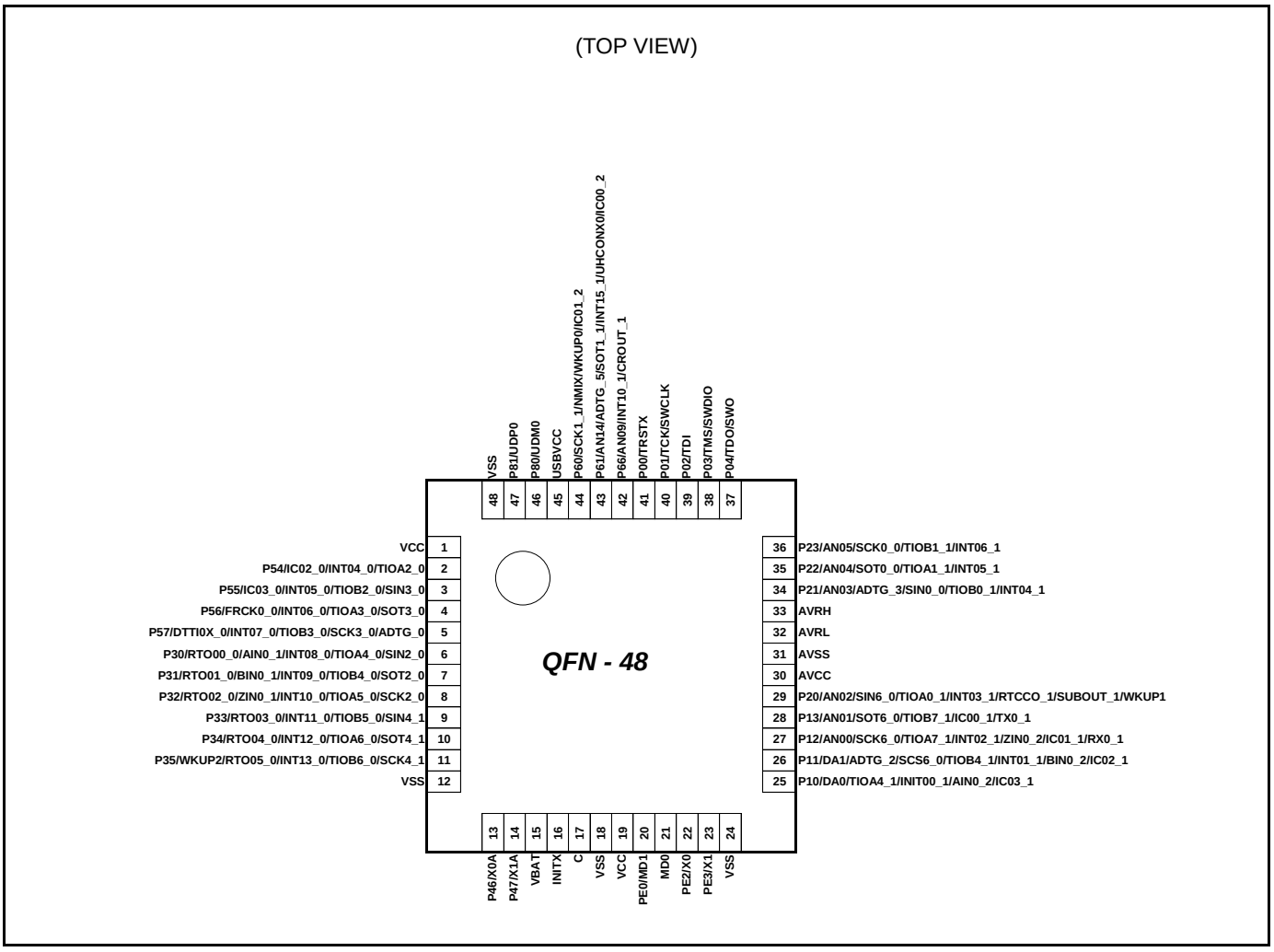
- Serial Wire JTAG Debug Port (SWJ-DP)

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Two Power Supplies

- Wide range voltage: VCC = 2.7 V to 5.5 V
- Power supply for VBAT: VBAT = 2.7 V to 5.5 V

LCC-48P-M73

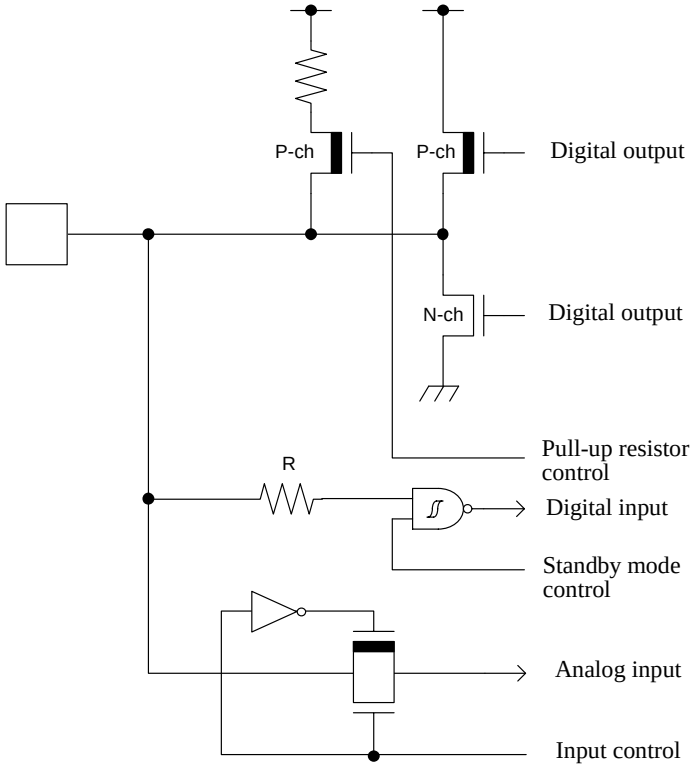
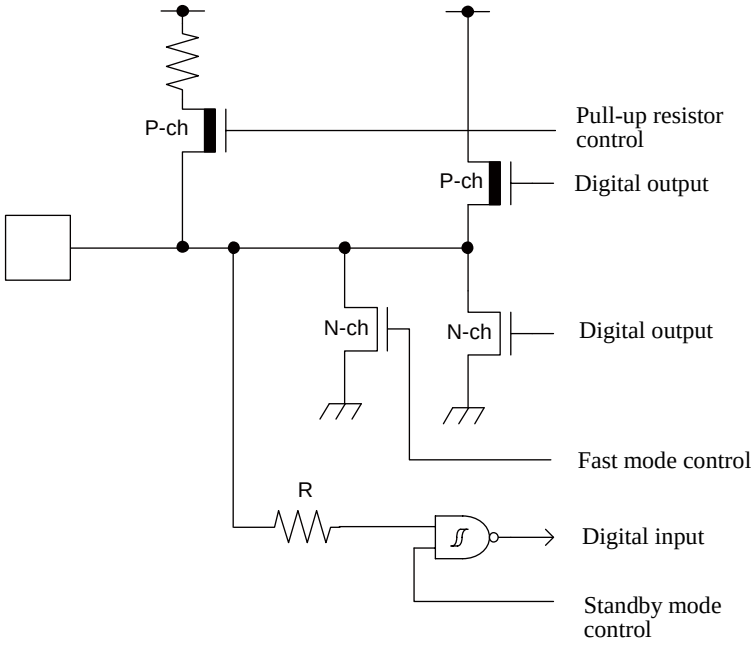


Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin No		Pin Name	I/O circuit type	Pin state type
LQFP64 QFN64	LQFP48 QFN48			
9	5	P57	N	K
		DTTI0X_0		
		INT07_0		
		TIOB3_0		
		SCK3_0 (SCL3_0)		
		ADTG_0		
10	6	P30	G	K
		RTO00_0		
		AIN0_1		
		INT08_0		
		TIOA4_0		
		SIN2_0		
11	7	P31	G	K
		RTO01_0		
		BIN0_1		
		INT09_0		
		TIOB4_0		
		SOT2_0 (SDA2_0)		
12	8	P32	G	K
		RTO02_0		
		ZIN0_1		
		INT10_0		
		TIOA5_0		
		SCK2_0 (SCL2_0)		
13	9	P33	G	K
		RTO03_0		
		INT11_0		
		TIOB5_0		
		SIN4_1		
14	10	P34	G	K
		RTO04_0		
		INT12_0		
		TIOA6_0		
		SOT4_1 (SDA4_1)		
15	11	P35	G	Q
		WKUP2		
		RTO05_0		
		INT13_0		
		TIOB6_0		
		SCK4_1 (SCL4_1)		

Pin function	Pin name	Function description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
External Interrupt	INT06_0	External interrupt request 06 input pin	8	4
	INT06_1		45	36
	INT07_0	External interrupt request 07 input pin	9	5
	INT07_1		46	-
	INT08_0	External interrupt request 08 input pin	10	6
	INT08_1		47	-
	INT09_0	External interrupt request 09 input pin	11	7
	INT09_1		48	-
	INT10_0	External interrupt request 10 input pin	12	8
	INT10_1		54	42
	INT11_0	External interrupt request 11 input pin	13	9
	INT11_1		55	-
	INT12_0	External interrupt request 12 input pin	14	10
	INT12_1		56	-
	INT13_0	External interrupt request 13 input pin	15	11
	INT13_1		57	-
	INT14_0	External interrupt request 14 input pin	26	-
	INT14_1		58	-
	INT15_0	External interrupt request 15 input pin	27	-
	INT15_1		59	43
	NMIX	Non-Maskable Interrupt input pin	60	44
GPIO	P00	General-purpose I/O port 0	53	41
	P01		52	40
	P02		51	39
	P03		50	38
	P04		49	37
	P10	General-purpose I/O port 1	34	25
	P11		35	26
	P12		36	27
	P13		37	28
	P20	General-purpose I/O port 2	38	29
	P21		43	34
	P22		44	35
	P23		45	36
	P24		46	-
	P25		47	-
	P26		48	-
	P30	General-purpose I/O port 3	10	6
	P31		11	7
	P32		12	8
	P33		13	9
	P34		14	10
	P35		15	11

Type	Circuit	Remarks
M		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
N		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) • I_{OL} = 20 mA (Fast Mode Plus) • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at "0" Hi-Z / Input enabled	Hi-Z / Internal input fixed at "0" Hi-Z / Input enabled	GPIO selected

*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Maintain previous state at timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7	5.5	V	
Power supply voltage (VBAT)		V_{BAT}	-	2.7	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC}=V_{CC}
Analog reference voltage		AVRH	-	*1	AV_{CC}	V	
Operating temperature	Junction temperature	Tj	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	- 40	*2	°C	

*1: The minimum value of Analog reference voltage depends on the value of compare clock cycle (Tcck).
See "5. 12-bit A/D Converter" for the details.

*2: The maximum temperature of the ambient temperature (Ta) can guarantee a range that does not exceed the junction temperature (Tj).
The calculation formula of the ambient temperature (Ta) is shown below.

$T_A(Max) = Tj(Max) - Pd(Max) \times \theta ja$

Pd: Power dissipation (W)
θja: Package thermal resistance (°C/W)

$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

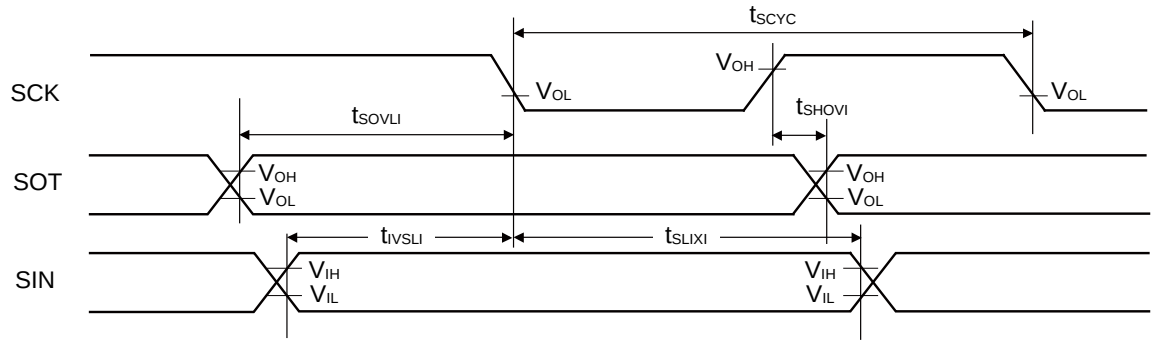
Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

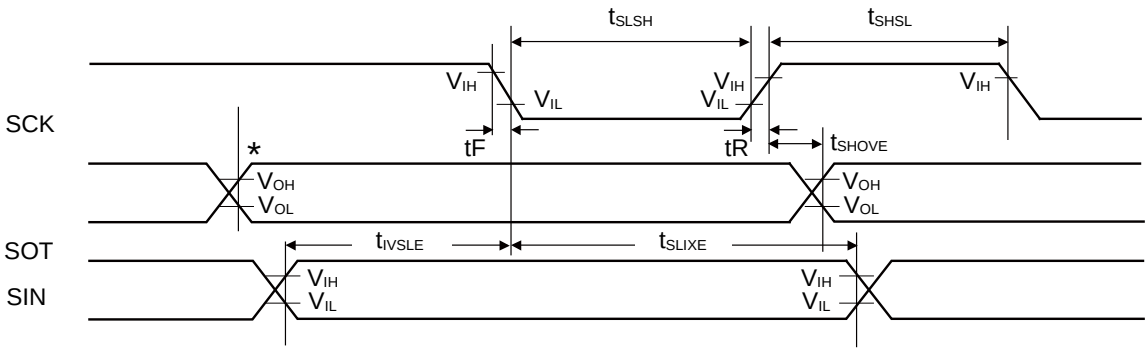
Package	Printed circuit board	Thermal resistance θja (°C/W)	Maximum permissible power (mW)	
			T_A=+85°C	T_A=+105°C
FPT-48P-M49 (0.5mm pitch)	Single-layered both sides	87	460	230
	4 layers	53	755	377
LCC-48P-M73 (0.5mm pitch)	Single-layered both sides	30	1333	667
	4 layers	24	1667	833
FPT-64P-M38 (0.5mm pitch)	Single-layered both sides	70	571	286
	4 layers	45	889	444
FPT-64P-M39 (0.65mm pitch)	Single-layered both sides	61	656	328
	4 layers	40	1000	500
LCC-64P-M24 (0.5mm pitch)	Single-layered both sides	24	1667	833
	4 layers	21	1905	952

WARNING:

1. *The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
   Any use of semiconductor devices will be under their recommended operating condition.
   Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
   No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

High-speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

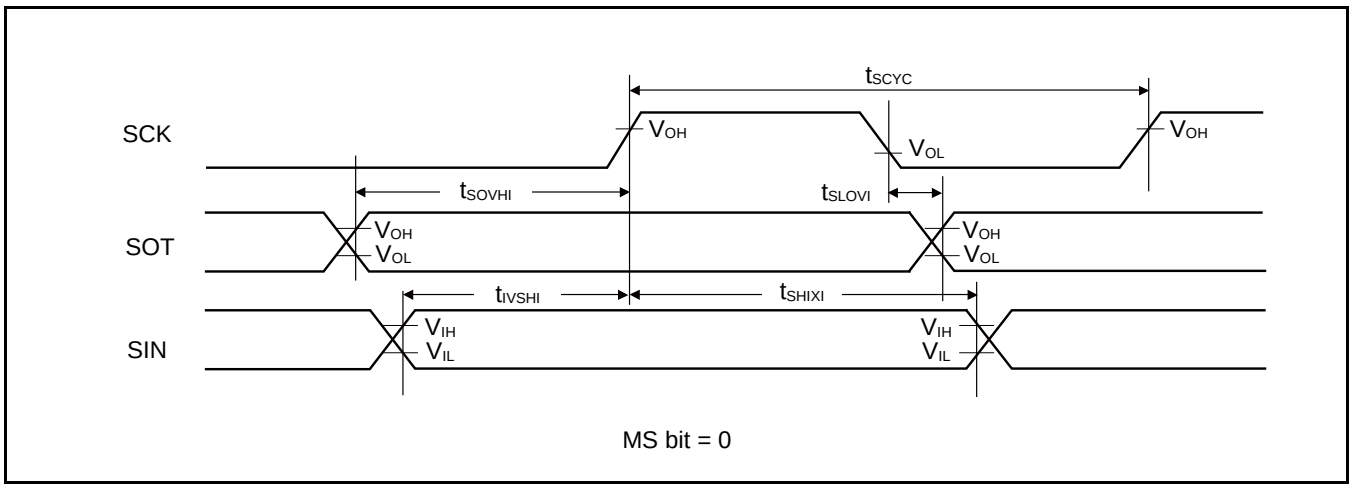
High-speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

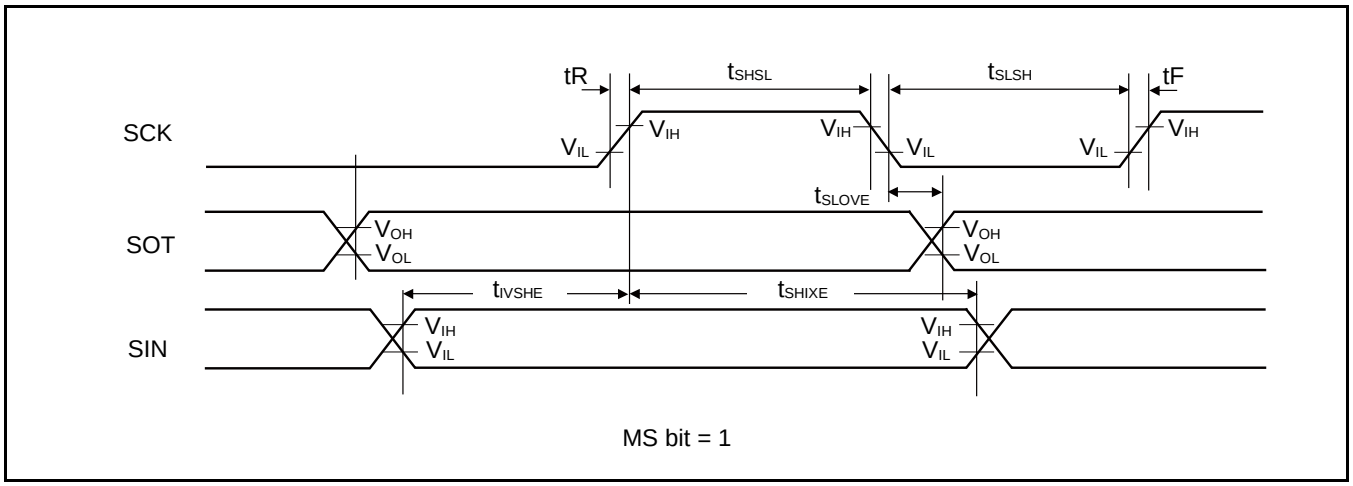
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK ↓ →SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ →SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK ↓ →SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

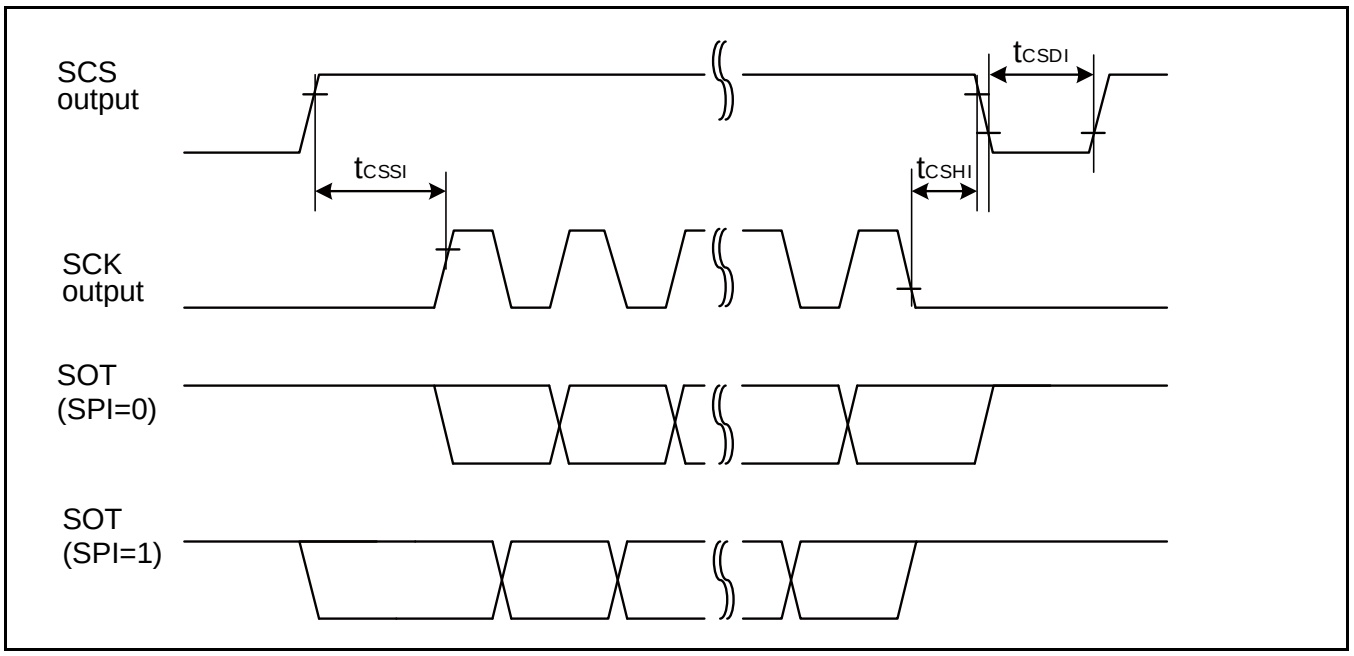
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

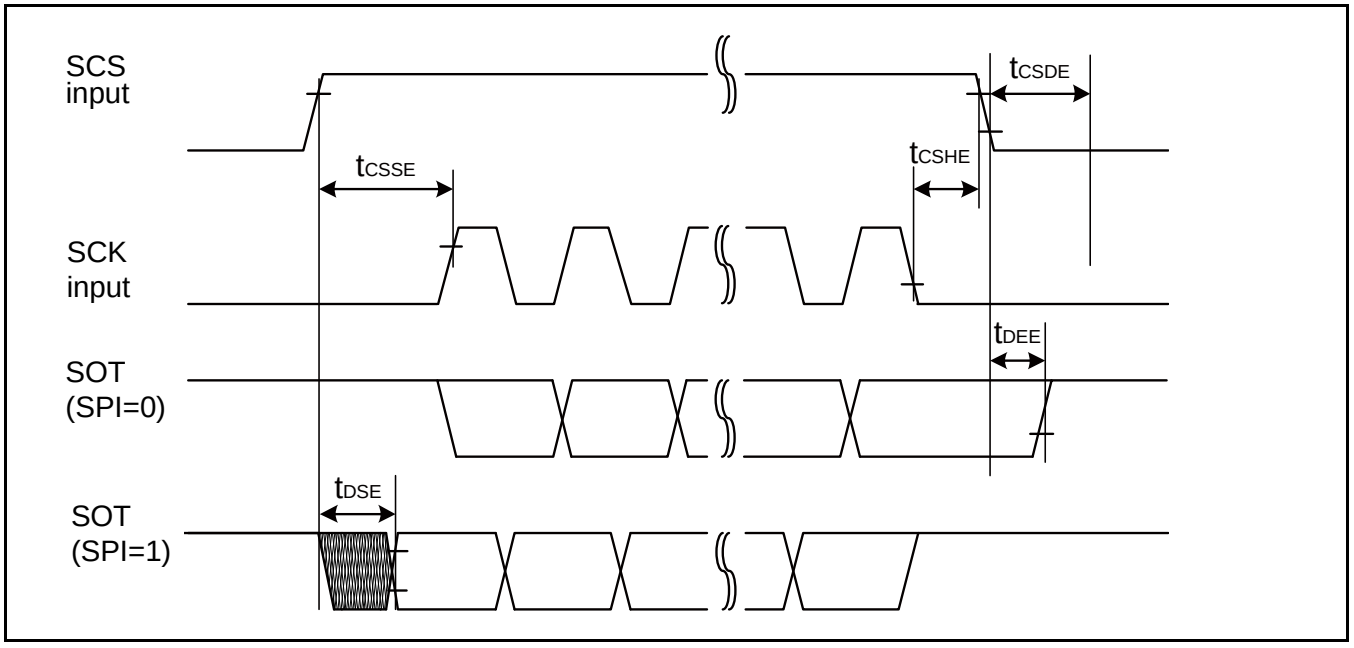
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual.*
- *When the external load capacitance C_L = 30 pF.*


SCS
output
tCSDI
tCSSI
tCSHI
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)


SCS
input
tCSDE
tCSSE
tCSHE
SCK
input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-4.5	-	+4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-2.5	-	+2.5	LSB	
Zero transition voltage	V_{ZT}	AN00 to AN14	-15	-	+15	mV	
Full-scale transition voltage	V_{FST}	AN00 to AN14	AVRH - 15	-	AVRH + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5V
Sampling time	Ts	-	*2	-	10	µs	AV_{CC} ≥ 4.5V
			*2	-			AV_{CC} < 4.5V
Compare clock cycle*3	Tcck	-	25	-	1000	ns	AV_{CC} ≥ 4.5V
			50	-	1000		AV_{CC} < 4.5V
State transition time to operation permission	Tstt	-	1.0	-	-	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	0.3	12	µA	When A/D stop
Reference power supply current (between AVRH and AVSS)	-	AVRH	-	1.1	1.97	mA	A/D 1unit operation AVRH=5.5 V
				0.2	4.2	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	10	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	AN00 to AN14	-	-	5	µA	
Analog input voltage	-	AN00 to AN14	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck < 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 150 ns, the value of compare time: 350 ns (AV_{CC} ≥ 4.5 V). Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck). For setting*4 of sampling time and compare clock cycle, see CHAPTER 1-1: A/D Converter in FM4 Family Peripheral Manual Analog macro part (002-04860). The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock. The sampling clock and compare clock are set in base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see 8. Block Diagram in this data sheet.

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

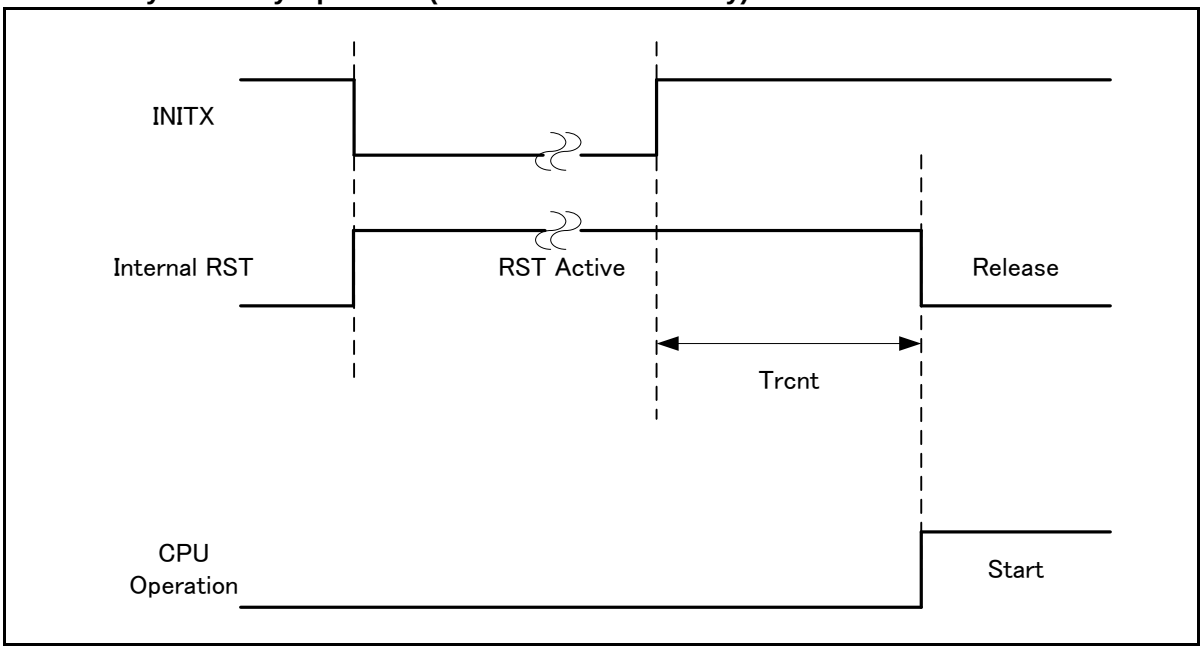
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

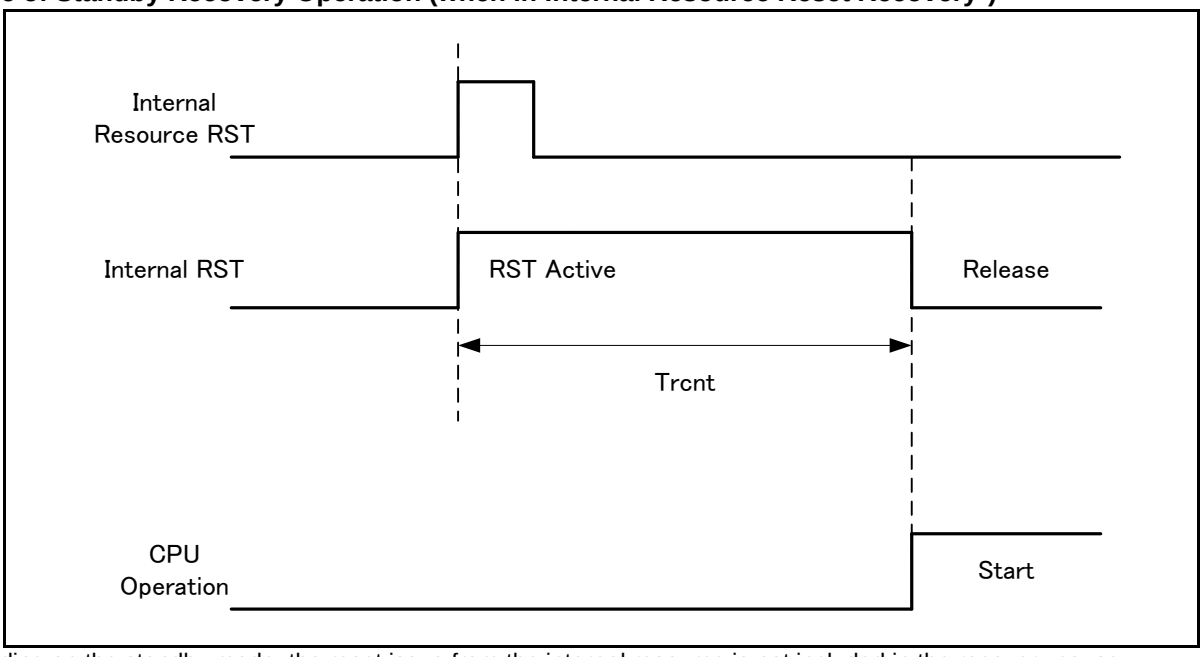
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Trcnt	116	266	µs	
High-speed CR timer mode Main timer mode PLL timer mode		116	266	µs	
Low-speed CR timer mode		258	567	µs	
Sub timer mode		258	567	µs	
RTC mode Stop mode		308	567	µs	
Deep standby RTC mode with RAM retention		308	668	µs	without RAM retention
Deep standby stop mode with RAM retention				µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



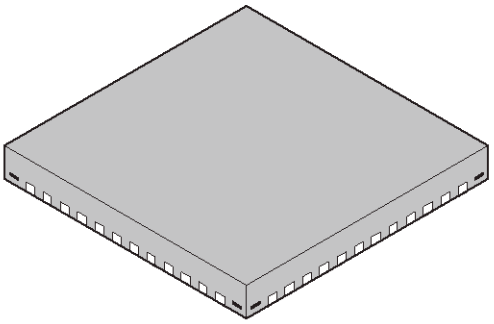
Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



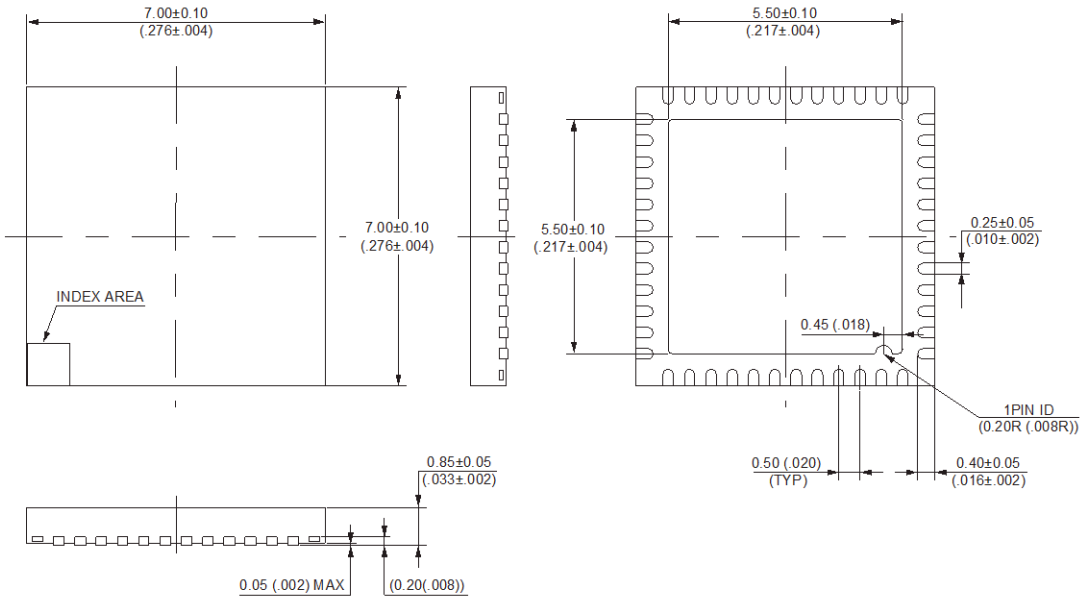
*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See (6) Power-on Reset Timing in 12.4 AC Characteristics in 12. Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

48-pin plastic QFN		
	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	–
(LCC-48P-M73)		

48-pin plastic QFN
(LCC-48P-M73)



Dimensions in mm (inches).
Note: The values in parentheses are reference **values**.

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