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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 6x16b SAR; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08mm128clh

1 Devices in the MC9S08MM128 series

The following table summarizes the feature set available in the MC9S08MM128 series of MCUs.

Table 1. MC9S08MM128 series Features by MCU and Package

Feature	MC9S08MM128			MC9S08MM64	MC9S08MM32	MC9S08MM32A
Pin quantity	81	80	64	64	64	64
FLASH size (bytes)	131072			65535	32768	32768
RAM size (bytes)	12K			12K	4K	2K
Programmable Analog Comparator (PRACMP)	yes			yes	yes	yes
Debug Module (DBG)	yes			yes	yes	yes
Multipurpose Clock Generator (MCG)	yes			yes	yes	yes
Inter-Integrated Communication (IIC)	yes			yes	yes	yes
Interrupt Request Pin (IRQ)	yes			yes	yes	yes
Keyboard Interrupt (KBI)	16	16	6	6	6	6
Port I/O[1]	47	46	33	33	33	33
Dedicated Analog Input Pins	12			12	12	12
Power and Ground Pins	8			8	8	8
Time Of Day (TOD)	yes			yes	yes	yes
Serial Communications (SCI1)	yes			yes	yes	yes
Serial Communications (SCI2)	yes			yes	yes	yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes	yes	yes
Serial Peripheral Interface 2 (SPI2)	yes			yes	yes	yes
Carrier Modulator Timer pin (IRO)	yes			yes	yes	yes
TPM input clock pin (TPMCLK)	yes			yes	yes	yes
TPM1 channels	4			4	4	4
TPM2 channels	4	4	2	2	2	2
XOSC1	yes			yes	yes	yes
XOSC2	yes			yes	yes	yes
USB	yes			yes	yes	no
Programmable Delay Block (PDB)	yes			yes	yes	yes
SAR ADC differential channels[2]	4	4	3	3	3	3
SAR ADC single-ended channels	8	8	6	6	6	6
DAC ouput pin (DACO)	yes			yes	yes	yes
Voltage reference output pin (VREFO)	yes			yes	yes	yes
General Purpose OPAMP (OPAMP)	yes			yes	yes	yes
Trans-Impedance Amplifier (TRIAMP)	yes			yes	yes	yes

1 Port I/O count does not include two (2) output-only and one (1) input-only pins.

2 Each differential channel is comprised of 2 pin inputs.

A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC16)	1
General Purpose Operational Amplifier (OPAMP)	1
Trans-Impedance Operational Amplifier (TRIAMP)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)[1]	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

[1] USB Module not available on MC9S08MM32A devices.

The block diagram in Figure 1 shows the structure of the MC9S08MM128 series MCU.

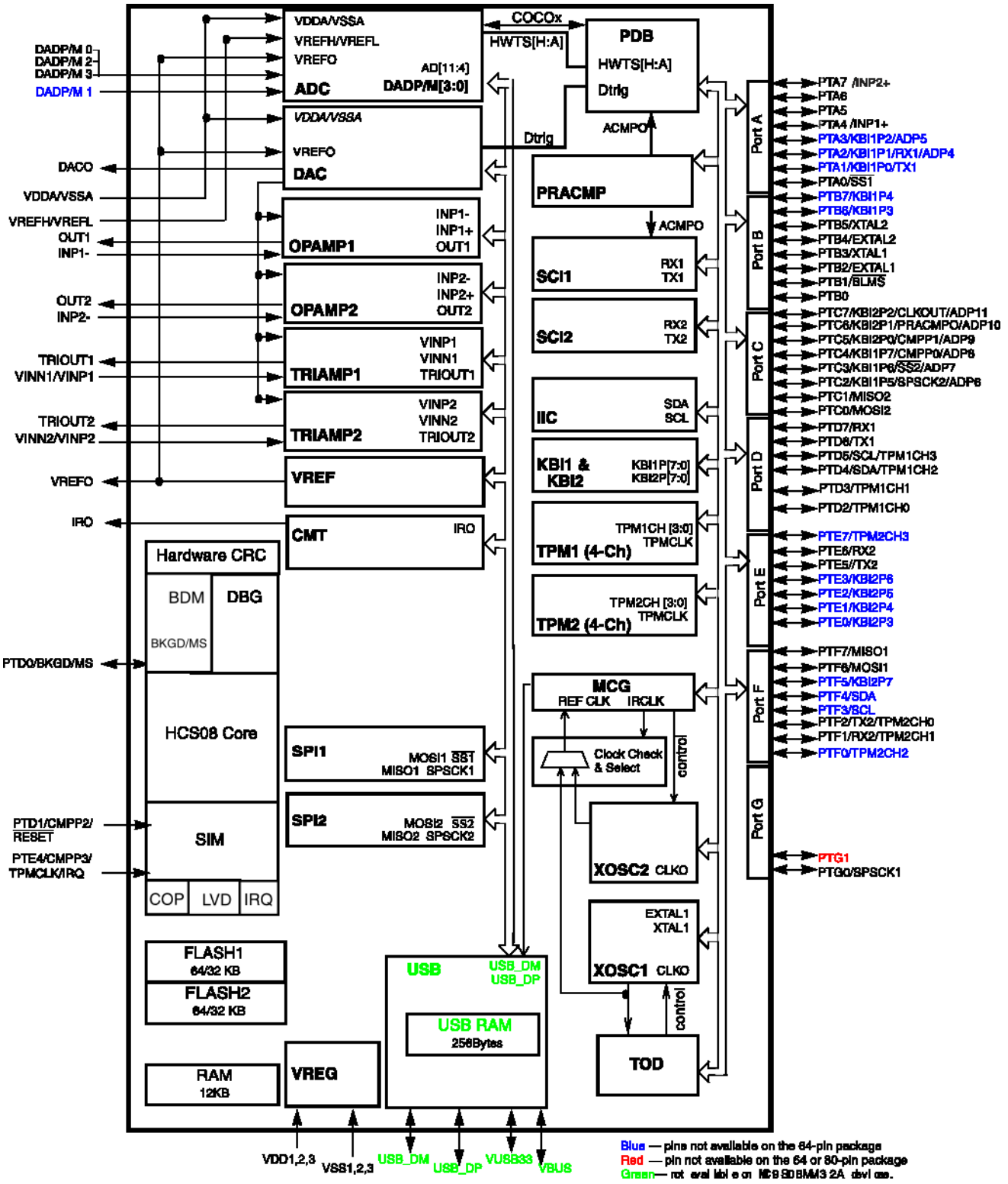


Figure 1. MC9S08MM128 series Block Diagram

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MC9S08MM128	–40 to 105	
		MC9S08MM64	–40 to 105	
		MC9S08MM32	–40 to 105	
		MC9S08MM32A	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
1	V_{DD}	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600$ µA	$V_{DD} - 0.5$	—	—	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current	Max total I_{OH} for all ports					
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600$ µA	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current	Max total I_{OL} for all ports —	—	—	100	mA	D
6	V_{IH}	Input high voltage	all digital inputs					
			all digital inputs, $V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V	P
			all digital inputs, 2.7 V > $V_{DD} \geq$ 1.8 V	0.85 x V_{DD}	—	—	V	P

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode; all modules ON[2]							
			24 MHz	3	20	24	mA	–40 to 25	P
			24 MHz	3	20	24	mA	105	P
			20 MHz	3	18	—	mA	–40 to 105	T
			8 MHz	3	8	—	mA	–40 to 105	T
			1 MHz	3	1.8	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; all modules OFF[3]							
			24 MHz	3	12.3	14.1	mA	–40 to 105	C
			20 MHz	3	10.5	—	mA	–40 to 105	T
			8 MHz	3	4.8	—	mA	–40 to 105	T
			1 MHz	3	1.3	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPS=0; all modules OFF[3]							
			16 kHz FBILP	3	153	222	µA	–40 to 105	T
			16 kHz FBELP	3	143	200	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPS=1, all modules OFF[3]							
			16 kHz FBELP	3	20	26	µA	0 to 70	T
			16 kHz FBELP	3	20	70	µA	–40 to 105	T

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			24 MHz	3	6.7	—	mA	–40 to 105	C
			20 MHz	3	5.6	—	mA	–40 to 105	T
			8 MHz	3	2.4	—	mA	–40 to 105	T
			1 MHz	3	1	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	10	40	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.39	0.8	µA	–40 to 25	P
			N/A	3	2.4	4.5	µA	70	C
			N/A	3	7	11	µA	85	C
			N/A	3	16	22	µA	105	P
			N/A	2	0.2	0.45	µA	–40 to 25	C
			N/A	2	2	3.8	µA	70	C
			N/A	2	8	12	µA	85	C
			N/A	2	10	20	µA	105	C

2.8 12-Bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	µA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	µA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C\text{-}C}LP$	—	—	5	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode (3 V at Room Temperature)	$Ts_{C\text{-}C}HP$	—	1	—	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0) (3 V at Room Temperature)	$V_{dacoutl}$	—	—	100	mV	T	

Table 15. 16-Bit ADC Operating Conditions (Continued)

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
10	f_{ADCK}	ADC Conversion Clock Frequency							
			ADLPC=0, ADHSC=1	1.0	—	8.0	MHz	D	
			ADLPC=0, ADHSC=0	1.0	—	5.0	MHz	D	
			ADLPC=1, ADHSC=0	1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

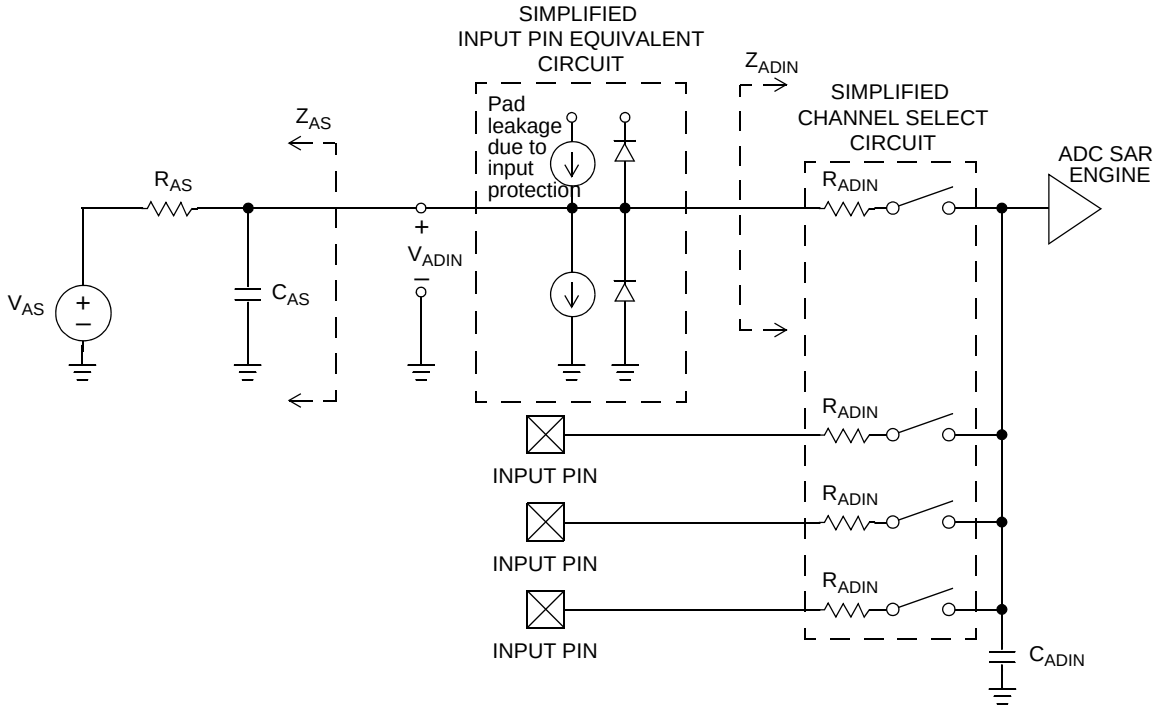


Figure 7. ADC Input Impedance Equivalency Diagram

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP =0 ADCO=1
		ADLPC=0, ADHSC=0		—	470	—			
		ADLPC=0, ADHSC=1		—	610	—			
2	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	T	
3	ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	C	$t_{ADACK} = 1/f_{ADACK}$
		ADLPC=0, ADHSC=0		—	5.2	—			
		ADLPC=0, ADHSC=1		—	6.2	—			
4	Sample Time	See Reference Manual for sample times							
5	Conversion Time	See Reference Manual for conversion times							
6	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+48/ –40 +56/ –28	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±3.0 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
7	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	+5/–3 +5/–3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 16. 16-Bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDA}, > 1.8, V_{REFL} = V_{SSA} ≤ 8 MHz, –40 to 85 °C) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
14	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–91.5	–74.3	dB	C	F_{in} = F_{sample}/100
		16-bit single-ended mode Avg=32		—	–85.5	—		D	
15	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	75.0	92.2	—	dB	C	F_{in} = F_{sample}/100
		16-bit single-ended mode Avg=32		—	86.2	—		D	
16	Input Leakage Error	all modes	E_{IL}	I_{In} * R_{AS}			mV	D	I_{In} = leakage current (refer to DC characteristics)
17	Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
		25°C – 125°C		—	1.769	—			
18	Temp Sensor Voltage	25°C	V_{TEMP25}	—	718.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} – V_{REFL})/2^N

Table 20. Control Timing

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

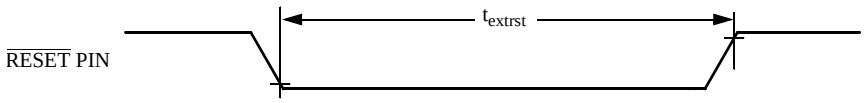


Figure 8. Reset Timing

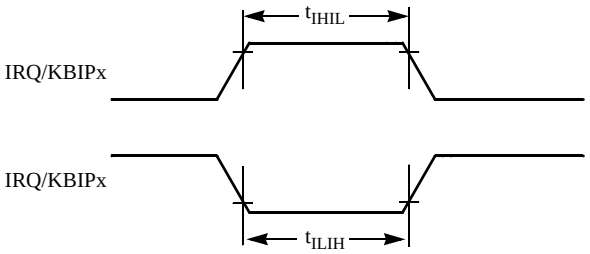
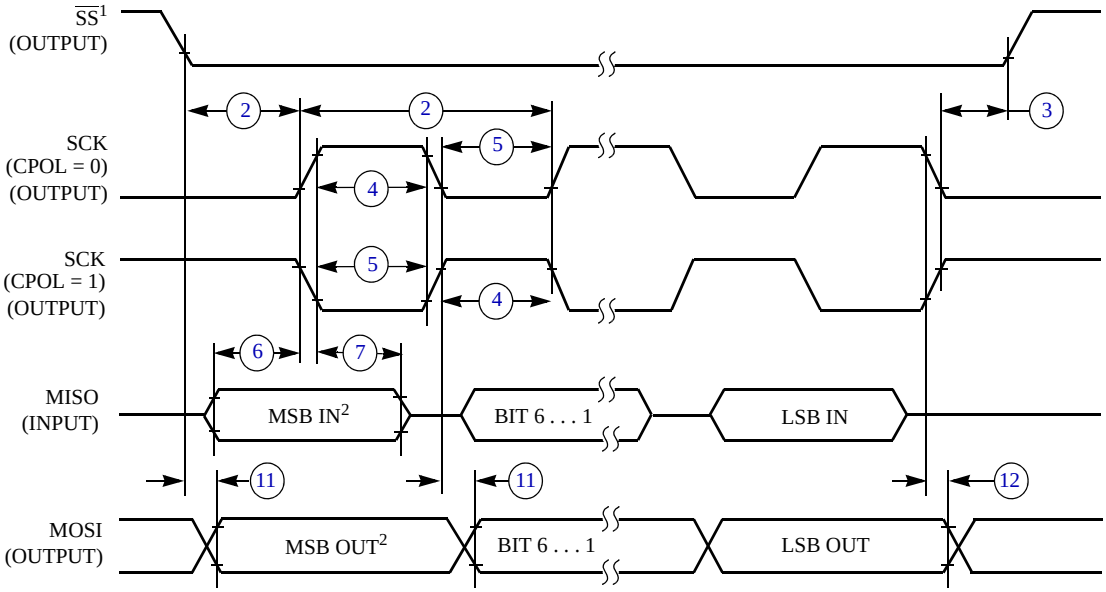
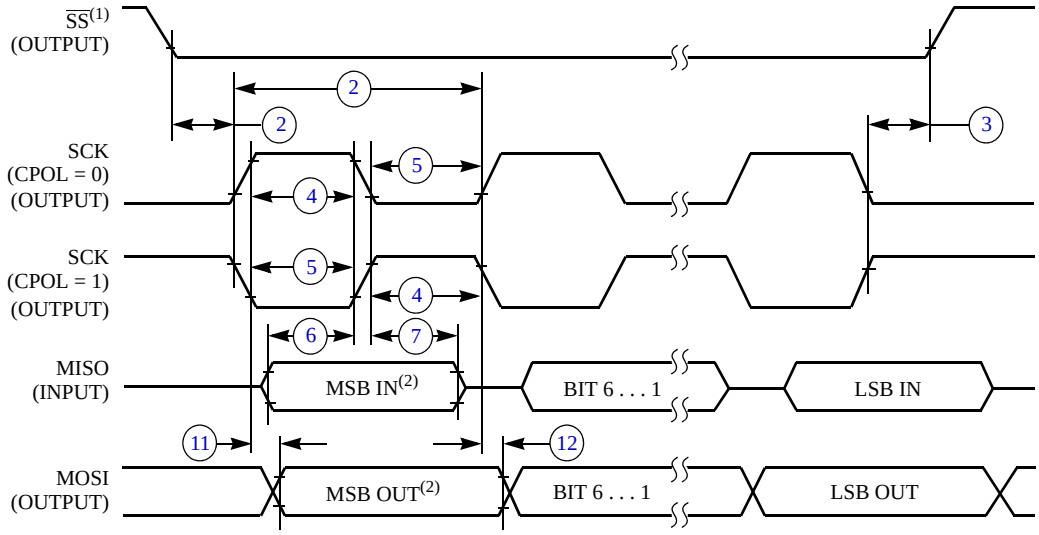


Figure 9. IRQ/KBIPx Timing



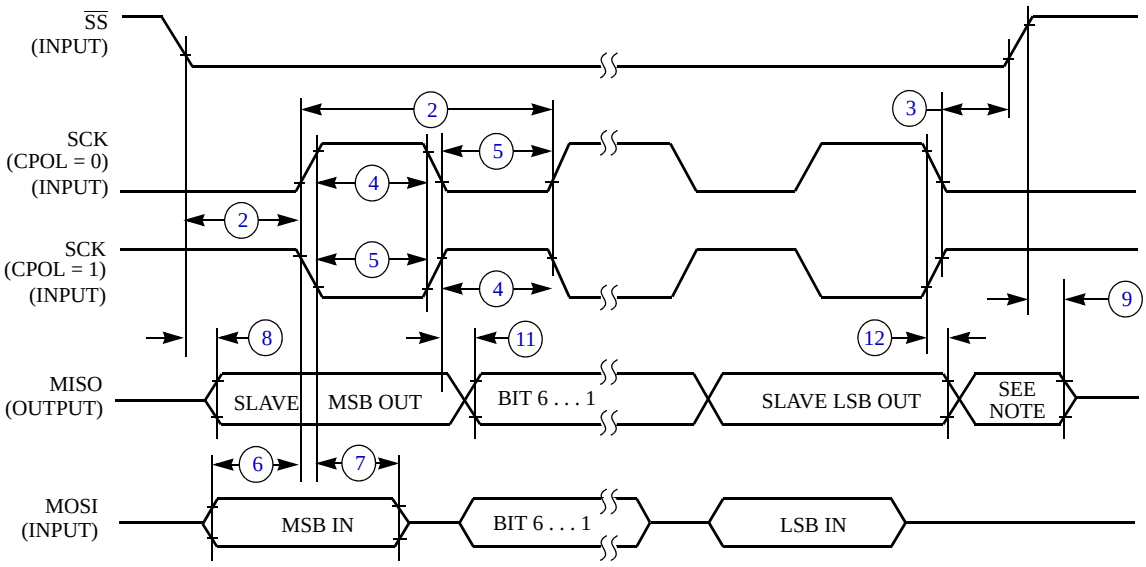
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

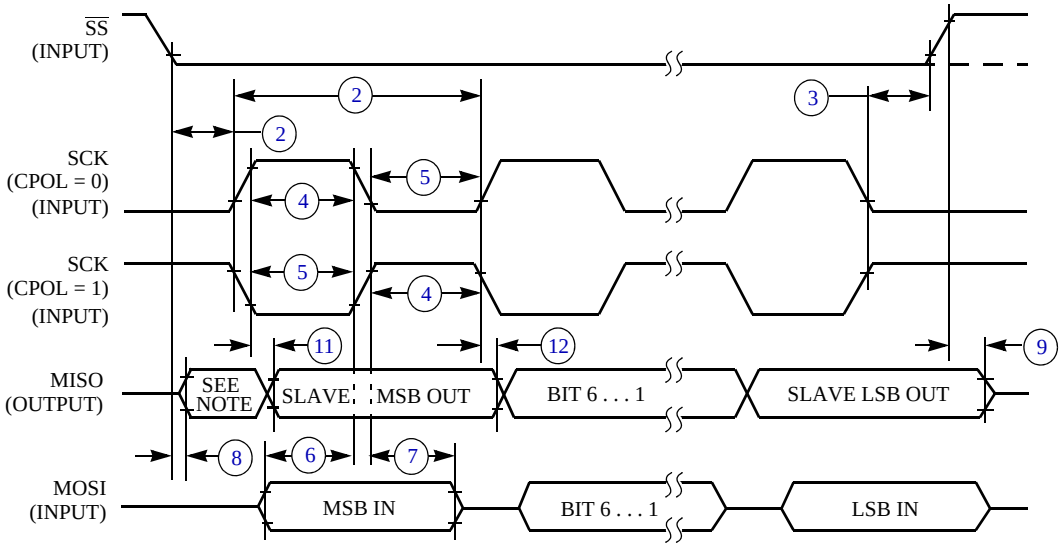
Figure 13. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 14. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 15. SPI Slave Timing (CPHA = 1)

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

2.17 OPAMP Electrical Parameters

Table 28. OPAMP Characteristics 1.8–3.6 V

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0 Low-Power mode)	I_{SUPPLY}	—	67	80	μA	T
3	Supply Current (I_{OUT}=0mA, CL=0 High-Speed mode)	I_{SUPPLY}	—	538	550	μA	T
4	Input Offset Voltage	V_{OS}	—	±2	±6	mV	T
5	Input Offset Voltage Temperature Coefficient	α_{VOS}	—	10	—	μV/C	T
6	Input Offset Current (–40°C to 105°C)	I_{OS}	—	±2.5	±250	nA	T
7	Input Offset Current (–40°C to 50°C)	I_{OS}	—	—	45	nA	T
8	Positive Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	0.8	3.5	nA	T
9	Positive Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	±2	nA	T
10	Negative Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	2.5	250	nA	T
11	Negative Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	45	nA	T
12	Input Common Mode Voltage Low	V_{CML}	0.1	—	—	V	T
13	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}	V	T
14	Input Resistance	R_{IN}	—	500	—	MΩ	T
15	Input Capacitances	C_{IN}	—	—	10	pF	D
16	AC Input Impedance (f_{IN}=100kHz Negative Channel)	$\lvert X_{IN} \rvert$	—	52	—	kΩ	D
17	AC Input Impedance (f_{IN}=100kHz Positive Channel)	$\lvert X_{IN} \rvert$	—	132	—	kΩ	D
18	Input Common Mode Rejection Ratio	CMRR	55	65	—	dB	T
19	Power Supply Rejection Ratio	PSRR	60	65	—	dB	T
20	Slew Rate (ΔV_{IN}=100mV Low-Power mode)	SR	0.1	—	—	V/μs	T
21	Slew Rate (ΔV_{IN}=100mV High-Speed mode)	SR	1	—	—	V/μs	T
22	Unity Gain Bandwidth (Low-Power mode)	GBW	0.2	—	—	MHz	T
23	Unity Gain Bandwidth (High-Speed mode)	GBW	1	—	—	MHz	T
24	DC Open Loop Voltage Gain	A_V	80	90	—	dB	T
25	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
26	Output Impedance AC Open Loop (@100 kHz Low-Power mode)	R_{OUT}	—	4k	—	Ω	D
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.15	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T

3.2 Package Information

Table 30. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F-02	98ASS23234W
80	Low Quad Flat Package	LQFP	LK	917-01	98ASS23174W
81	MAPBGA Package	Map PBGA	MB	1662-01	98ASA10670D

3.3 Mechanical Drawings

Table 30 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08MM128 series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 30, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 30) in the “Enter Keyword” search box at the top of the page.

4 Revision History

Table 31. Revision History

Rev	Date	Description of Changes
0	06/2009	Initial release of the Data Sheet.
1	07/2009	Updated MCG and XOSC Average internal reference frequency.
2	01/2010	Revised to include MC9S08MM32 and MC9S08MM32A devices.Updated electrical characteristic data.
3	10/2010	Updated with the latest characteristic data. Added several figures. Added the ADCTypical Operation table.

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