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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08mm128cmb

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08MM128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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1 Devices in the MC9S08MM128 series

The following table summarizes the feature set available in the MC9S08MM128 series of MCUs.

Table 1. MC9S08MM128 series Features by MCU and Package

Feature	MC9S08MM128			MC9S08MM64	MC9S08MM32	MC9S08MM32A
Pin quantity	81	80	64	64	64	64
FLASH size (bytes)	131072			65535	32768	32768
RAM size (bytes)	12K			12K	4K	2K
Programmable Analog Comparator (PRACMP)	yes			yes	yes	yes
Debug Module (DBG)	yes			yes	yes	yes
Multipurpose Clock Generator (MCG)	yes			yes	yes	yes
Inter-Integrated Communication (IIC)	yes			yes	yes	yes
Interrupt Request Pin (IRQ)	yes			yes	yes	yes
Keyboard Interrupt (KBI)	16	16	6	6	6	6
Port I/O[1]	47	46	33	33	33	33
Dedicated Analog Input Pins	12			12	12	12
Power and Ground Pins	8			8	8	8
Time Of Day (TOD)	yes			yes	yes	yes
Serial Communications (SCI1)	yes			yes	yes	yes
Serial Communications (SCI2)	yes			yes	yes	yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes	yes	yes
Serial Peripheral Interface 2 (SPI2)	yes			yes	yes	yes
Carrier Modulator Timer pin (IRO)	yes			yes	yes	yes
TPM input clock pin (TPMCLK)	yes			yes	yes	yes
TPM1 channels	4			4	4	4
TPM2 channels	4	4	2	2	2	2
XOSC1	yes			yes	yes	yes
XOSC2	yes			yes	yes	yes
USB	yes			yes	yes	no
Programmable Delay Block (PDB)	yes			yes	yes	yes
SAR ADC differential channels[2]	4	4	3	3	3	3
SAR ADC single-ended channels	8	8	6	6	6	6
DAC ouput pin (DACO)	yes			yes	yes	yes
Voltage reference output pin (VREFO)	yes			yes	yes	yes
General Purpose OPAMP (OPAMP)	yes			yes	yes	yes
Trans-Impedance Amplifier (TRIAMP)	yes			yes	yes	yes

1 Port I/O count does not include two (2) output-only and one (1) input-only pins.

2 Each differential channel is comprised of 2 pin inputs.

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/$\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	INP1+	—	—	PTA4/INP1+
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	INP2+	—	—	PTA7/INP2+
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	INP1-	—	—	—	INP1-
E1	15	12	OUT1	—	—	—	OUT1
F2	16	13	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
F1	17	14	VINP1	—	—	—	VINP1
E2	18	15	DADM2	VINN1	—	—	DADM2/VINN1
F3	19	16	INP2-	—	—	—	INP2-
E3	20	17	OUT2	—	—	—	OUT2
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
H4	23	20	VINP2	—	—	—	VINP2
G4	24	21	DADM3	VINN2	—	—	DADM3/VINN2
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33[1]	—	—	—	VUSB33
B4	73	57	USB_DM[2]	—	—	—	USB_DM
A4	74	58	USB_DP[3]	—	—	—	USB_DP
A5	75	59	VBUS[4]	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

1 NC on MC9S08MM32A devices.
2 NC on MC9S08MM32A devices.
3 NC on MC9S08MM32A devices.
4 NC on MC9S08MM32A devices.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08MM128/64/32/32A microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVWH}	Low-voltage warning threshold — high range[9] — V_{DD} falling						
			—	2.36	2.46	2.56	V	P
		V_{DD} rising						
			—	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9] — V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.23	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.15	1.17	1.18	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to V_{DD} or V_{SS} and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

Table 11. Typical Stop Mode Adders (Continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			–40	25	70	85	105		
7	DAC[1]	High-Power mode; no load on DACO	369	377	377	390	410	µA	T
		Low-Power mode	50	51	51	52	60	µA	T
8	OPAMP[1]	High-Power mode	453	538	538	540	540	µA	T
		Low-Power mode	56	67	67	68	70	µA	T
9	TRIAMP[1]	High-Power mode	430	432	433	438	478	µA	T
		Low-Power mode	52	52	52	55	60	µA	T

1 Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	80	µA	D
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	D
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	D
6	Analog input offset voltage	VAIO	—	5	40	mV	D
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	D
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	D
10	Programmable reference generator inputs	V_{In2} (V_{DD25})	1.8	—	2.75	V	D
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	0.75	1	1.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	V_{In}/32	—	V_{in}	V	P

Table 16. 16-Bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDA}, > 1.8, V_{REFL} = V_{SSA} ≤ 8 MHz, –40 to 85 °C) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
8	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.5 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
9	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+32/ –24 +24/ –16	LSB[2]	T	V_{ADIN} = V_{SSA}
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.5 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
10	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+10/0 +14/0	+42/–2 +46/–2	LSB[2]	T	V_{ADIN} = V_{DDA}
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±3.5 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
11	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
12	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	C	F_{in} = F_{sample}/100
13	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+24/ –24 +32/–20	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.0 ±1.25		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
2	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
3	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
4	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, f_{ADACK} ≤ 4 MHz, ADHSC = 1) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
5	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
6	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
7	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
8	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		
9	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–95.8	–90.4	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
10	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	91.0	96.5	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
11	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	D
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz	D
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz	D
		• High range (RANGE = 1), • High gain (HGO = 1), • BLPE mode	f_{hi-hgo}	1	—	16	MHz	D
		• High range (RANGE = 1), • Low power (HGO = 0), • BLPE mode	f_{hi-lp}	1	—	8	MHz	D
2	Load capacitors		C_1 C_2	See crystal or resonator manufacturer's recommendation.				D
3	Feedback resistor	• Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ	D
		• High range (1 MHz to 16 MHz)		—	1	—		D
4	Series resistor — Low range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)		—	100	—		D
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)						D
		≥ 8 MHz		—	0	0		D
		4 MHz		—	0	10		D
		1 MHz		—	0	20		D

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
6	Crystal start-up time [4]	• Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms	D
		• Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—		D
		• High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH-LP}$	—	5	—		D
		• High range, high gain (RANGE = 1, HGO = 1)[5]	$t_{CSTH-HGO}$	—	15	—		D

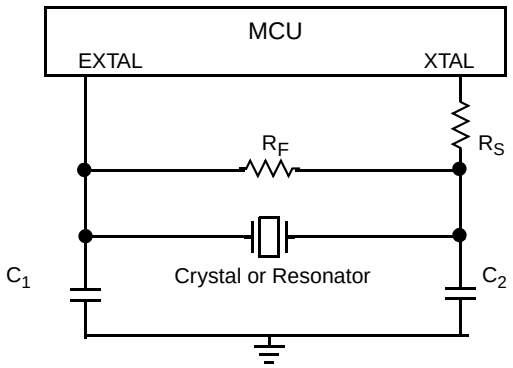
1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout porcedures must be followed to achieve specifications.

5 4 MHz crystal.



2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 20. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		700	1000	1300	P	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

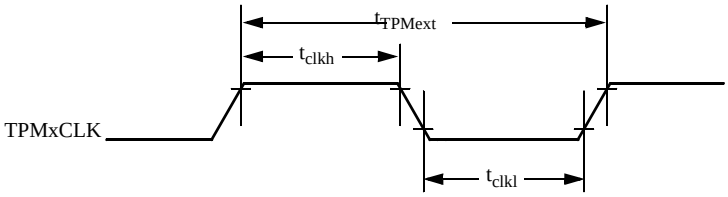


Figure 10. Timer External Clock

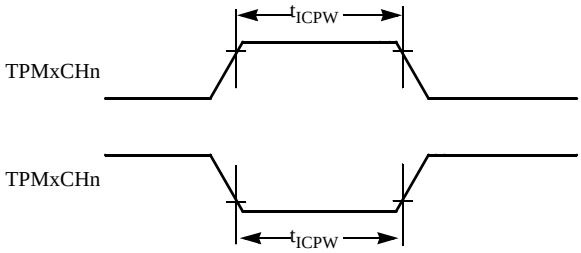
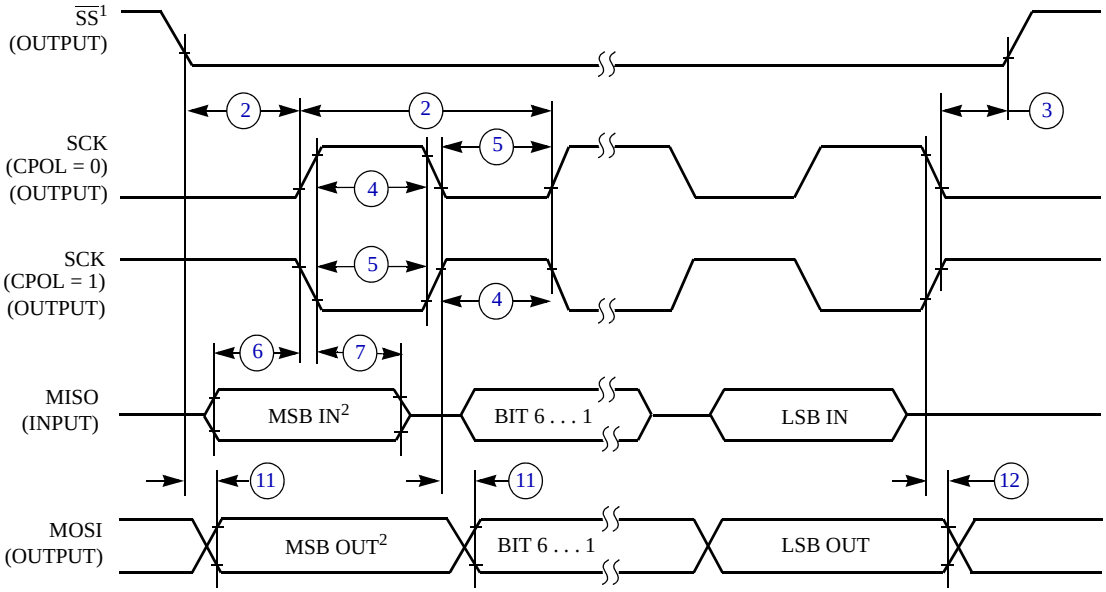
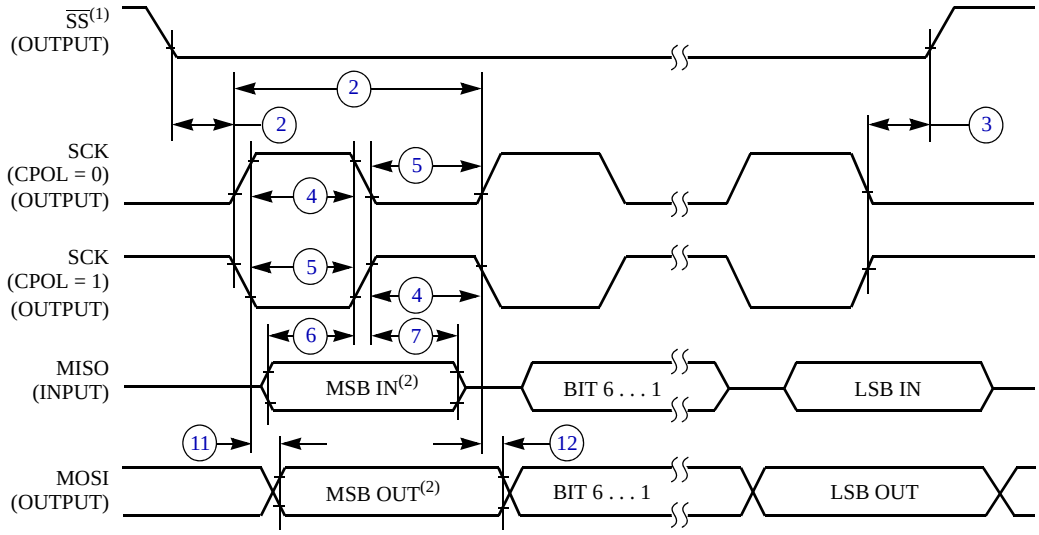


Figure 11. Timer Input Capture Pulse



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 13. SPI Master Timing (CPHA = 1)

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

2.15 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V at 25°C.	Vout	1.140	1.160	V	P
6	Temperature Drift (Vmin – Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	µV/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation V_{DD} < 2.3 V, Delta V_{DDA} = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection)	DC	70	—	dB	C

1 See typical chart that follows (Figure 16).

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging µV/year. V_{refo} data recorded per month.

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim (Temperature range from 0° C to 50° C)	V_{out}	1.149	1.152	mV	T	
2	Temperature Drift (V_{min} – V_{max} Temperature range from 0° C to 50° C)	T_{drift}	—	3	mV[1]	T	

1 See typical chart that follows (Figure 16).

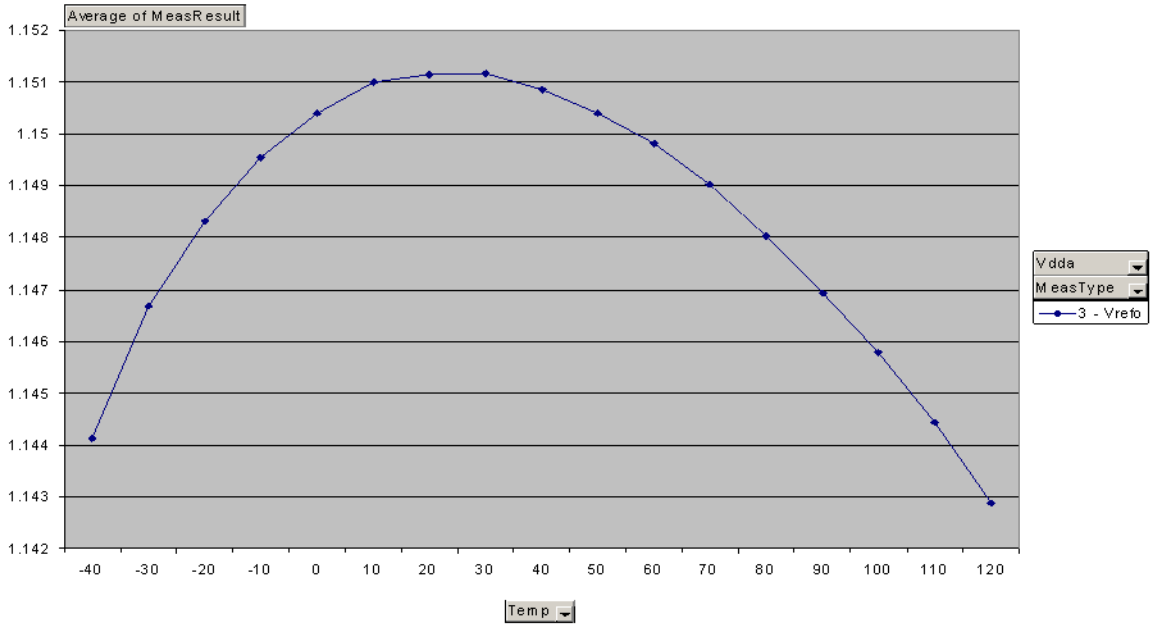


Figure 16. Typical VREF Output vs. Temperature

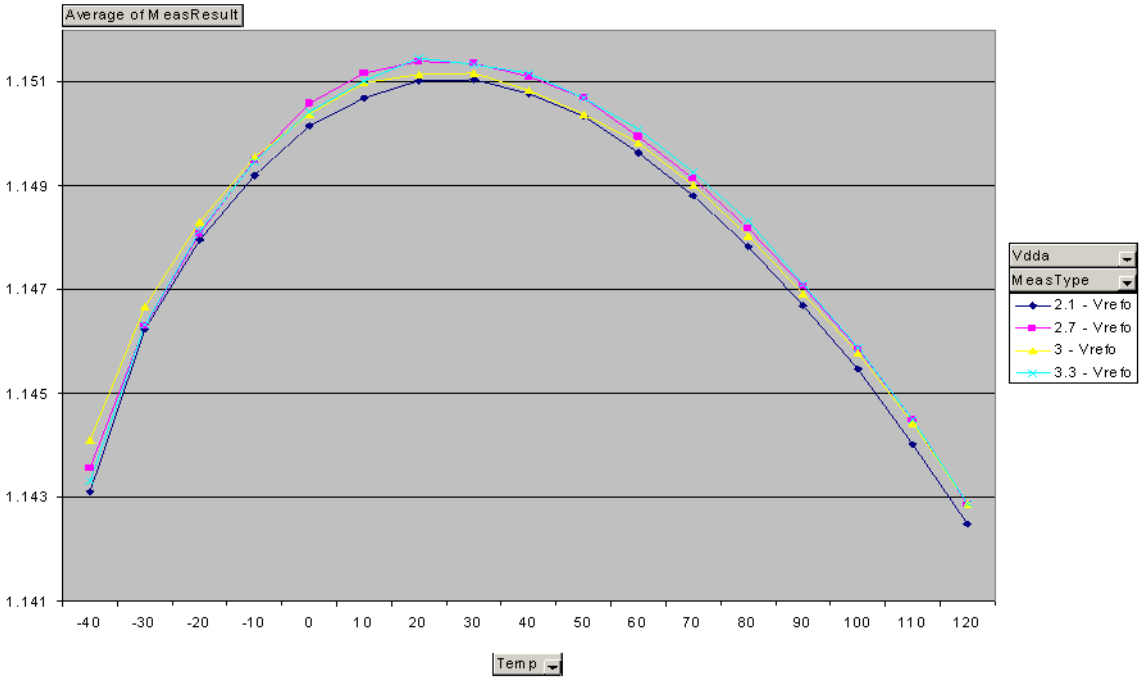


Figure 17. Typical VREF Output vs. V_{DD}

Table 28. OPAMP Characteristics 1.8–3.6 V (Continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

3 Ordering Information

This appendix contains ordering information for the device numbering system. MC9S08MM128 and MC9S08MM64 devices.

3.1 Device Numbering System

Example of the device numbering system:

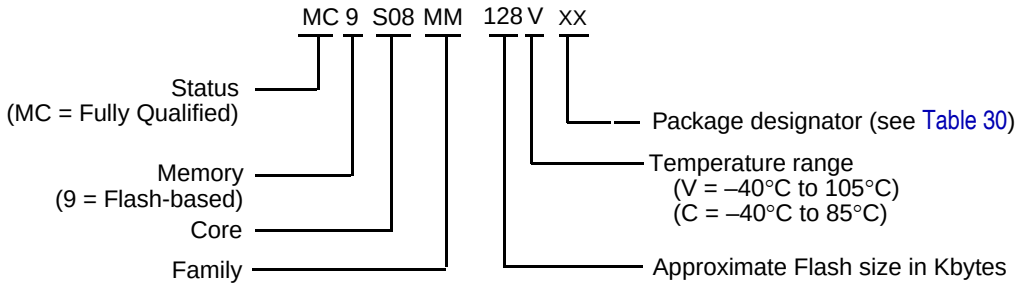


Table 29. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08MM128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08MM64	65,536	12,288	64 LQFP
MC9S08MM32	32768	4096	64 LQFP
MC9S08MM32A	32768	2048	64 LQFP

1 See Table 2 for a complete description of modules included on each device.
2 See Table 30 for package information.