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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 6x16b SAR; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08mm128vlh

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08MM128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC16)	1
General Purpose Operational Amplifier (OPAMP)	1
Trans-Impedance Operational Amplifier (TRIAMP)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)[1]	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

[1] USB Module not available on MC9S08MM32A devices.

The block diagram in Figure 1 shows the structure of the MC9S08MM128 series MCU.

1.1 Pin Assignments

This section shows the pin assignments for the MC9S08MM128 series devices.

1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration. The first illustrates the pinout configuration for MC9S08MM128, MC9S08MM64, and MC9S08MM32 devices.

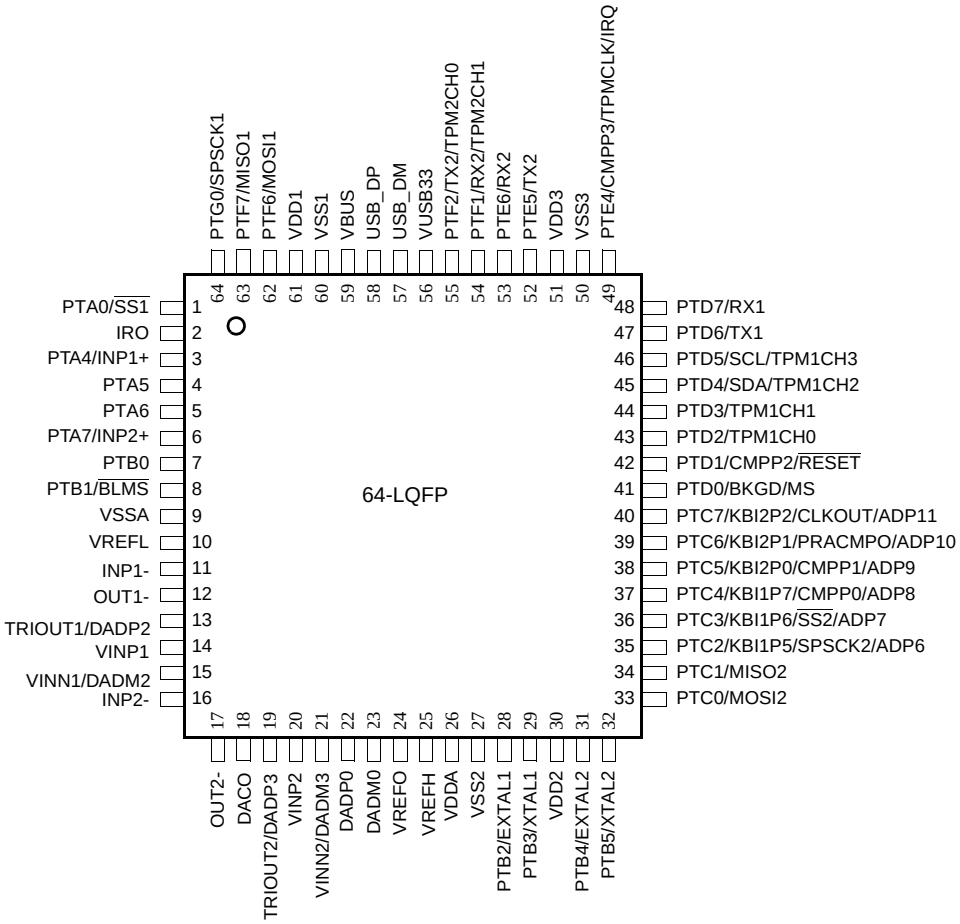


Figure 2. 64-Pin LQFP for MC9S08MM128, MC9S08MM64, and MC9S08MM32 devices

For MC9S08MM32A devices, pins 56, 57, 58, and 59 are no connects (NC) as illustrated in the following figure.

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/$\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	INP1+	—	—	PTA4/INP1+
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	INP2+	—	—	PTA7/INP2+
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	INP1-	—	—	—	INP1-
E1	15	12	OUT1	—	—	—	OUT1
F2	16	13	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
F1	17	14	VINP1	—	—	—	VINP1
E2	18	15	DADM2	VINN1	—	—	DADM2/VINN1
F3	19	16	INP2-	—	—	—	INP2-
E3	20	17	OUT2	—	—	—	OUT2
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
H4	23	20	VINP2	—	—	—	VINP2
G4	24	21	DADM3	VINN2	—	—	DADM3/VINN2
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
J3	30	25	VREFH	—	—	—	VREFH
J4	31	26	VDDA	—	—	—	VDDA
F4	32	27	VSS2	—	—	—	VSS2
J5	33	28	PTB2	EXTAL1	—	—	PTB2/EXTAL1
J6	34	29	PTB3	XTAL1	—	—	PTB3/XTAL1
E4	35	30	VDD2	—	—	—	VDD2
J8	36	31	PTB4	EXTAL2	—	—	PTB4/EXTAL2
J9	37	32	PTB5	XTAL2	—	—	PTB5/XTAL2
G6	38	—	PTB6	KBI1P3	—	—	PTB6/KBI1P3
F7	39	—	PTB7	KBI1P4	—	—	PTB7/KBI1P4
G7	40	33	PTC0	MOSI2	—	—	PTC0/MOSI2
G8	41	34	PTC1	MISO2	—	—	PTC1/MISO2
G9	42	35	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
H5	43	36	PTC3	KBI1P6	$\overline{SS2}$	ADP7	PTC3/KBI1P6/$\overline{SS2}$/ADP7
H6	44	37	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
H8	45	38	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
H9	46	39	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	47	40	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
H7	48	41	PTD0	BKGD	MS	—	PTD0/BKGD/MS
J7	49	42	PTD1	CMPP2	$\overline{RESET}$	—	PTD1/CMPP2/$\overline{RESET}$
E7	50	43	PTD2	TPM1CH0	—	—	PTD2TPM1CH0
E8	51	44	PTD3	TPM1CH1	—	—	PTD3/TPM1CH1
F9	52	45	PTD4	SDA	TPM1CH2	—	PTD4/SDA/TPM1CH2
D7	53	46	PTD5	SCL	TPM1CH3	—	PTD5/SCL/TPM1CH3
E9	54	47	PTD6	TX1	—	—	PTD6/TX1
D8	55	48	PTD7	RX1	—	—	PTD7/RX1
D9	56	—	PTE0	KBI2P3	—	—	PTE0/KBI2P3
C9	57	—	PTE1	KBI2P4	—	—	PTE1/KBI2P4
C8	58	—	PTE2	KBI2P5	—	—	PTE2/KBI2P5
B9	59	—	PTE3	KBI2P6	—	—	PTE3/KBI2P6
A9	60	49	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33[1]	—	—	—	VUSB33
B4	73	57	USB_DM[2]	—	—	—	USB_DM
A4	74	58	USB_DP[3]	—	—	—	USB_DP
A5	75	59	VBUS[4]	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

1 NC on MC9S08MM32A devices.
2 NC on MC9S08MM32A devices.
3 NC on MC9S08MM32A devices.
4 NC on MC9S08MM32A devices.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MC9S08MM128	–40 to 105	
		MC9S08MM64	–40 to 105	
		MC9S08MM32	–40 to 105	
		MC9S08MM32A	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
7	V_{IL}	Input low voltage — all digital inputs						
			all digital inputs, $V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			all digital inputs, $2.7 > V_{DD} \geq 1.8$ V	—	—	0.30 x V_{DD}	V	P
8	V_{hys}	Input hysteresis — all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current — all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.5	µA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3] — all digital input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	0.003	0.5	µA	P
11	R_{PU}	Pull-up resistors	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit						
			$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		Total MCU limit, includes sum of all stressed pins						
			$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	µs	D
18	V_{LVDH}[9]	Low-voltage detection threshold — high range — V_{DD} falling						
			—	2.11	2.16	2.22	V	P
		V_{DD} rising						
			—	2.16	2.23	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9] — V_{DD} falling						
			—	1.80	1.84	1.88	V	P
		V_{DD} rising						
			—	1.88	1.93	1.96	V	P

Table 11. Typical Stop Mode Adders (Continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			–40	25	70	85	105		
7	DAC[1]	High-Power mode; no load on DACO	369	377	377	390	410	µA	T
		Low-Power mode	50	51	51	52	60	µA	T
8	OPAMP[1]	High-Power mode	453	538	538	540	540	µA	T
		Low-Power mode	56	67	67	68	70	µA	T
9	TRIAMP[1]	High-Power mode	430	432	433	438	478	µA	T
		Low-Power mode	52	52	52	55	60	µA	T

1 Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	80	µA	D
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	D
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	D
6	Analog input offset voltage	VAIO	—	5	40	mV	D
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	D
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	D
10	Programmable reference generator inputs	V_{In2} (V_{DD25})	1.8	—	2.75	V	D
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	0.75	1	1.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	V_{In}/32	—	V_{in}	V	P

2.9 ADC Characteristics

Table 15. 16-Bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
1	V_{DDA}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV_{DDA}		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	–100	0	+100	mV	D	
3	ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	–100	0	+100	mV	D	
4	V_{REFH}	Ref Voltage High		1.15	V_{DDA}	V_{DDA}	V	D	
5	V_{REFL}	Ref Voltage Low		V_{SSA}	V_{SSA}	V_{SSA}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance	16-bit modes 8/10/12-bit modes	—	8 4	10 5	pF	T	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	T	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
		16-bit mode	f_{ADCK} > 8 MHz	—	—	0.5	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	1	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	2	kΩ	T	
		13/12-bit mode	f_{ADCK} > 8 MHz	—	—	1	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	2	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	T	
		11/10-bit mode	f_{ADCK} > 8 MHz	—	—	2	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	T	
		9/8-bit mode	f_{ADCK} > 8 MHz	—	—	5	kΩ	T	
			f_{ADCK} < 8 MHz	—	—	10	kΩ	T	

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP =0 ADCO=1
		ADLPC=0, ADHSC=0		—	470	—			
		ADLPC=0, ADHSC=1		—	610	—			
2	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	T	
3	ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	C	$t_{ADACK} = 1/f_{ADACK}$
		ADLPC=0, ADHSC=0		—	5.2	—			
		ADLPC=0, ADHSC=1		—	6.2	—			
4	Sample Time	See Reference Manual for sample times							
5	Conversion Time	See Reference Manual for conversion times							
6	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+48/ –40 +56/ –28	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±3.0 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
7	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	+5/–3 +5/–3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, f_{ADACK} ≤ 4 MHz, ADHSC = 1) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
5	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
6	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
7	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
8	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		
9	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–95.8	–90.4	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
10	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	91.0	96.5	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
11	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
6	Crystal start-up time [4]	• Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms	D
		• Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—		D
		• High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH-LP}$	—	5	—		D
		• High range, high gain (RANGE = 1, HGO = 1)[5]	$t_{CSTH-HGO}$	—	15	—		D

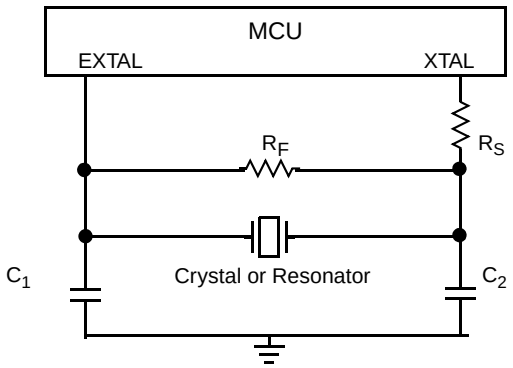
1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout porcedures must be followed to achieve specifications.

5 4 MHz crystal.



2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 20. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		700	1000	1300	P	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

2.12 SPI Characteristics

Table 22 and Figure 12 through Figure 15 describe the timing requirements for the SPI system.

Table 22. SPI Timing

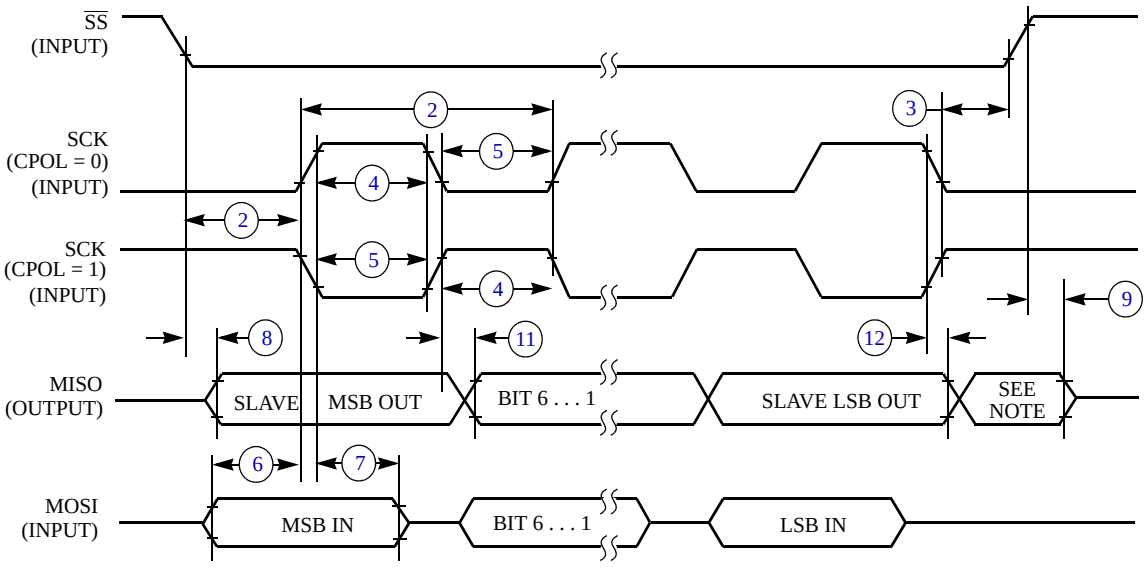
No.[1]	Characteristic[2]	Symbol	Min	Max	Unit	C
1	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	 t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	 t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 12 through Figure 15.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

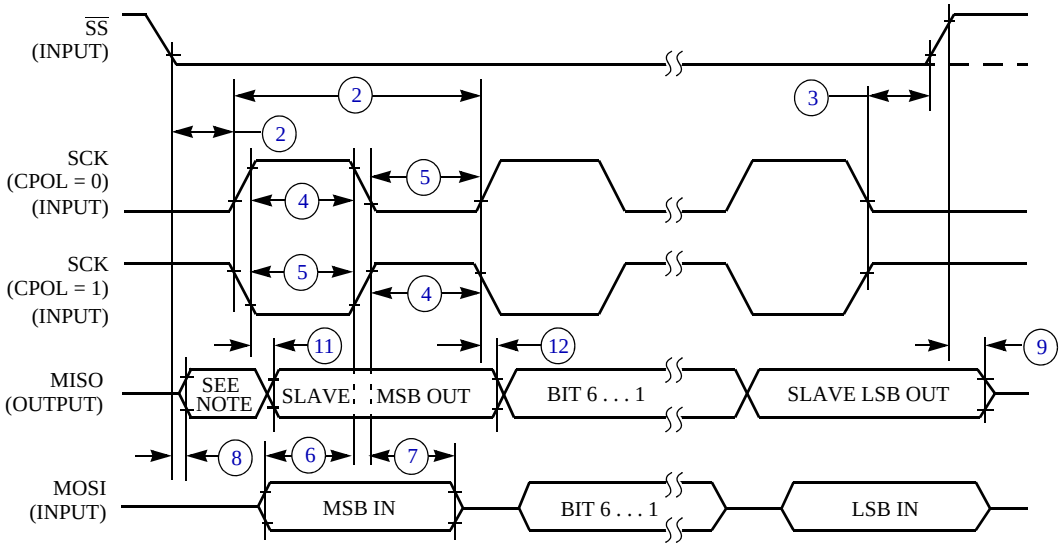
4 Hold time to high-impedance state.



NOTE:

1. Not defined, but normally MSB of character just received

Figure 14. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 15. SPI Slave Timing (CPHA = 1)

2.15 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V at 25°C.	Vout	1.140	1.160	V	P
6	Temperature Drift (Vmin – Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	µV/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation V_{DD} < 2.3 V, Delta V_{DDA} = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection)	DC	70	—	dB	C

1 See typical chart that follows (Figure 16).

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging µV/year. V_{refo} data recorded per month.

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim (Temperature range from 0° C to 50° C)	V_{out}	1.149	1.152	mV	T	
2	Temperature Drift (V_{min} – V_{max} Temperature range from 0° C to 50° C)	T_{drift}	—	3	mV[1]	T	

1 See typical chart that follows (Figure 16).

2.17 OPAMP Electrical Parameters

Table 28. OPAMP Characteristics 1.8–3.6 V

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0 Low-Power mode)	I_{SUPPLY}	—	67	80	μA	T
3	Supply Current (I_{OUT}=0mA, CL=0 High-Speed mode)	I_{SUPPLY}	—	538	550	μA	T
4	Input Offset Voltage	V_{OS}	—	±2	±6	mV	T
5	Input Offset Voltage Temperature Coefficient	α_{VOS}	—	10	—	μV/C	T
6	Input Offset Current (–40°C to 105°C)	I_{OS}	—	±2.5	±250	nA	T
7	Input Offset Current (–40°C to 50°C)	I_{OS}	—	—	45	nA	T
8	Positive Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	0.8	3.5	nA	T
9	Positive Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	±2	nA	T
10	Negative Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	2.5	250	nA	T
11	Negative Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	45	nA	T
12	Input Common Mode Voltage Low	V_{CML}	0.1	—	—	V	T
13	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}	V	T
14	Input Resistance	R_{IN}	—	500	—	MΩ	T
15	Input Capacitances	C_{IN}	—	—	10	pF	D
16	AC Input Impedance (f_{IN}=100kHz Negative Channel)	$\lvert X_{IN} \rvert$	—	52	—	kΩ	D
17	AC Input Impedance (f_{IN}=100kHz Positive Channel)	$\lvert X_{IN} \rvert$	—	132	—	kΩ	D
18	Input Common Mode Rejection Ratio	CMRR	55	65	—	dB	T
19	Power Supply Rejection Ratio	PSRR	60	65	—	dB	T
20	Slew Rate (ΔV_{IN}=100mV Low-Power mode)	SR	0.1	—	—	V/μs	T
21	Slew Rate (ΔV_{IN}=100mV High-Speed mode)	SR	1	—	—	V/μs	T
22	Unity Gain Bandwidth (Low-Power mode)	GBW	0.2	—	—	MHz	T
23	Unity Gain Bandwidth (High-Speed mode)	GBW	1	—	—	MHz	T
24	DC Open Loop Voltage Gain	A_V	80	90	—	dB	T
25	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
26	Output Impedance AC Open Loop (@100 kHz Low-Power mode)	R_{OUT}	—	4k	—	Ω	D
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.15	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T

Table 28. OPAMP Characteristics 1.8–3.6 V (Continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

3 Ordering Information

This appendix contains ordering information for the device numbering system. MC9S08MM128 and MC9S08MM64 devices.

3.1 Device Numbering System

Example of the device numbering system:

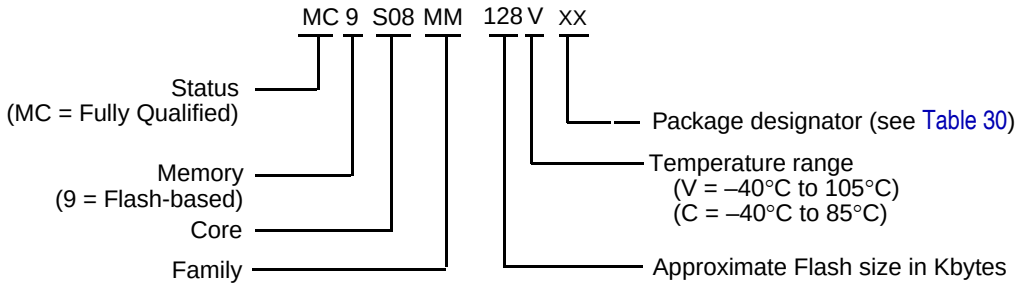


Table 29. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08MM128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08MM64	65,536	12,288	64 LQFP
MC9S08MM32	32768	4096	64 LQFP
MC9S08MM32A	32768	2048	64 LQFP

1 See Table 2 for a complete description of modules included on each device.
2 See Table 30 for package information.

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