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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+40
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-40-qilro-4

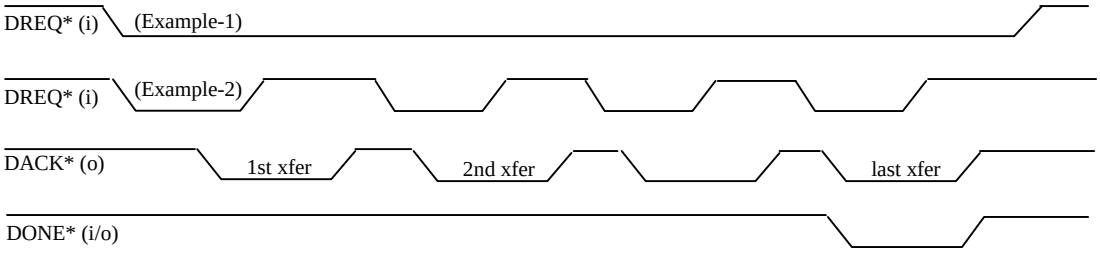


Figure 4-5: External DMA Timing

DREQ*

DREQ* is an input to the NET+ARM, sourced by the external device. All transfers are initiated when the external device asserts DREQ* low. When the external device wants a DMA transfer (either read or write) it will assert the DREQ* signal. The DREQ* can stay low until all data transfers are complete (see the first example of DREQ* in Figure 4-5) or it can be asserted once for each transfer (see the second example of DREQ* in Figure 4-5). Either method is treated the same by the NET+ARM.

DACK*

DACK* is an input to the external device, sourced by the NET+ARM. After the NET+ARM receives DREQ*, and it is ready for a data transfer, it will assert DACK* low at the same time that it asserts the data transfer signals (ADDR, R/W, CAS, RAS, etc). DACK* should be used by the external device as an enable for its memory. If DACK* and R/W* are low the external device should take data from its memory and put it on the data bus. If DACK* is low and R/W* is high, the external device should take the data that is on the data bus and put it in its memory.

DONE*

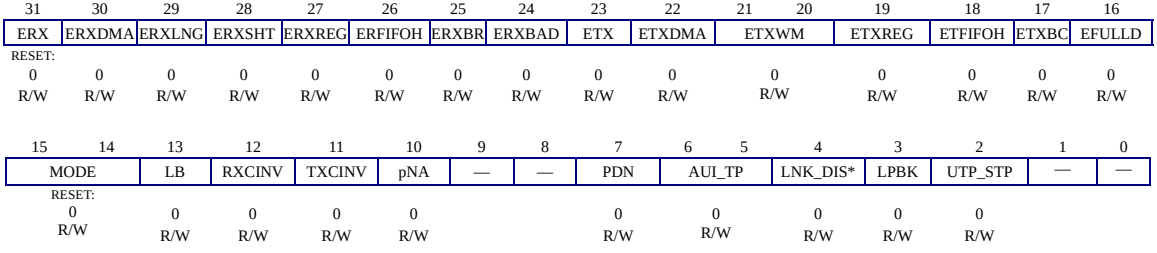
The DONE* signal is either an input or an output depending upon configuration of the direction bit in the GPIO configuration register.

When the transfer is a fly-by write (external device to memory), the external device can send DONE* to the NET+ARM to indicate that it has no more data to send. The external device should make sure that the DONE* signal it sends to the NET+ARM is asserted low while DACK* is asserted low (it should OR the DONE* signal it sends with the DACK* signal it receives). When the NET+ARM receives the DONE* signal, it will close the current buffer and set the NCIP (Normal Completion Interrupt

5.3.1 Ethernet General Control Register

The Ethernet general control register is a 32-bit register. The register bit assignments are defined as follows:

Address = FF80 0000



ERX **Enable RX FIFO**

The ERX bit must be set to active high to allow data to be received from the MAC receiver. The ERX can be used to reset the receive side FIFO. In general, the ERX bit should be set once on device open.

ERXDMA **Enable Receive DMA**

The ERXDMA bit must be set to active high to allow the EFE module to issue receive data move requests to the DMA controller. This bit can be cleared to temporarily stall receive side Ethernet DMA. This bit should not be set when operating the Ethernet receiver in interrupt service mode. In general, the ERXDMA bit should be set once on device open.

ERXLNG **Accept Long (> 1518 bytes) Receive Packets**

When set, the ERXLNG bit allows packets that are larger than 1518 bytes to be accepted by the MAC. In general, the ERXLNG bit should be set once on device open. The ERXLNG bit is typically set only for debugging.

ERXSHT **Accept Short (< 64 bytes) Receive Packets**

When set, the ERXSHT bit allows packets that are smaller than 64 bytes to be accepted by the MAC. In general, the ERXSHT bit should be set once on device open. The ERXSNT bit is typically set only for debugging.

TXAUR **Transmit Abort Under Run**

The TXAUR bit is set to 1 to indicate the last Ethernet packet was not transmitted successfully. Transmission of the packet was aborted due to a FIFO under run condition. A FIFO under run condition indicates the DMA controller was unable to fill the FIFO at a fast enough rate as compared to the rate of transmission on the Ethernet medium. This typically means the DMA controller was not configured for Bursting or the memory peripheral device was not configured for bursting or the memory peripheral device is too slow to support the Ethernet interface.

TXAJ **Transmit Abort Jumbo**

The TXAJ bit is set to 1 to indicate the last Ethernet packet was not transmitted successfully. Transmission of the packet was aborted due to a jumbo condition. The jumbo condition means the packet was too large, larger than 1518 bytes. Packets larger than 1518 bytes will not be transmitted successfully unless the HUGEN bit is set in the MAC Configuration Register.

TXDEF **Transmit Packet Deferred**

The TXDEF bit is set to 1 to indicate the last Ethernet packet transmitted successfully encountered a deferral. TXDEF simply means the packet transmission was delayed because the Ethernet medium was busy at the time of first transmission attempt.

TXCRC **Transmit Packet CRC Error**

The TXCRC bit is set to 1 to indicate the last Ethernet packet transmitted successfully had an embedded CRC error. This condition only occurs when the CRCEN bit in the MAC Configuration Register is set to 0. When CRCEN is set to 0, the MAC does not insert a CRC. Instead, the MAC expects a precompiled CRC to be contained in the last four bytes of the Ethernet packet. If the precompiled CRC is found to be incorrect by the MAC, the MAC sets the TXCRC bit in the Transmit Status Register.

TXLCOL **Transmit Packet Late Collision**

The TXLCOL bit is set to 1 to indicate the MAC encountered a Late Collision while attempting to transmit the Ethernet packet. TXLCOL does not imply the packet was not transmitted, only that a late collision event had occurred. The TXAL bit will be set if the packet transmission was aborted. The MAC attempts to retransmit the packet when the RETRYL bit in the MAC Configuration Register is set to 1.

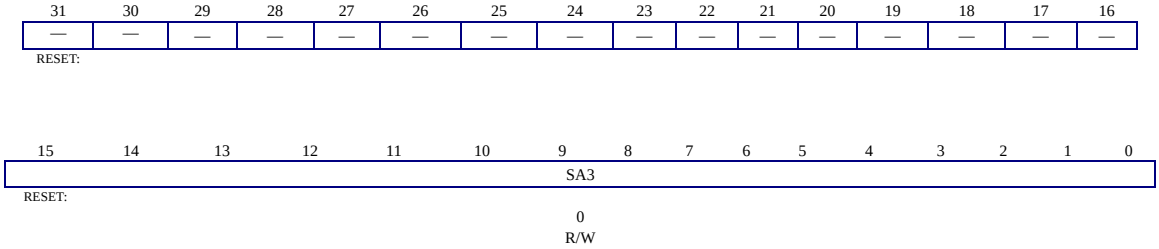
TXCOLC **Transmit Packet Collision Count**

The TXCOLC field indicates how many collisions the MAC encountered while it was attempting to transmit the packet. TXCOLC does not imply the packet was not transmitted; only that collision events had occurred. The TXAEC bit is set if the packet transmission was aborted. The MAC attempts to retransmit the packet up to

TXMCR

The TXMCR counter is incremented each time a packet transmission is aborted because it received too many collisions. The maximum number of allowable collisions is defined by the RETRY field in the Collision Window / Collision Retry Register. The counter is automatically cleared when read provided the AUTOZ bit is set in the STL Configuration Register.

Address = FF80 05CC



SA3

The SA3 field provides the least significant (lower) 16 bits of the 48-bit Station Address value.

6.6.4 Shared Register

The NET+ARM chip supports an 8-bit shared register that allows the ENI interface some control over operation of the ENI interface and provides the NET+ARM chip with the means to interrupt the ENI. The NET+ARM chip accesses this register via the ENI controller configuration space. The ENI itself accesses this register through the ENI interface.

The shared register is accessible only when the ENI controller is configured to operate in ENI shared RAM or ENI FIFO mode.

The ENI Interface accesses the shared register by setting PA16 high. PA16 low accesses the shared RAM. When the ENI is configured to operate in 8-bit mode, the shared register is accessed using PDATA15 through PDATA8. When the ENI is configured to operate in 16-bit mode, the shared register is accessed using PDATA7 through PDATA0.

The VDAINT and STSINT bits in the shared register are set to 0 with a hardware or software reset from the local CPU. The other bits are set to 0 only by a hardware reset from the ENI interface reset (PRESET*).

The shared register can be configured to operate in either NORMAL mode or PSIO mode. The mode is configured using the PSIO bit in the ENI control register. Table 6-13 shows the two possible views for the shared register from the external ENI interface perspective. The register layout from the local CPU perspective always appears in NORMAL mode.

Unlike accessing Shared RAM, when accessing the Shared Register from the external ENI interface, the Shared Register access timing is always the same. The ENI hardware does not need to arbitrate with internal resources when accessing the Shared Register. As such, the Shared Register access timing is fast and consistent.

Data Bit	Normal Mode	PSIO Mode
D7	RSTIO	Reserved
D6	INTIOF	Reserved
D5	EMMINT	EMMINT
D4	EHWINT	RSTIO
D3	SINTP2	CLRINT
D2	VDAINT	EHWINT
D1	STSINT	STSINT
D0	CLRINT	INTIOF

Table 6-13: Shared Register Layout (ENI Interface Perspective Only)

modify EHWINT directly. The EHWINT bit must be set to 1 by the external ENI interface in order to allow either the PINT1* or PINT2* signals to generate an active low interrupt to the external ENI interface. Sources of interrupt for the external ENI interface include the STSINT and VDAINT bits in this register, the RDBUFRDY* and WRBUFEMP* bits in the FIFO Mask/Status Register, and a write by the NET+ARM CPU to the Pulsed Interrupt Register.

SINTP2 ENI PINT1*/PINT2* Interrupt Selection

0: PINT1*

1: PINT2*

Only the external ENI interface can modify the SINTP2 bit. The NET+ARM CPU cannot modify SINTP2 directly. The SINTP2 bit is controlled by the external ENI interface to determine which signal PINT1* or PINT2* will be used for interrupts to the external ENI interface.

VDAINT NET+ARM Interrupt to External ENI Interface

Only the internal ARM processor can modify the VDAINT bit. The external ENI interface cannot modify VDAINT directly. The VDAINT bit is set by the NET+ARM CPU to send an interrupt to the external ENI interface using either PINT1* or PINT2* depending upon the value defined in SINTP2. The EHWINT bit must also be set to active high for VDAINT to generate an interrupt to the external ENI interface. The VDAINT interrupt condition is cleared by the external ENI interface by setting the CLRINT bit to 1 then back to 0. The VDAINT can also be acknowledged by having the external ENI interface write to the Clear Interrupts memory mapped address location defined in Section *6.6.2 Memory Map*.

STSINT NET+ARM Interrupt to ENI

Only the internal ARM processor can modify the STSINT bit. The external ENI interface cannot modify STSINT directly. The STSINT bit is set by the NET+ARM CPU to send an interrupt to the external ENI interface using either PINT1* or PINT2* depending upon the value defined in SINTP2. The EHWINT bit must also be set to active high for STSINT to generate an interrupt to the external ENI interface. The STSINT interrupt condition is cleared by the external ENI interface by setting the CLRINT bit to 1 then back to 0. The STSINT can also be acknowledged by having the external ENI interface write to the Clear Interrupts memory mapped address location defined in Section *6.6.2 Memory Map*.

CLRINT ENI Clear Interrupt from NET+ARM

Only the external ENI interface can modify the CLRINT bit. The NET+ARM CPU cannot modify CLRINT directly. The CLRINT bit can be used by the external ENI interface to clear the VDAINT and STSINT interrupt conditions. The CLRINT bit must be set to 1 then back to 0 to clear these interrupt conditions.

Chapter 8
GEN Module

The GEN module provides the NET+ARM chip with some miscellaneous functions:

1. (2) Programmable Timers with Interrupt
2. (1) Programmable Bus-Error Timer
3. (1) Programmable Watch-Dog Timer
4. (3) 8-bit programmable Parallel I/O Ports with Interrupt
5. System Priority Interrupt Controller
6. Miscellaneous System Control Functions

8.1 Module Configuration

The General module has a block of configuration space is mapped into the GEN module configuration space as defined in Table 2-1, *BBus Address Decoding*.

Address	Register
FFB0 0000	System Control Register
FFB0 0004	System Status Register
FFB0 0008	PLL Control Register
FFB0 000C	Software Service Register
FFB0 0010	Timer 1 Control Register
FFB0 0014	Timer 1 Status Register
FFB0 0018	Timer 2 Control Register
FFB0 001C	Timer 2 Status Register
FFB0 0020	PORT A Register
FFB0 0024	PORT B Register
FFB0 0028	PORT C Register

Table 8-1: General Configuration

PORTB6

The PORTB6 bit can be configured for GPIO Input mode or GPIO Output Mode.

The PORTB6 bit can be configured for Special Function Output. When configured for Special Function Output, the PORTB6 signal provides the Data Terminal Ready (DTR) signal for Serial PORT B. Control Register A within the SER Module configuration controls the state of DTR. The DTR signal configuration is active high inside the NET+ARM and active low outside the NET+ARM. The GEN Module performs inversion before driving the PORTB6 I/O pad.

The PORTB6 bit can be configured for Special Function Input. When configured for Special Function Input, the PORTB6 signal provides the active low DMA Request (DREQ*) input signal for DMA Channel 4. DMA Channel 4 only uses the DMA Request Input on PORTB6 when the REQ bit is set to 1 in the DMA Channel 4 Control Register.

PORTB5

The PORTB5 bit can be configured for GPIO Input mode or GPIO Output Mode.

The PORTB5 bit can be configured for Special Function Output. When configured for Special Function Output, the PORTB5 signal provides the Request To Send (RTS) signal for Serial PORT B. Control Register A within the SER Module configuration controls the state of RTS. The RTS signal configuration is active high inside the NET+ARM and active low outside the NET+ARM. The GEN Module performs inversion before driving the PORTB5 I/O pad.

The PORTB5 bit has no useful function when configured to operate in Special Function Input mode.

PORTB4

The PORTB4 bit can be configured for GPIO Input mode or GPIO Output Mode.

The PORTB4 bit can be configured for Special Function Output. When configured for Special Function Output, PORTB4 provides one of 3 Serial Channel B features, depending upon the configuration of the Serial Channel.

When the Serial Channel is configured for SPI Master mode, PORTB4 Special Function Output drives the active low SPI Master Enable signal out the PORTB4 pin.

When the Serial Channel is not configured for SPI Master mode and the RXEXT bit is set to 1 in the Serial Channel Bit-Rate Register, then the Serial Channel Receiver Clock will be driven out the PORTB4 pin.

When the Serial Channel is not configured for SPI Master mode and the RXEXT bit is set to 0 in the Serial Channel Bit-Rate Register, then the Serial Channel General Purpose OUT 1 signal will be driven out the PORTB4 pin. Control Register A within

There are two read-only registers in the interrupt controller:

- The first is the Interrupt Status Register Raw that indicates the source of a NET+ARM interrupt regardless of the Interrupt Enable Register's state. All interrupts that are active in their respective module will be visible in the Interrupt Status Register Raw (0xFFB0 0038).
- The second read-only register is the Interrupt Status Register Enabled (0xFFB0 0034). This register identifies the current state of all interrupt sources that are enabled and is defined by performing a logical *AND* of the Interrupt Status Register Raw and the Interrupt Enable Register. All of the bits in the Interrupt Status Register Enabled are then *OR-ed* together; the output of which is fed directly to the IRQ line that then interrupts the ARM.

All of the five Interrupt Control Registers use the same 32-bit register layout definition as defined below.

Address = FFB0 0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA1	DMA2	DMA3	DMA4	DMA5	DMA6	DMA7	DMA	DMA9	DMA10	ENI PORT 1	ENI PORT 2	ENI PORT 3	ENI PORT 4	ENET RX	ENET TX
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER 1 RX	SER 1 TX	SER2 RX	SER 2 TX	—	—	—	—	—	Watch Dog	Timer 1	Timer 2	PortC PC3	PortC PC2	PortC PC1	PortC PC0
RESET:															
0	0	0	0						0	0	0	0	0	0	0
R/W	R/W	R/W	R/W						R/W	R/W	R/W	R/W	R/W	R/W	R/W

DMA 1

The DMA 1 bit position corresponds to interrupts source by DMA Channel 1. Please refer to Section *4.4.3 DMA Status/Interrupt Enable Register* for more details.

DMA 2

The DMA 2 bit position corresponds to interrupts source by DMA Channel 2. Please refer to Section *4.4.3 DMA Status/Interrupt Enable Register* for more details.

DMA 3

The DMA 3 bit position corresponds to interrupts source by DMA Channel 3. Please refer to Section *4.4.3 DMA Status/Interrupt Enable Register* for more details.

Chapter 10
Memory Controller Module

The memory module provides a glueless interface to external memory devices such as Flash, DRAM, EEPROM, and so on. The memory controller contains an integrated DRAM controller. The memory controller supports 5 unique chip select configurations. Each chip select can be configured to interface with an asynchronous device (such as static RAM or flash) or a DRAM device.

The MEM module monitors the BBus interface for access to the BUS module. Those accesses are destined for external resources. If the desired address corresponds to an address base register within the MEM module, then the MEM module provides the memory access signals and responds to the BBus with the necessary completion signal.

The MEM module can be configured to interface with FD, EDO, or synchronous DRAM, however, the NET+ARM chip cannot interface with a mixture of synchronous DRAM and FP or EDO DRAM. All chip selects configured for DRAM must be configured with the same style of DRAM.

10.1 Module Configuration

The memory module has a block of configuration space that is mapped into the MEM module configuration space as defined in Table 2-1, BBus Address Decoding.

Address		Register
FFC0 0000	MMCR	Memory Module Configuration Register
FFC0 0010	BAR0	Chip Select 0 Base Address Register
FFC0 0014	OR0	Chip Select 0 Option Register
FFC0 0020	BAR1	Chip Select 1 Base Address Register
FFC0 0024	OR1	Chip Select 1 Option Register

Table 10-1: Memory Controller Configuration

- Allow External Bus Master Access to DRAM bank
- Support Normal and Burst (page/EDO) cycles
- Programmable Wait States for Normal (also first cycle in burst access), and Burst Cycles
- Programmable Base Address and Chip Select Size

10.6.1 Single Cycle Read/Write

Figure 10-6 shows FP DRAM normal read and write cycles. All DRAM cycles must operate a minimum of 1 wait state. This figure shows DRAM cycles with 2 wait states. A single wait state DRAM cycle requires the DRAM devices to tolerate a single BCLK cycle for RAS pre-charge and CAS access timing. The CAS* signal is deasserted on the rising edge in which TA* is recognized. The RAS* signal is deasserted on the falling edge of BCLK after CAS* is asserted.

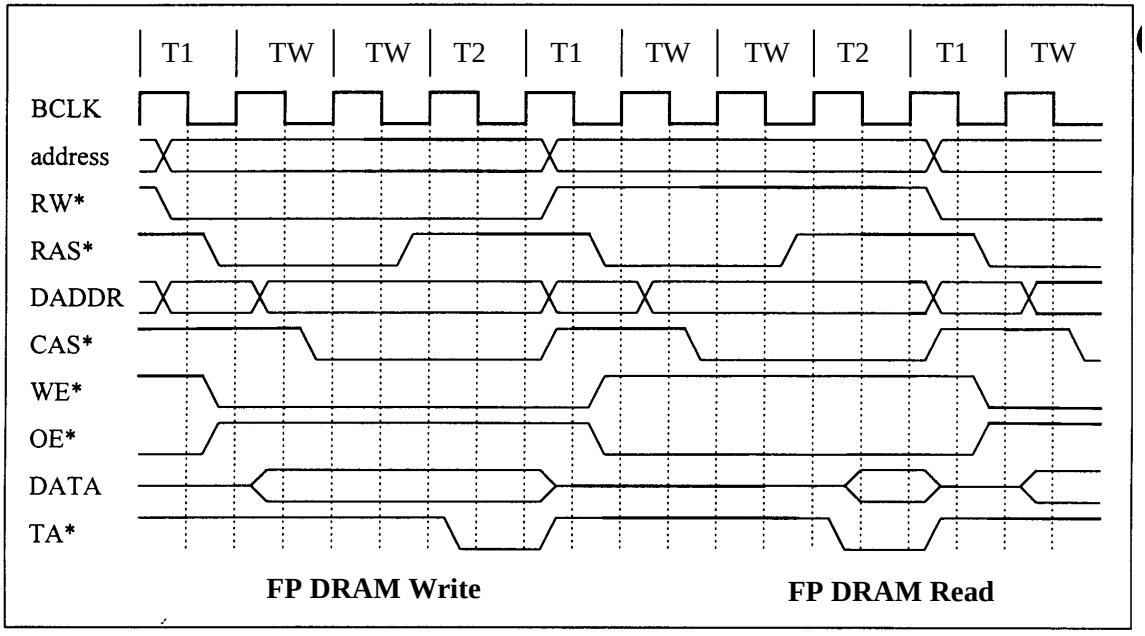


Figure 10-6: Normal FP DRAM Bus Cycles

X16 SDRAM Configuration

The following chart identifies the interconnect between the NET+ARM chip and SDRAM when the SDRAM is used in a x16 configuration. Typically, a x16 SDRAM configuration is constructed using (1) x16 SDRAM component.

NET+ARM Chip Signal	16M SDRAM Signal	64M SDRAM Signal
CS/RAS*	CS*	CS*
CAS3*	RAS*	RAS*
CAS2*	CAS*	CAS*
CAS1*	WE*	WE*
CAS0*	A10/AP	A10/AP
BE3*	UDQM*	UDQM*
BE2*	LDQM*	LDQM*
BE1*	-	-
BE0*	-	-
A1	A0	A0
A2	A1	A1
A3	A2	A2
A4	A3	A3
A5	A4	A4
A6	A5	A5
A7	A6	A6
A8	A7	A7
A9	A8	A8
A10	A9	A9
A11		
A12		A11
A13		
A20	BA	
A21		BA0
A22		BA1

Table 10-4: 16 SDRAM Interconnect

NET+ARM Chip Module	RESET Condition				
	Power Up	RESET*	Watch Dog	ENI	Software
CPU	Yes	Yes	Yes	Yes	No
EFE	Yes	Yes	Yes	Yes	Yes
DMA	Yes	Yes	Yes	Yes	Yes
ENI	Yes	Yes	Yes	No	No
GEN[a]	Yes	Yes	Yes	Yes	Yes
MEM	Yes	Yes	Yes	No	No
SER	Yes	Yes	Yes	Yes	Yes

Table 11-1: RESET Operation

a. All registers in the GEN Module are reset during Power UP, RESET*, Watch Dog, ENI, and Software Reset with a few exceptions. The following GEN Module fields are reset during the POWER UP and RESET* condition only (NOT Watch Dog, ENI, Software Reset):
   BSPEED (GCR),
   BCLKD (GCR),
   PORTA,
   PORTB,
   PORTC
   The reason the above fields are not affected by Watch Dog, ENI, and Software Resets is to prevent the PORTA/B/C and CLOCK outputs from glitching when a reset occurs. This might cause a “valve” to accidentally switch.

The NET+ARM chip contains an integral power up reset circuit that generates the Power UP Reset condition. It is not recommended designs rely solely on the internal power up reset circuit. It is recommended that a system include an external power up reset circuit that drives the RESET* pin active low during power up.

The RESET* pin can be driven active low to reset the NET+ARM chip. RESET* must be driven active low a minimum of 40ms after Vdd reaches the minimum

12.1 ATPG

The NET+ARM chip supports ATPG testing using the full-scan methodology. The NET+ARM chip uses multiple scan chains. The scan chains propagate from primary inputs to primary outputs. Scan testing is enabled when SCANEN* is defined in its active low state.

During scan testing on a tester, the PLL must be disabled such that the tester has direct control of the system clock. The PLLTST* signal, when pulled active low, allows the PLL to be bypassed and all system clocks to be provided by the XTAL1 primary input.

Scan Chain	PLLTST*	BISTEN*	SCANEN*	Input	Output
Chain 1	0	0	0	PA0	PORTA0
Chain 2	0	0	0	PA1	PORTA1
Chain 3	0	0	0	PA2	PORTA2
Chain 4	0	0	0	PA3	PORTA3
Chain 5	0	0	0	PA4	PORTA4
Chain 6	0	0	0	PA5	PORTA5
Chain 7	0	0	0	PA6	PORTA6
Chain 8	0	0	0	PA7	PORTA7
Chain 9	0	0	0	PA8	PORTB0
Chain 10	0	0	0	PA9	PORTB1
Chain 11	0	0	0	PA10	PORTB2
Chain 12	0	0	0	PA11	PORTB3
Chain 13	0	0	0	PA12	PORTB4
Chain 14	0	0	0	PA13	PORTB5
Chain 15	0	0	0	PA14	PORTB6
Chain 16	0	0	0	PA15	PORTB7

Table 12-2: ATPG Test Mode Connections

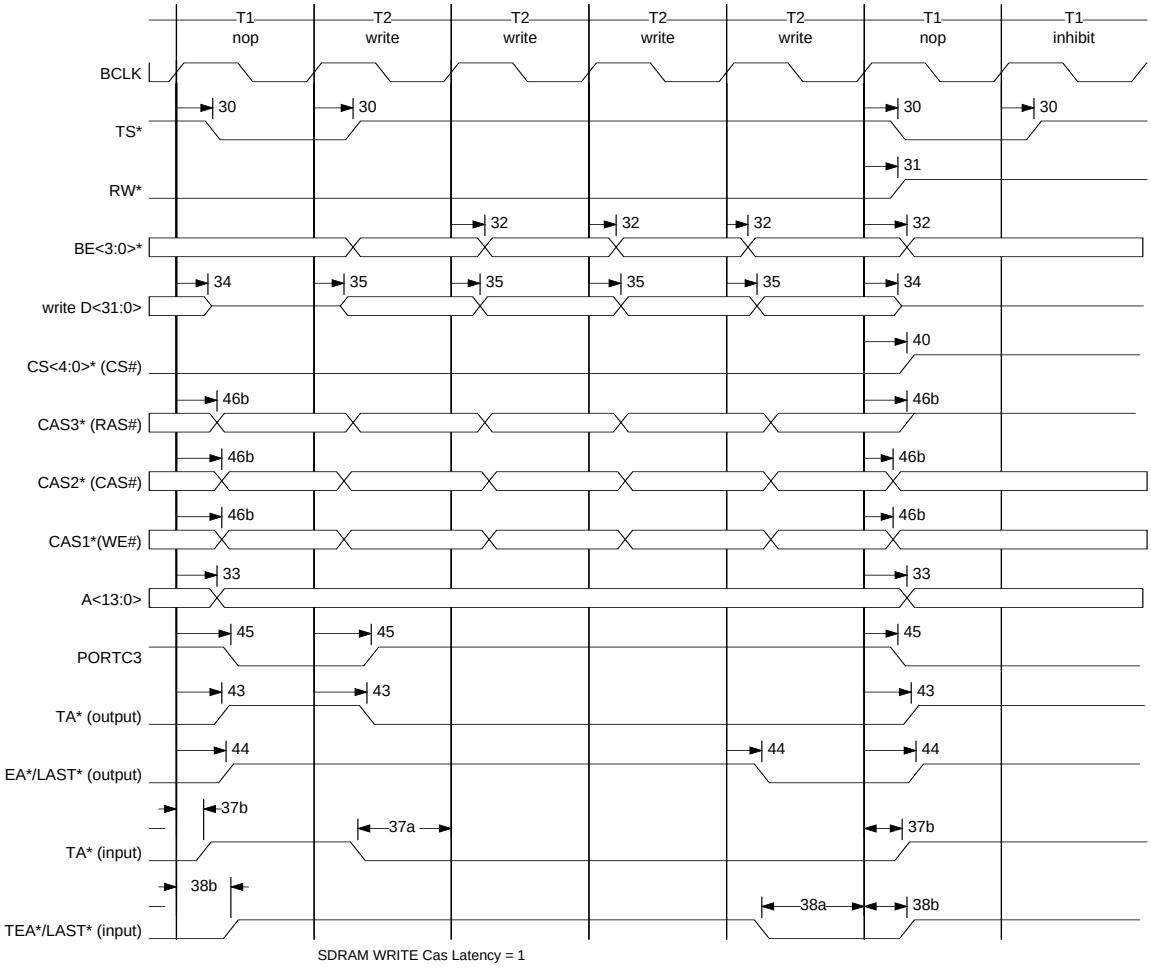


Figure 13-13: SDRAM Burst Write

Refer to Tables 13-9 and 13-10 for values.

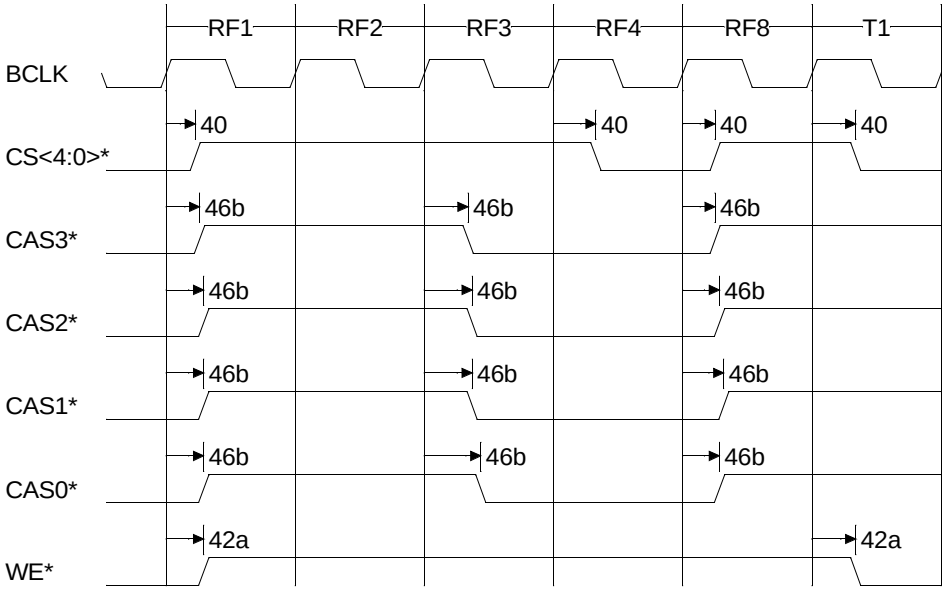


Figure 13-19: DRAM Refresh (RCYC = 3)

Refer to Table 13-10 for values.

Num	Characteristic	Min	Max	Unit
50	BCLK High to DACK* valid		12	ns
51	BCLK High to DONE* (output) valid	0	12	ns
52	DACK* low to DREQ* high (hold)	0		ns
53a	DREQ* valid to BCLK high (setup)	11		ns
53b	BCLK high to DREQ* valid (hold)	0		
54a	DONE* (input) valid to BCLK high (setup)	9		ns
54b	BCLK high to DONE* (input) valid (hold)	0		ns

Table 13-11: External DMA Timing

Num	Characteristic	Min	Max	Unit
60a	RW* valid to BCLK high (setup)	10		ns
60b	BCLK high to RW* invalid (hold)	0		ns
61a	BE* valid to BCLK high (setup)	8		ns
61b	BCLK high to BE* invalid (hold)	0		ns
62a	Address valid to BCLK high (setup)	8		ns
62b	BCLK high to Address invalid (hold)	0		ns
63a	BCLK high to Read Data valid	6	12	ns
63b	BCLK high to Data High Impedance	14	26	ns
64a	Data In valid to BCLK high (setup)	14		ns
64b	BCLK high to Data In invalid (hold)	0		ns
65a	A25/BLAST* valid to BCLK (T2) high (setup)	10		ns
65b	BCLK (T2) high to A25/BLAST* invalid (hold)	0		ns

Table 13-12: External Bus Master Timing

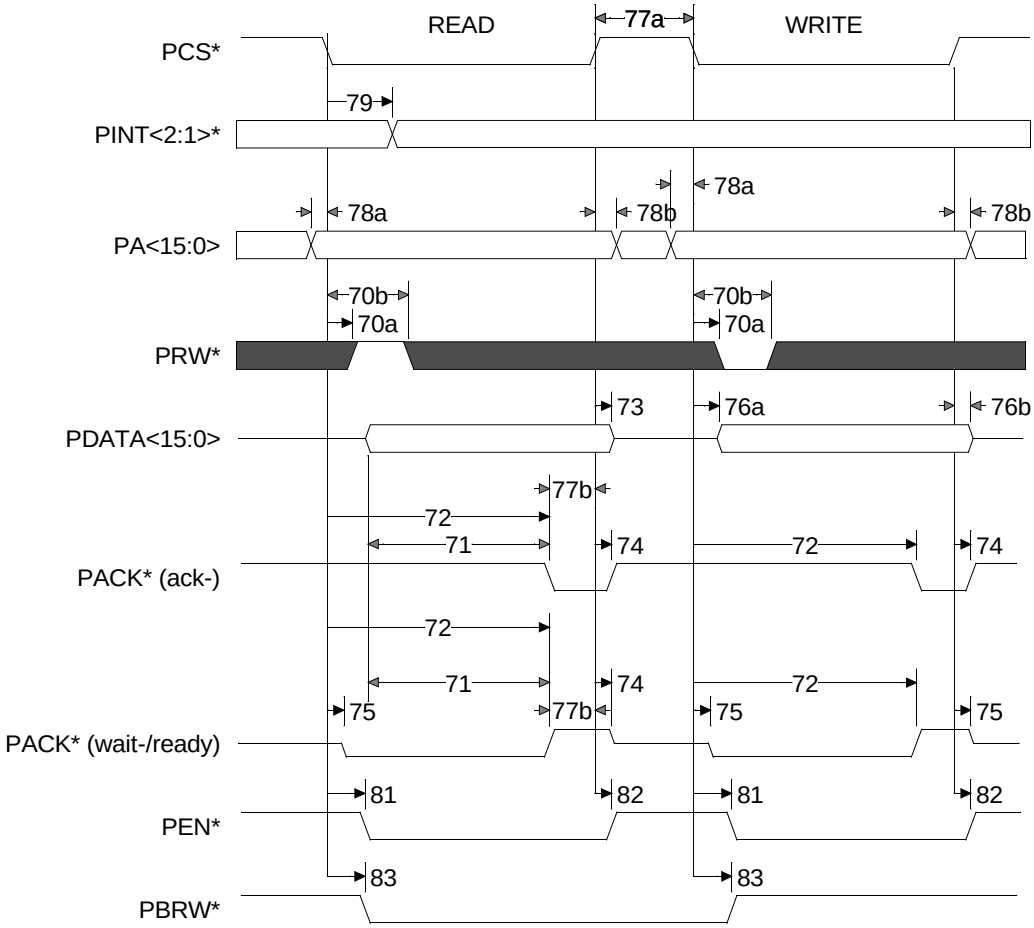


Figure 13-22: ENI Shared RAM & Register Cycle Timing
Refer to Table 13-13 for values.

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Numerics

A

B