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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+40
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-40-qinro-4

Chapter 1
Introduction

The NETsilicon NET+ARM chip is a single chip 32-bit RISC processor containing an integrated 10/100 Mbit Ethernet MAC and all the peripherals (other than RAM or ROM) required to complete an embedded networking peripheral application.

1.1 NET+ARM Chip Overview

CPU Core

- 32-bit RISC Processor
- 3rd Party Software Support
- 32-bit Internal Bus
- 2 Programmable Timers
- 2 Async Serial Ports
- 4K Cache (NET+40 only)

Bus Interface

- 8-bit, 16-bit, and 32-bit peripherals
- 28-bit External Address Bus
- Multi-master Support
- Normal and Burst Cycles
- 5 Programmable Chip-Selects
- Glueless Interface Flash & DRAM
- Configurable Endian Support

Integrated Ethernet Support

- 10/100 Mbit Media Access Controller MII Interface to External Ethernet PHY
- Bi-directional Capability
- Address Filtering
- Dedicated DMA Support

instruction is not executed – for example because a branch occurs while it is in the pipeline – the abort does not take place.

If a data abort occurs, the action taken depends on the instruction type:

1. Single data transfer instructions (LDR, STR) write back modified base registers; the Abort handler must be aware of this.
2. The swap instruction (SWP) is aborted as though it had not been executed.
3. Block data transfer instructions (LDW, STM) complete. If write-back is set, the base is updated. If the instruction would have overwritten the base with data (i.e. it has the base in the transfer list), the overwriting is prevented. All register overwriting is prevented after an abort is indicated, which means in particular that R15 (always the last register to be transferred) is preserved in an aborted LDM instruction.

The abort mechanism allows the implementation of a demand paged virtual memory system. In such a system the processor is allowed to generate arbitrary addresses. When the data at an address is unavailable, the Memory Management Unit (MMU) signals an abort. The abort handler must then work out the cause of the abort, make the requested data available, and retry the aborted instruction. The application program needs no knowledge of the amount of memory available to it, nor is its state in any way affected by the abort.

After fixing the reason for the abort, the handler should execute the following instructions irrespective of the state (ARM or THUMB):

```
SUBSPC, R14_abt, #4for a prefetch abort, or
SUBSPC, R14_abt, #8for a data abort
```

3.3.10 IRQ Exception

The IRQ (Interrupt Request) exception is a normal interrupt sourced by the NET+ARM Interrupt Controller. IRQ has a lower priority than FIRQ and is masked out when a FIRQ sequence is entered. It may be disabled at any time by setting the I bit in the CPSR to 1, though this can only be done from a privileged (non-User) mode.

Irrespective of whether the exception was entered from ARM or THUMB state, a FIRQ handler should leave the interrupt by executing

```
SUBSPC, R14_irq, #4
```

TAG Tag Reference

The TAG field identifies which memory location is currently stored within this cache entry. The TAG field is only valid when one of the four "V" valid bits are set to 1. The following formula can be used to calculate the actual physical address of the information for this cache entry.

physicalAddress =

```
(TAG << 10) || ((cacheAddress & 0x000007F8) >> 1)
```

INVALID Invalidate

0 - Location is value for cacheable entries

1- Location is invalid for any cache entries

The INVALID bit is used to prevent specific cache lines within a SET from being used for cache entries. The INVALID field is typically used to reserve cache entries for code that will be locked down in the cache at a later time.

LOCK Locked State

0 - Entry not locked

1- Entry locked in cache

The LOCK field is used to cause an entry to remain static within the cache. The LOCK field can be set to 1 in order to fix the current entry to remain in the cache SET forever. The LOCK bit is typically used to preload software functions in the cache.

V3 Byte 3 Valid

0 – Byte 3 is invalid

1 – Byte 3 is valid

The V3 bit is set to 1 to indicate that Byte 3 in this cache entry is valid. Byte 3 refers to the least significant address byte of a 32-bit word when operating in Big Endian mode, the most significant byte when operating in Little Endian mode.

V2 Byte 2 Valid

0 – Byte 2 is invalid

1 – Byte 2 is valid

The V2 bit is set to 1 to indicate that Byte 2 in this cache entry is valid.

V1 Byte 1 Valid

0 – Byte 1 is invalid

must be configured as an input and DREQ* and DACK* will act the same as in Fly-by mode.

If the Source Buffer Pointer points to NET+ARM memory, then the Destination Buffer Pointer must point to external device memory. The transfer will then be similar to a Fly-by Read, the DONE* must be configured as an output and DREQ* and DACK* will act the same as in Fly-by mode. In either direction the external device initiates the transfer by asserting DREQ* low, the NET+ARM will then take over and control the memory cycles.

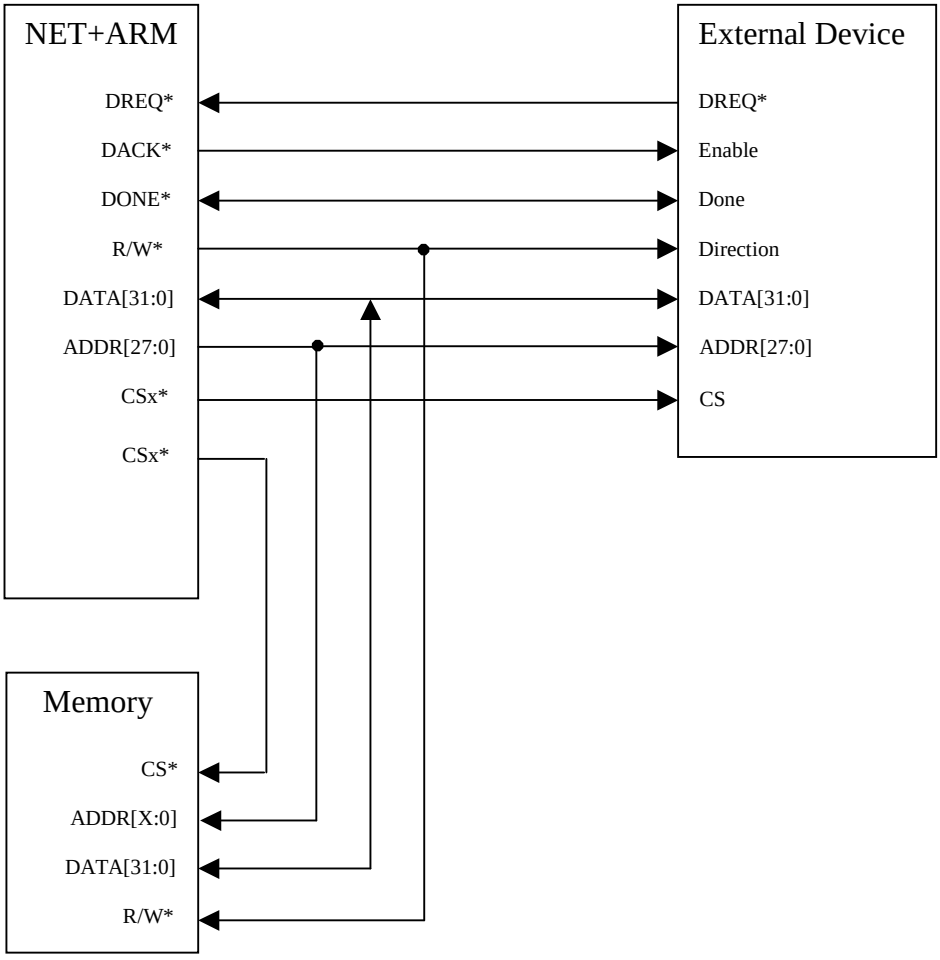

Figure 4-7: Hardware Needed for External Memory-to-Memory DMA Transfers

4.7 DMA Controller Reset

The entire DMA Controller Module can be reset without affecting any of the NET+ARM modules, by simply setting the DMA reset bit in the System Control Register to “1” and then back to “0.”

The DMA Controller Module is also reset by all forms of hardware and software resets.

```
 *  Description:
 *
 *     This routine creates a hash table based on the CRC values of
 *     the MAC addresses setup by eth_add_mca(). The CRC value of
 *     each MAC address is calculated and the lower six bits are used
 *     to generate a value between 0 and 64. The corresponding bit in
 *     the 64-bit hash table then set.
 *
 *  Parameters:
 *
 *     hash_table          pointer to buffer to store hash table in.
 *
 *  Return Values:
 *
 *     none
 *
 */

static void eth_make_hash_table (WORD16 *hash_table)

{
   int index;

   memset (hash_table, 0, 8);                /* clear hash table*/

   for (index = 0; index < mca_count; index++) /* for each mca address*/
   {
      set_hash_bit ((BYTE *) hash_table, calculate_hash_bit (mca_address [index]));
   }
}



/*
 *
 *  Function: void set_hash_bit (BYTE *table, int bit)
```

3. The host waits for the acknowledgment from the peripheral via an active BUSY.
4. The host drives AUTOFD* inactive high to acknowledge the peripheral.
5. The host drives STROBE* inactive and tri-states the DATA bus to end the EPP write cycle.
6. States 1 through 5 are repeated as necessary.

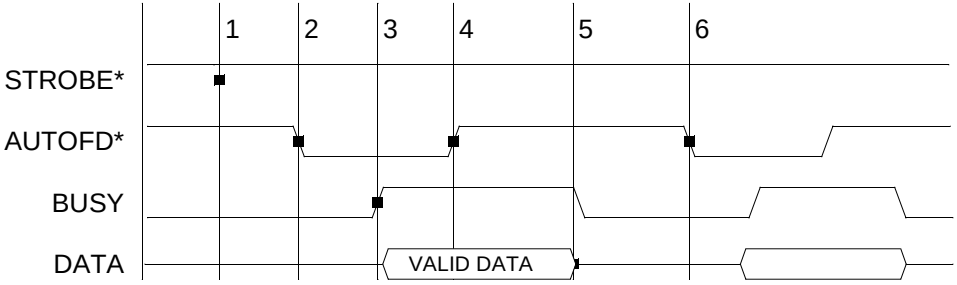

Figure 6-11: EPP Data Read Cycle

EPP Data Read Cycle:

1. NET+ARM chip bus master executes a read cycle from the EPP data byte address in the port data register. The Host asserts STROBE* high as a result. STROBE* high indicates a read cycle.
2. The AUTOFD* signal is asserted active since BUSY is inactive. The host does not assert AUTOFD* until BUSY is inactive.
3. The host waits for the acknowledgment from the peripheral via an active BUSY. The peripheral drives the data bus when BUSY is driven active.
4. The host drives AUTOFD* inactive high to acknowledge the peripheral. Read data is latched at this time.
5. The peripheral removes BUSY and tri-states the data bus.
6. States 1 through 5 are repeated as necessary.

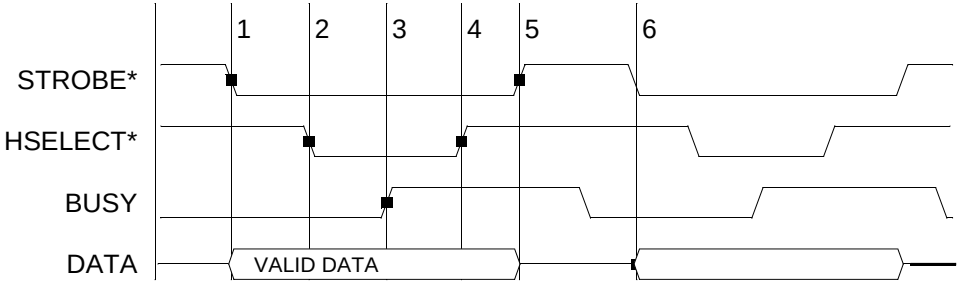

Figure 6-12: EPP Address Write Cycle

asserted. Setting FAST to 0 allows the external ENI interface to change PRW* slightly after PCS* or PDACK* are asserted.

DPACK* DMA PACK* Generation

0 = Drive PACK* active during DMA cycles

1 = Disable PACK* during DMA cycles

The DPACK* bit can be used to disable the assertion of PDACK* during DMA cycles. PDACK* should be disabled during DMA cycles when the external ENI interface is not designed to wait for PDACK* during DMA cycles.

PSIO PSIO Configuration for Shared Register

0 = Shared Register configured for NORMAL mode

1 = Shared Register configured for PSIO mode

The PSIO bit controls the bit formatting for the ENI shared register. Refer to Table 6-13. When the PSIO bit is set to 0, both the ARM processor and ENI interface use the same bit format for the shared register. When the PSIO bit is set to 1, the ENI Interface has an altered view of the ENI shared register as defined in Table 6-13. The default state for PSIO is established at bootstrap by sampling the A7 signal during reset. The inverted version of the A7 value is loaded into the PSIO configuration bit.

KYOINT Kyocera Interrupt Option

0 = Normal Interrupt Mode

1 = Kyocera Interrupt occurs when ENI interface writes to the most significant address of shared RAM.

The Kyocera interrupt option is an alternate mechanism for the ENI Interface to issue and interrupt to the ARM processor. When the KYOINT bit is set to 1, the ENI interface can issue an ARM interrupt by writing to the most significant word of shared RAM. The INTP* bit is set active low when the interrupt is issued. The KYOINT bit is a useful mechanism for generating an interrupt to the ARM processor when the ENI interface cannot address the shared register.

INTP* Interrupt Pending

The INTP* bit is set active low when the ENI Interface issues an interrupt to the ARM processor. The INTP* bit remains low until cleared by the ARM processor. The ARM processor clears the INTP* bit by writing a 1 to the same bit position in the ENI control register. An active low setting in INTP* causes an ARM processor interrupt when both IRQEN* (ENI control register) is set active low and ENI3 (GEN module interrupt enable register) is set active high.

This bit, when low, indicates that an interrupt from the ENI is pending. This bit is returned to the inactive 1 state by writing a 1 to this bit position.

The buffer GAP timer needs to be configured to allow any residual receive data bytes to be written into the receive FIFO. Either the buffer GAP timer or character GAP timer can be used. Using one of the GAP timers is only required when the size of the transmit data block is not a multiple of four bytes. If the size of the transmit data block is a multiple of 4, then the GAP timers are not required.

TRUN - 1 for enable
CT - user defined

4. Configure the Character GAP Timer:

   The character GAP timer needs to be configured to allow any residual receive data bytes to be written into the receive FIFO. Either the buffer GAP timer or character GAP timer can be used. Using one of the GAP timers is only required when the size of the transmit data block is not a multiple of four bytes. If the size of the transmit data block is a multiple of 4, then the GAP timers are not required.

   TRUN- 1 for enable
   CT - user defined

5. Configure control register B:

   RBGT- 1 To enable the buffer GAP timer
   RCGT- 1 To enable the character GAP timer
   MODE - “11” for slave mode
   BITORDR- user defined

6. Configure control register A:

   CE - 1 for enable
   WLS - “11” for 8-bit operation

to the same bit position in status register A. The RII status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

DSRI

The DSRI field indicates a state change in the EIA data set ready signal. When set, the DSRI field remains set until acknowledged. The DSRI bit is acknowledged by writing a 1 to the same bit position in status register A. The DSRI status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

CTSI

The CTSI field indicates a state change in the EIA clear to send signal. When set, the CTSI field remains set until acknowledged. The CTSI bit is acknowledged by writing a 1 to the same bit position in status register A. The CTSI status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

TRDY

The TRDY field indicates data can be written to the FIFO data register. The TRDY field is typically only used in interrupt driven applications, the TRDY field is not used for DMA operation. The TRDY status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

The TRDY bit is never active while the TBC-bit is active. The TBC bit must be acknowledged to activate the TRDY-bit. When the transmitter is configured to operate in DMA mode, the interlock between TBC and TRDY is handled automatically in hardware.

THALF

The THALF field indicates the transmit data FIFO contains room for at least 16 bytes. The THALF field is typically only used in interrupt driven applications, the THALF field is not used for DMA operation. The THALF status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

TBC

The transmit buffer closed (TBC) field indicates a transmit buffer closed condition. When set, the TBC field remains set until acknowledged. The TBC bit is acknowledged by writing a 1 to the same bit position in status register A. The TBC bit is automatically acknowledged by hardware when the transmitter is configured to operate in DMA mode. The TBC status condition can be programmed to generate an interrupt by setting the IE bit in control register A.

TBC is only used in HDLC applications. For HDLC applications, the TBC field indicates that bits D15:14 in status register B are valid. While the TBC field is active, the TRDY-bit is not active. To activate TRDY (to write to the data FIFO), the TBC bit

8.2.9 PORT C Register

The PORTC Register is used to configure the personality of each PORTC General Purpose I/O pin. Each of the eight PORTC GPIO pins can be individually programmed to be one of the following:

- General Purpose Input
- General Purpose Output
- Special Function Input
- Special Function Output

Table 8.4 – PORT C Configuration describes the possible configurations for each of the PORTC signals. Many, but not all, of the PORTC signals can be configured for Special Function. Note that this table has four basic columns, each column denoting one of the four possible configurations for each PORTC bit.

The eight bits in the MODE field determine which of the PORTC bits are configured for GPIO or Special Function.

General Purpose I/O

When a MODE bit is set to 0, the respective PORTC bit is configured for General Purpose I/O (GPIO).

When a PORTC MODE bit is set to 0, the respective bit in the DIR field is used to control the direction of the GPIO configuration; a DIR bit of 0 configures Input Mode while a DIR setting of 1 configures Output Mode.

When both MODE and DIR are set to 0, the PORTC bit is configured in Input Mode. The NET+ARM processor can read the current logic value on the PORTC bit by reading the state of the respective bit in the DATA field.

When the MODE bit is set to 0 and the DIR bit is set to 1, the PORTC bit is configured in Output Mode. The NET+ARM processor can set the current logic value on the PORTC bit by setting the state of the respective bit in the DATA field. Reading the DATA field when configured in Output Mode simply returns the current setting of the DATA field.

Special Function Mode

Many of the PORTC signals can be configured for Special Function I/O. Special Function Mode is used primarily for connecting the internal NET+ARM Serial Ports to the external interface pins; however, Special Function Mode also provides other miscellaneous features.

When the PORTC MODE bit is set to 1 and the PORTC DIR bit is set to 0, the PORTC bit is configured to operate in Special Function Input Mode. When the

8.2.11 Interrupt Enable Register - Set

The Interrupt Enable - Set register is a 32-bit write-only register. This register sets specific bits without affecting the other bits. Writing a one to a bit position in this register sets the respective bit in the Interrupt Enable Register. A zero in any bit position has no affect.

Address = FFB0 0034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA1	DMA2	DMA3	DMA4	DMA5	DMA6	DMA7	DMA	DMA9	DMA10	ENI PORT 1	ENI PORT 2	ENI PORT 3	ENI PORT 4	ENET RX	ENET TX
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER 1 RX	SER 1 TX	SER2 RX	SER 2 TX	—	—	—	—	—	Watch Dog	Timer 1	Timer 2	PortC PC3	PortC PC2	PortC PC1	PortC PC0
RESET:															
0	0	0	0						0	0	0	0	0	0	0
R/W	R/W	R/W	R/W						R/W	R/W	R/W	R/W	R/W	R/W	R/W

8.2.12 Interrupt Enable Register - Clear

The Interrupt Enable - Clear register is a 32-bit write-only register. This register clears specific bits without affecting the other bits. Writing a 1 to a bit position in this register clears the respective bit in the Interrupt Enable Register. A zero in any bit position has no affect.

Address = FFB0 0038

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DMA1	DMA2	DMA3	DMA4	DMA5	DMA6	DMA7	DMA	DMA9	DMA10	ENI PORT 1	ENI PORT 2	ENI PORT 3	ENI PORT 4	ENET RX	ENET TX
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SER 1 RX	SER 1 TX	SER2 RX	SER 2 TX	—	—	—	—	—	Watch Dog	Timer 1	Timer 2	PortC PC3	PortC PC2	PortC PC1	PortC PC0
RESET:															
0	0	0	0						0	0	0	0	0	0	0
R/W	R/W	R/W	R/W						R/W	R/W	R/W	R/W	R/W	R/W	R/W

ADDR[06]	:	ENI ControlWR_OC (see Section *6.5.10 ENI Control Register*)
ADDR[05]	:	ENI ControlDINT2* (see Section *6.5.10 ENI Control Register*)
ADDR[04]	:	ENI Control I_OC (see Section *6.5.10 ENI Control Register*)
ADDR[03]	:	ENI Control DMAE* (see Section *6.5.10 ENI Control Register*)
ADDR[02]	:	Reserved (see Section *6.5.10 ENI Control Register*)
ADDR[01]	:	ENI ControlEPACK* (see Section *6.5.10 ENI Control Register*)
ADDR[00]	:	ENI ControlPULINT* (see Section *6.5.2 General Control Register*)

Note: The inverted PSIO address bit (ADDR7) is loaded into the PSIO configuration bit within the ENI Control Register. In the ENI Control Register, 0=Normal, 1=PSIO).

Note: The inverted ENDIAN bit (ADDR27) is loaded into the LENDIAN bit within the System Control Register. In the System Control Register, LENDIAN=1 (for little endian mode) and LENDIAN=0 (for big endian mode).

12.1 ATPG

The NET+ARM chip supports ATPG testing using the full-scan methodology. The NET+ARM chip uses multiple scan chains. The scan chains propagate from primary inputs to primary outputs. Scan testing is enabled when SCANEN* is defined in its active low state.

During scan testing on a tester, the PLL must be disabled such that the tester has direct control of the system clock. The PLLTST* signal, when pulled active low, allows the PLL to be bypassed and all system clocks to be provided by the XTAL1 primary input.

Scan Chain	PLLTST*	BISTEN*	SCANEN*	Input	Output
Chain 1	0	0	0	PA0	PORTA0
Chain 2	0	0	0	PA1	PORTA1
Chain 3	0	0	0	PA2	PORTA2
Chain 4	0	0	0	PA3	PORTA3
Chain 5	0	0	0	PA4	PORTA4
Chain 6	0	0	0	PA5	PORTA5
Chain 7	0	0	0	PA6	PORTA6
Chain 8	0	0	0	PA7	PORTA7
Chain 9	0	0	0	PA8	PORTB0
Chain 10	0	0	0	PA9	PORTB1
Chain 11	0	0	0	PA10	PORTB2
Chain 12	0	0	0	PA11	PORTB3
Chain 13	0	0	0	PA12	PORTB4
Chain 14	0	0	0	PA13	PORTB5
Chain 15	0	0	0	PA14	PORTB6
Chain 16	0	0	0	PA15	PORTB7

Table 12-2: ATPG Test Mode Connections

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	Type: S2, I_{OL} = 2 mA;	0		0.4	V
		Type: S4, I_{OL} = 4 mA;	0		0.4	V
		Type: S8, I_{OL} = 8 mA;	0		0.4	V
V_{OH}	Output High Voltage	Type: S2, I_{OH} = 2 mA;	2.4		V_{DD}	V
		Type: S4, I_{OH} = 4 mA;	2.4		V_{DD}	V
		Type: S8, I_{OH} = 8 mA;	2.4		V_{DD}	V
P_D	Power Dissipation	NET+15			500	mW
P_D	Power Dissipation	NET+40			750	mW
I_{OZ}	High-Z Leakage Current	V_{PAD}=3.6V, V_{PAD}=0V	-5 -5		+5	uA uA
C_{OUT}	Output Capacitance				10	pF
C_{IO}	Input/Output Capacitance	Any I/O			15	pF
C_L	Output Load Capacitance	BCLK, TA*, TEA*, BR*, BG*			20	pF
		BUSY*, CSO-4*, MDC, MDIO			20	pF
		TXD3-0, TXER, TXEN, PEN*			20	pF
		PBRW*, TDO			20	pF
		BE3-0*, RW*, CAS3-0*, WE*			30	pF
		OE*			30	pF
		ADDR, DATA, TS*, PDATA			50	pF
		PACK*, PINT1*, PINT2*			50	pF
		PA13, PA14, PORTA, PORTB			50	pF
		PORTC			50	pF

Table 13-4: DC Characteristics - Outputs

Num	Characteristic	Min	Max	Unit
50	BCLK High to DACK* valid		12	ns
51	BCLK High to DONE* (output) valid	0	12	ns
52	DACK* low to DREQ* high (hold)	0		ns
53a	DREQ* valid to BCLK high (setup)	11		ns
53b	BCLK high to DREQ* valid (hold)	0		
54a	DONE* (input) valid to BCLK high (setup)	9		ns
54b	BCLK high to DONE* (input) valid (hold)	0		ns

Table 13-11: External DMA Timing

Num	Characteristic	Min	Max	Unit
60a	RW* valid to BCLK high (setup)	10		ns
60b	BCLK high to RW* invalid (hold)	0		ns
61a	BE* valid to BCLK high (setup)	8		ns
61b	BCLK high to BE* invalid (hold)	0		ns
62a	Address valid to BCLK high (setup)	8		ns
62b	BCLK high to Address invalid (hold)	0		ns
63a	BCLK high to Read Data valid	6	12	ns
63b	BCLK high to Data High Impedance	14	26	ns
64a	Data In valid to BCLK high (setup)	14		ns
64b	BCLK high to Data In invalid (hold)	0		ns
65a	A25/BLAST* valid to BCLK (T2) high (setup)	10		ns
65b	BCLK (T2) high to A25/BLAST* invalid (hold)	0		ns

Table 13-12: External Bus Master Timing

Num	Characteristic	Min	Max	Unit
115	DATA valid to STROBE* low (setup)	STROBE		ns
116	STROBE* width low	STROBE		ns
117	STROBE* low to BUSY (input) high	0		ns
119	BUSY low to DATA change (hold)	3 * T_{sys}		ns
120	STROBE* high to DATA change (hold)	STROBE		ns

Table 13-17: 1284 Compatibility SLOW Mode Timing (FAST = 0)

Num	Characteristic	Min	Max	Unit
115	DATA valid to STROBE* low (setup)	STROBE		ns
116	STROBE* width low	STROBE		ns
117	STROBE* low to BUSY (input) high	0		ns
119	BUSY low to DATA change (hold)	3 * T_{sys}		ns
120	STROBE* high to DATA change (hold)	3 * T_{sys}		ns

Table 13-18: 1284 Compatibility FAST Mode Timing (FAST = 1)

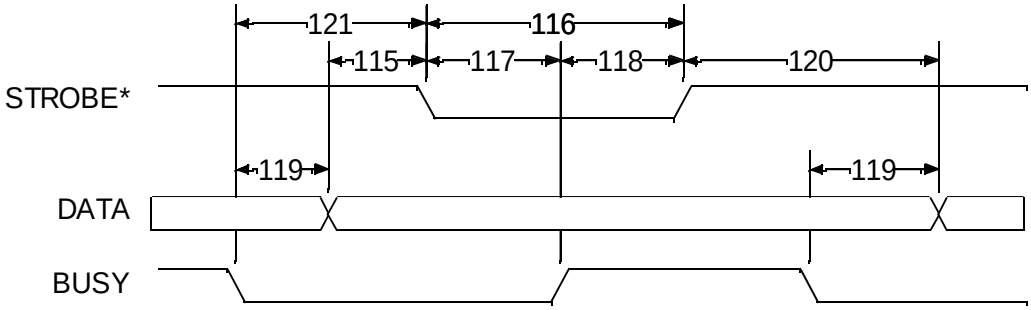

Figure 13-30: 1284 Compatibility Mode Timing

Refer to Tables 13-17 and 13-18 for values.

The table below specifies the dimensions for the NET+ARM chip.

208 Lead - All Dimensions are in millimeters			
	Minimum	**Nominal**	**Maximum**
A	3.22	3.57	3.97
A1	0.05	0.25	0.50
A2	3.17	3.32	3.47
D	30.95	31.20	31.45
D1	27.90	28.00	28.10
E	30.95	31.20	31.45
E1	27.90	28.00	28.10
L	0.35	0.50	0.65
P		0.50	
B	0.10	0.20	0.30

Table 14-1: NET+ARM Chip Dimensions