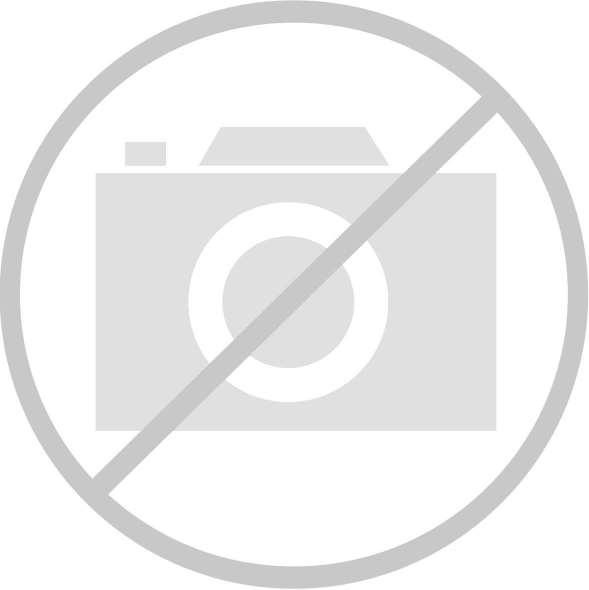
Digi - NET+40-QIVRO-4 Datasheet



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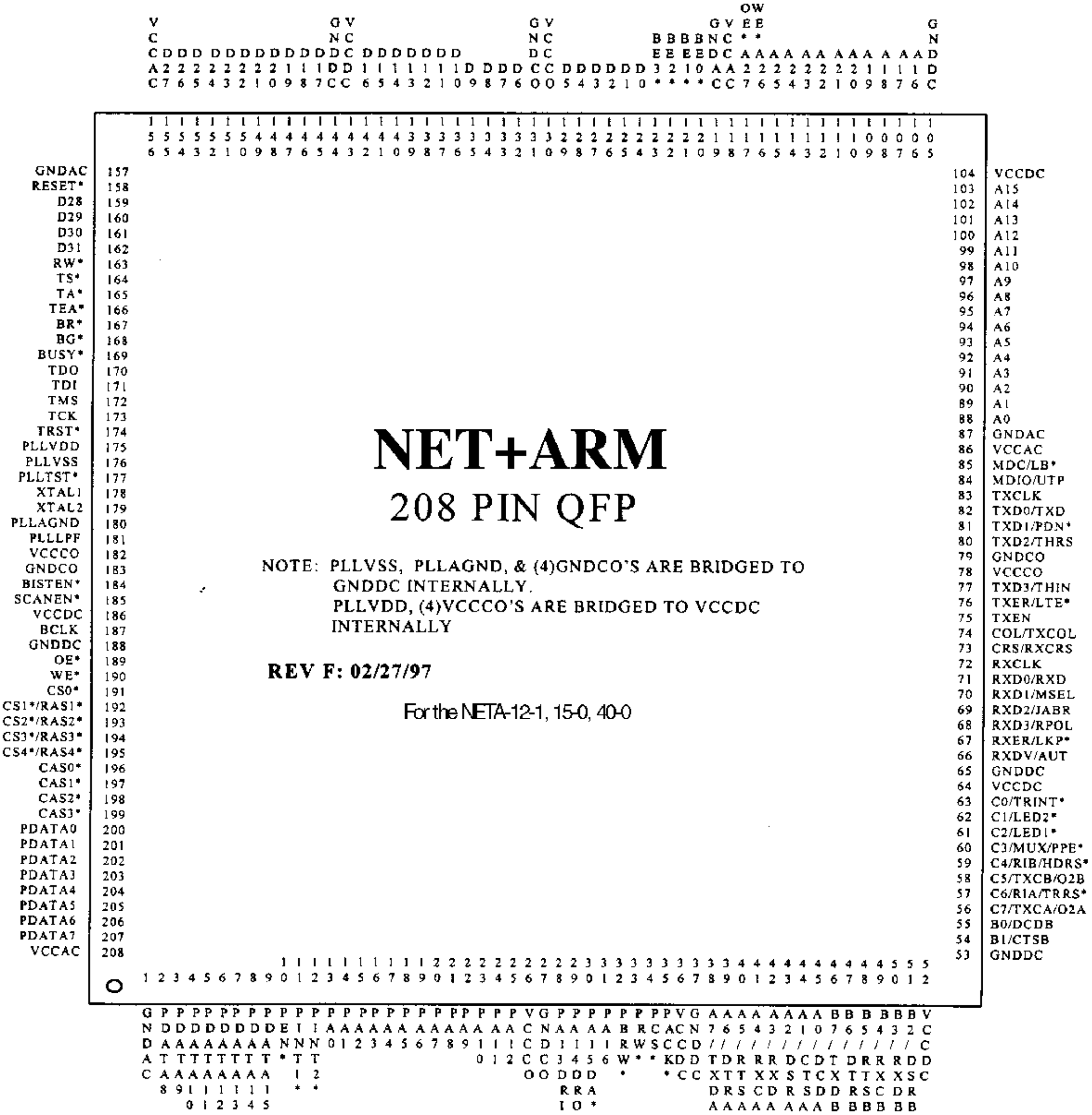
What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	NET+40
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, HDLC, IEEE1284/ENI, SPI, UART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/net-40-qivro-4

1.4 NET+ARM Chip Pinout

Refer to Table 1-1 for details concerning the pinout of the NET+ARM chip.



NOTE: PLLVSS, PLLAGND, & (4)GNDCO'S ARE BRIDGED TO GNDDC INTERNALLY.
PLLVDD, (4)VCCCO'S ARE BRIDGED TO VCCDC INTERNALLY

REV F: 02/27/97

For the NETA-12-1, 15-0, 40-0

Figure 1-3: NET+ARM Chip Pinout

BUSY*   Bus Busy

The bus busy signal is asserted active low by the current bus master to indicate it has assumed ownership of the system bus. The current bus master relinquishes ownership of the system bus by driving the BUSY* signal inactive high. The BUSY* signal is a bi-directional signal for the NET+ARM chip.

CS0*   Chip Select 0

CS1*   Chip Select 1

CS2*   Chip Select 2

CS3*   Chip Select 3

CS4*   Chip Select 4

The NET+ARM chip supports five unique chip select outputs. Each chip select can be configured to decode a portion of the available address space and can address a maximum of 256M bytes of address space. The chip selects are configured using registers in the memory module.

CS0* is unique in that it can be configured via bootstrap configurations to be enabled at powerup. This allows the ARM processor to boot from a Flash or EPROM device attached to CS0*.

CAS0*   Column Address Strobe

CAS1*

CAS2*

CAS3*

The CAS* signals are activated when an address is decoded by a chip select module that is configured for DRAM mode. The CAS* signals are active low and provide the column address strobe function for DRAM devices.

The CAS* signals also identify which 8-bit bytes of the 32-bit data bus are active during any given system bus memory cycle.

The following chart identifies the relationship between the CAS* signals and the data bus lanes.

RESET* System Reset

The RESET* input resets the NET+ARM chip hardware. A valid RESET* input must be issued for a minimum of 40ms after power reaches 3.0 volts. A RESET* input can be issued at any time to reset the NET+ARM chip.

1.5.8 Test Support

PLLTST* PLL Test and Disable

When driven active low, the PLLTST* input disables the internal PLL. The operating clock for the NET+ARM chip is based upon a TTL clock input attached to the XTAL1 pin. The PLLTST* pin must be left unconnected or driven high to enable the crystal oscillator and internal PLL.

BISTEN* BIST Enable

The BISTEN* pin is used for testing purposes only. It should always be left unconnected or driven high.

SCANEN* SCAN Enable

The SCANEN* pin is used for testing purposes only. It should always be left unconnected or driven high.

1.5.9 ARM Debugger

There are five pins that provide a dedicated connection to the internal ARM processor core. These five signals only connect to the ARM processor and are used for software development using the ARM Embedded ICE module (or similar device). These five signals should not be confused with 1149.1 JTAG Testing.

TDI

TDO

TMS

TRST*

TCK

Note: TRST* must be pulsed active low after power up.

1.5.10 Power

VCCAC Power A/C Switching

Vector Address	Vector	Description
0x0	RESET	Reset Vector; for initialization and startup
0x4	Undefined	Undefined Instruction Encountered
0x8	SWI	Software Interrupt; used for entry point into the kernel
0xC	Abort (Prefetch)	Bus Error (no response or error) fetching instructions
0x10	Abort (Data)	Bus Error (no response or error) fetching data
0x14	Reserved	Reserved
0x18	IRQ	Interrupt from NET+ARM Interrupt Controller
0x1C	FIRQ	Fast Interrupt from NET+ARM Interrupt Controller

Table 3-2: Exception Vector Table

All internal NET+ARM peripheral interrupts are presented to the CPU using the IRQ or FIRQ interrupt inputs. The ARM has the ability to mask various NET+ARM peripheral interrupts at the global level using the NET+ARM Interrupt Controller. Furthermore, the ARM has the ability to mask interrupts at the micro-level using configuration features with the peripheral modules.

All IRQ interrupts are disabled when the “I” bit is set in the ARM CPSR register. When the “I” bit is cleared, those interrupts enabled in the NET+ARM Interrupt Controller are allowed to assert the IRQ input to the ARM processor.

Upon entering an interrupt, the “I” bit is automatically set by the ARM processor. This disables recursive interrupts. The first task of the Interrupt Service Routine (ISR) is to read the interrupt status register. This register identifies all active sources for the IRQ interrupt. Firmware can prioritize which interrupt should be serviced by using the bits defined in the interrupt status register.

3.3.2 Action on Entering an Exception

When handling an exception, the ARM7TDMI:

Return/ Exception	Return Instruction	Previous State ARM R14_x	Previous State THUMB R14_x	Notes
BL	MOV PC, R14	PC + 4	PC + 2	1
RESET	NA	—	—	4
UNDEF	MOVS PC, R14_und	PC + 4	PC + 2	1
SWI	MOVS PC, R14_svc	PC + 4	PC + 2	1
ABORT P	SUBS PC, R14_abt, #4	PC + 4	PC + 4	1
ABORT D	SUBS PC, R14_abt, #8	PC + 8	PC + 8	3
IRQ	SUBS PC, R14_irq, #4	PC + 4	PC + 4	2
FIRQ	SUBS PC, R14_firq, #4	PC + 4	PC + 4	2

Table 3-3: Exception Entry / Exit

Notes:

1. Where PC is the address of the BL/SWI/Undefined Instruction fetch that had the prefetch abort.
2. Where PC is the address of the instruction that did not get executed since the FIRQ or IRQ took priority.
3. Where PC is the address of the Load or Store instruction that generated the data abort.
4. The value saved in R14_svc upon reset is unpredictable.

3.3.5 Reset Exception

When the ARM7TDMI is held in reset, the ARM7TDMI abandons the executing instruction and then continues to fetch instructions from incrementing word addresses.

When the ARM7TDMI is removed from reset, the ARM7TDMI:

1. Overwrites R14_svc and SPSR_svc by copying the current values of the PC and CPSR into them. The value of the saved PC and SPSR is not defined.
2. Forces the CPSR M field to 10011 (Supervisor mode), sets the I and F bits in the CPSR, and clears the CPSR T bit (back to ARM mode).

3. Forces the PC to fetch the next instruction from address 0x00.
4. Execution resumes in ARM state.

3.3.6 Undefined Exception

When the ARM7TDMI comes across an instruction that it cannot handle, it takes the undefined instruction trap. This mechanism may be used to extend either the THUMB or ARM instruction set by software emulation.

After emulating the failed instruction, the trap handler should execute the following instruction irrespective of the state (ARM or THUMB):

```
MOVS PC, R14_und
```

This restores the PC and CPSR, and returns to the instruction following the undefined instruction.

3.3.7 SWI Exception

The software interrupt instruction (SWI) is used for entering Supervisor mode, usually to request a particular supervisor function. A SWI handler should return by executing the following instruction irrespective of the state (ARM or THUMB):

```
MOVS PC, R14_svc
```

This restores the PC and CPSR, and returns to the instruction following the SWI.

3.3.8 Abort Exception

An abort indicates that the current memory access cannot be completed. It can be signaled by the external ABORT input. The ARM7TDMI checks for the abort exception during memory access cycles.

There are two types of abort:

Prefetch Abort	occurs during an instruction prefetch
Data Abort	occurs during a data operand access

If a prefetch abort occurs, the prefetched instruction is marked as invalid, but the exception will not be taken until the instruction reaches the head of the pipeline. If the

Interrupt sources include DMA channels 1-10, ENI, Ethernet receive and transmit, serial port receive and transmit, watchdog timer, timers 1 and 2, and 4 pins on Port C. Each of these sources is enabled/disabled within their respective module (and sub-modules) within the NET+ARM ASIC, however, the interrupt controller in the GEN module does not latch any of the interrupt signals

Note: Causes of interrupts are latched in their respective sub-module until cleared.

The specific interrupts that each source is capable of generating are outlined below:

3.3.14 DMA Interrupts

All of the DMA channels, including the four sub-channels of the Ethernet receiver, have four possible sources of interrupts. These are found in the DMA status/interrupt enable register (starting 0xFF90 0014) in Section *4.4.3 DMA Status/Interrupt Enable Register*. Under normal operations, only the NCIP and NRIP interrupts are used; the other interrupts would indicate a catastrophic failure. The interrupts are acknowledged by writing a “1” to the register location. This resets the interrupt condition.

5.3.2 Ethernet General Status Register

The Ethernet General Status Register is a 32-bit register. The register bit assignments are defined as follows:

Address = FF80 0004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
—	—	RXFDB		RXREGR	RXFIFOH	RXBR	RXSKIP	—	—	—	—	TXREGE	TXFIFOH	TXBC	TXFIFOE
RESET:															
		0		0	0	0	0					0	0	0	0
		R		R	R	R/C	R/W					R	R	R/C	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FullDuplex	—	MANSENSE	AUD_TP	LINKPUL*	ATUOMAN	—	—	—	—	—	—	—	—	—	—
RESET:															
0		0	0	0	0										
R		R	R	R	R										

RXFDB **Receive FIFO Data Bytes Available**

This field must be used in conjunction with RXREGR. When RXREGR is set, this field identifies how many bytes are available in the receive data register. The RXFDB field is only used when operating the Ethernet receiver in interrupt service mode instead of DMA mode. In general, DMA mode is more desirable and the RXFDB can usually be ignored.

RXREGR **Receive Register Ready**

The RXREGR bit is set whenever data is available to be read from the FIFO data register. This bit, when active high, can cause an interrupt to occur when the ERXREGR bit is set. The RXREGR bit is never active while RXBR is set. The RXBR bit must be cleared to activate RXREGR. The RXREGR bit is only used when operating the Ethernet receiver in interrupt service mode instead of DMA mode. In general, DMA mode is more desirable and the RXREGR bit can usually be ignored.

RXFIFOH **Receive FIFO Half Full**

The RXFIFOH bit is set whenever the receive FIFO is at least half full (> 1024 bytes). This bit, when active high, can cause an interrupt to occur when the ERFIFOH bit is set. The RXFIFOH bit is only used when operating the Ethernet receiver in interrupt service mode instead of DMA mode. In general, DMA mode is more desirable and the RXFIFOH bit can usually be ignored.

RXBR **Receive Buffer Ready**

TXFIFOH **Transmit FIFO Half Empty**

The TXFIFOH bit is set whenever the transmit FIFO is at least half empty (< 64 bytes). This bit, when active high, can cause an interrupt to occur when the ETFIFOH bit is set. The TXFIFOH bit is only used when operating the Ethernet receiver in interrupt service mode instead of DMA mode. In general, DMA mode is more desirable and the TXFIFOH bit can usually be ignored.

TXBC **Transmit Buffer Complete**

The TXBC bit is set whenever packet transmission has completed. This bit, when active high, can cause an interrupt to occur when the ETXBC bit is set. The TXBC bit is an indication to the interrupt service routine to read the transmit status register. After the transmit status register is read, the TXBC bit can be cleared by writing a 1 to the TXBC bit position in the EGSR. After the TXBC bit is cleared, the TXREGE and TXFIFOH bits become active. The TXBC bit is only used when operating the Ethernet receiver in interrupt service mode instead of DMA mode. In general, DMA mode is more desirable and the TXBR bit can usually be ignored. While operating in DMA mode, the TXBC is automatically cleared by the DMA controller.

TXFIFOE **Transmit FIFO Empty**

The TXFIFOE bit is active whenever the Transmit FIFO is empty.

D15:D0 **ENDEC Media Status Bits**

The least significant 16 bits of the EGSR are only used when the MODE field is configured for ENDEC mode. In this configuration, various NET+ARM chip signals are reconfigured to provide simple status inputs. The status inputs can be used to monitor status signals on the external ENDEC PHY device.

Table 5-3 shows the relationship between the lower bits in the EGSR and the NET+ARM chip pin, which they monitor. The NET+ARM chip pins can only be monitored when the MODE field is configured for ENDEC mode.

Data Bit	Signal Name	NET+ARM Pin
D15	FullDuplex	RXD2
D13	Mansense	RXD1
D12	AUI_TP	RXD3
D11	LINKPUL*	RXER
D10	Automan	RXDV

Table 5-3: ENDEC Status Sign Cross-Reference

5.3.16.2 Alignment Error Counter

The alignment error counter is incremented each time a receive frame is discarded because it was received with an alignment error.

Address = FF80 044C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RESET:															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXAEC															
RESET:															
0															
R															

RXAEC

The RXAEC counter is incremented each time a packet is received with an alignment (dribble bit) error. The packet is automatically discarded if the ERXBAD field in the General Control Register is set to 0. This counter will increment for each packet received with an alignment condition regardless of the value in the ERXBAD field. The counter is automatically cleared when read provided the AUTOZ bit is set in the STL Configuration Register.

5.3.16.3 Code Error Counter

The code error counter is incremented each time a receive frame is discarded because it was received with a coding error.

Address = FF80 0588

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RESET:															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXCEC															
RESET:															
0															
R															

RXCEC

The RXCEC counter is incremented each time a packet is received with a coding error. A coding error occurs when the PHY asserts the RXER input to the NET+ARM

TXMCR

The TXMCR counter is incremented each time a packet transmission is aborted because it received too many collisions. The maximum number of allowable collisions is defined by the RETRY field in the Collision Window / Collision Retry Register. The counter is automatically cleared when read provided the AUTOZ bit is set in the STL Configuration Register.

The RPSF* signal is driven active low by the NET+ARM chip to identify the beginning of each Ethernet packet being transferred from the Ethernet PHY to the NET+ARM chip internal MAC. The RPSF* signal is driven active low while the fifth nibble is being transferred. The external CAM hardware must monitor the MII receive interface between the PHY and MAC waiting for the RPSF* assertion. When RPSF* is asserted, the CAM hardware can then extract the destination address field from the MII receive bus.

After performing the necessary destination address lookup, the incoming packet can be rejected by the CAM filtering hardware by simply asserting the REJECT* input active low during any nibble-time between RPSF* assertion and nibble number 128.

Figure 5-2 shows the timing relationship between the RPSF*, REJECT*, and MII receive interface signals. In this example, the MII receive interface is transferring a packet whose first 6 nibbles have the values 1,2,3,4,5, and 6. Notice that the RPSF* signal is activated while the fifth nibble is being transferred from the MII (nibbles are transferred in Little Endian order within a BYTE).

The external CAM hardware uses the RPSF* signal to find the alignment for the destination address. After the lookup is performed, the CAM hardware can assert the REJECT* signal to discard the frame. The REJECT* signal can be asserted during any RXCLK cycle between when RPSF* is asserted and nibble number 128.

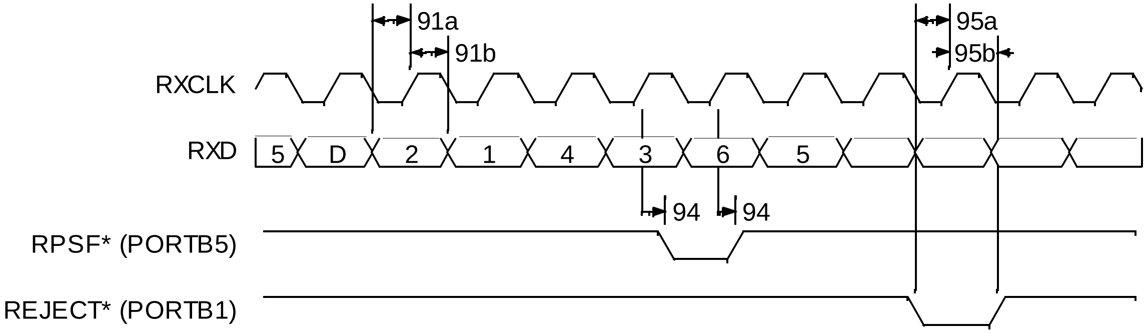


Figure 5-2: External Ethernet CAM Filtering

remain in the FIFO and stall the completion of the receive data buffer.

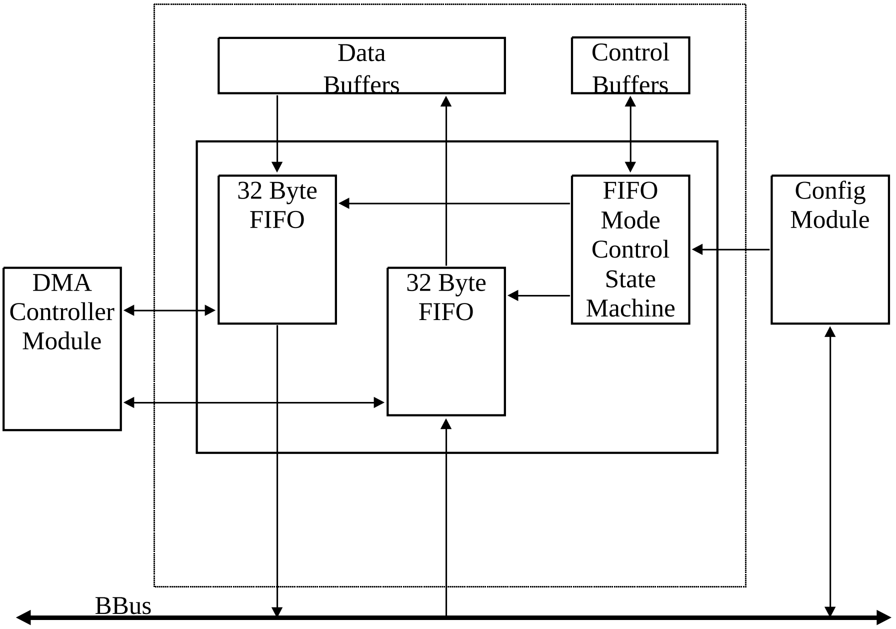


Figure 6-15: ENI FIFO Mode Block Diagram

6.6.7 FIFO Data Register

The FIFO data register is only accessible from the ENI interface when the ENI controller is configured to operate in ENI FIFO mode.

The FIFO data register passes data between the NET+ARM chip and the ENI controller. The RDBUFRDY* and WRBUFEMP* flags in the mask/status register are used to identify the current state of the ENI FIFO mode data register. The FIFO Data Register must only be written when the WRBUFEMP* status bit in the FIFO Mask/Status Register is active low. The FIFO Data Register can only be read when the RDBUFRDY* status bit in the FIFO Mask/Status Register is active low.

The data register can be memory mapped, using the PCS* select input, whose address is defined in Table 6-12. The memory mapped data register can be used in polled or interrupt-driven applications. The memory mapped data register can also be used in DMA applications that use the dual address, or memory-to-memory DMA operations. The dual address (or memory-to-memory) method requires two bus cycles per DMA operation; one bus cycle to access the data register and another bus cycle to access the RAM on the controller board.

The data register can also be DMA mapped using the PDACK* input. When using the PDACK* input, all ENI address inputs are ignored. Furthermore, the sense of PRW* is reversed. For DMA operations, PRW* high writes to the data register (read from controller memory), PRW* low reads from the data register (write to controller memory). The DMA mapped interface is designed for use in single address, or fly-by DMA operations. The single address (or fly-by) method requires a single bus cycle per DMA operation. The memory is simply accessed (read or write) on the controller. During DMA memory accesses, the PDACK* signal is asserted to the ENI interface. During DMA cycles, a PRW* high signal instructs the ENI interface to accept FIFO data from the controller, a PRW* low signal instructs the ENI interface to provide FIFO data to the controller.

The FIFO mode data register can be configured using an 8- or 16-bit interface. When configured for 8-bit operation, only the upper 8 data bits, PDATA(15:8), are used.

Unlike accessing Shared RAM, when accessing the FIFO Data Register from the external ENI interface, the access timing is always the same. The ENI hardware does not need to arbitrate with internal resources when accessing the FIFO Data Register. As such, the access timing for the FIFO Data Register is fast and consistent.

Address = FFD0 001C / 5C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RDMB1								RDMB2							
RESET:	0								0							
	R/W								R/W							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMB3								RDMB4							
RESET:	0								0							
	R/W								R/W							

7.5.10 Receive Match MASK Register

The receive match MASK register masks those bits in the receive match DATA register that should NOT be included in the match comparison. To mask a bit in the match comparison function, place a 1 in the same bit position within this register.

Address = FFD0 0020 / 60

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RMMB1								RMMB2							
RESET:	0								0							
	R/W								R/W							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RMMB3								RMMB4							
RESET:	0								0							
	R/W								R/W							

7.5.11 Control Register C (HDLC)

Control register C provides the configuration bits required when the serial channel is configured to operate in HDLC mode.

Address = FFD0 0024 / 64

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NFLAG				—	—	—	—	CRC		RXCRC	CHKCRC*	—	—	TXCRC*	FLAG*/IDL
RESET:	0								0		0	0			0	0
	R/W								R/W		R/W	R/W			R/W	R/W

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RESET:																

the SER Module configuration controls the state of OUT1. The OUT1 signal configuration is active high inside the NET+ARM and active low outside the NET+ARM. The GEN Module performs inversion before driving the PORTB4 I/O pad.

The PORTB4 bit can be configured for Special Function Input. When configured for Special Function Input, PORTB4 provides one of 2 Serial Channel B features, depending upon the configuration of the Serial Channel.

When the Serial Channel is configured for SPI Slave mode, PORTB4 Special Function Input receives the SPI Slave clock signal from the PORTB4 pin.

When the RXSRC bit is set to 1 in the Serial Channel Bit-Rate Register, then the Serial Channel Receiver Clock will be accepted from the PORTB4 pin.

PORTB3

The PORTB3 bit can be configured for GPIO Input mode or GPIO Output Mode.

The PORTB3 bit has no useful function when configured to operate in Special Function Output mode.

The PORTB3 bit can be configured for Special Function Input. When configured for Special Function Input, the PORTB3 signal provides the Receive Data (RXD) signal for Serial PORT B. The RXD signal is used for Serial Receive Data when configured to operate in UART, SPI, or HDLC modes.

PORTB2

The PORTB2 bit can be configured for GPIO Input mode or GPIO Output Mode.

The PORTB2 bit can be configured for Special Function Output. When configured for Special Function Output, the PORTB5 signal provides the active low DMA Acknowledge signal for DMA Channel 4. The DMA Acknowledge signal is driven active low when DMA Channel 4 is performing an external DMA cycle. The DMA Acknowledge is only used when the REQ bit is set in DMA Channel 4 Control Register.

The PORTB2 bit can be configured for Special Function Input. When configured for Special Function Input, the PORTB2 signal provides the Data Set Ready (DSR) signal for Serial PORT B. Status Register A within the SER Module configuration returns the state of RTS. The RTS signal status is active high inside the NET+ARM and active low outside the NET+ARM. The GEN Module performs inversion after receiving the PORTB2 I/O pad.

PORTB1

The PORTB1 bit can be configured for GPIO Input mode or GPIO Output Mode.

WATCH DOG

The WATCH DOG bit position corresponds to an interrupt condition sourced by the watchdog timer. Please refer to Section *8.2.1 System Control Register* for more details regarding the watchdog timer.

TIMER 1

The TIMER 1 bit position corresponds to an interrupt condition sourced by the TIMER 1 module. Please refer to Section *8.2.6 Timer Status Register* for more details on timer interrupts.

TIMER 2

The TIMER 2 bit position corresponds to an interrupt condition sourced by the TIMER 2 module. Please refer to Section *8.2.6 Timer Status Register* for more details on timer interrupts.

PORTC PC3

The PORTC PC3 bit position corresponds to an interrupt condition caused by an edge transition detected on the PORTC3 pin. Please refer to Section *8.2.9 PORT C Register* for more information regarding the PORTC edge detection interrupts.

PORTC PC2

The PORTC PC2 bit position corresponds to an interrupt condition caused by an edge transition detected on the PORTC2 pin. Please refer to Section *8.2.9 PORT C Register* for more information regarding the PORTC edge detection interrupts.

PORTC PC1

The PORTC PC1 bit position corresponds to an interrupt condition caused by an edge transition detected on the PORTC1 pin. Please refer to *8.2.9 PORT C Register* for more information regarding the PORTC edge detection interrupts.

PORTC PC0

The PORTC PC0 bit position corresponds to an interrupt condition caused by an edge transition detected on the PORTC0 pin. Please refer to Section *8.2.9 PORT C Register* for more information regarding the PORTC edge detection interrupts.

X16 SDRAM Configuration

The following chart identifies the interconnect between the NET+ARM chip and SDRAM when the SDRAM is used in a x16 configuration. Typically, a x16 SDRAM configuration is constructed using (1) x16 SDRAM component.

NET+ARM Chip Signal	16M SDRAM Signal	64M SDRAM Signal
CS/RAS*	CS*	CS*
CAS3*	RAS*	RAS*
CAS2*	CAS*	CAS*
CAS1*	WE*	WE*
CAS0*	A10/AP	A10/AP
BE3*	UDQM*	UDQM*
BE2*	LDQM*	LDQM*
BE1*	-	-
BE0*	-	-
A1	A0	A0
A2	A1	A1
A3	A2	A2
A4	A3	A3
A5	A4	A4
A6	A5	A5
A7	A6	A6
A8	A7	A7
A9	A8	A8
A10	A9	A9
A11		
A12		A11
A13		
A20	BA	
A21		BA0
A22		BA1

Table 10-4: 16 SDRAM Interconnect

Note	Description
1	Parameters 70a/70b only apply when the ENI FAST bit is set to 0. When ENI FAST is set to 1, then parameters 84a/84b apply.
2	The PEN* and PBRW* signals are used to control an external bi-directional data bus transceiver for the PDATA bus that can only drive 2mA.
3	Specification 72 only applies to ENI Registers while FAST is set to 0. This specification does NOT apply to Shared RAM access.
4	Specification 72a applies to all Shared RAM accesses when FAST is set to 0. The Max specification for PCS* to PACK* valid is larger for shared RAM accesses. The additional delay is dependent upon the speed of the external RAM assigned to provide the physical shared RAM. As such, the Max specification for shared RAM accesses is system dependent.
5	Specification 72b applies to ENI register accesses when FAST is set to 1.
6	Specification 72c applies to ENI shared RAM accesses when FAST is set to 1.
7	Specification 85 applies when FAST is set to 0. Specification 85a applies when FAST is set to 1.
8	Specification 77c can be reduced to (3 *Tsys) when FAST is set to 1.