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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e2051akg

11.2 Reset State 48
12 INTERRUPTS 51
12.1 Interrupt Sources 51
12.2 Priority Level Structure 52
12.3 Response Time 54
13 PROGRAMMABLE TIMERS/COUNTERS 55
13.1 Timer/Counters 0 & 1 55
13.2 Time-Base Selection 55
13.2.1 Mode 0 55
13.2.2 Mode 1 56
13.2.3 Mode 2 56
13.2.4 Mode 3 57
14 NVM MEMORY 58
15 WATCHDOG TIMER 59
15.1 WATCHDOG CONTROL 60
15.2 CLOCK CONTROL of Watchdog 60
16 SERIAL PORT (UART) 62
16.1 MODE 0 62
16.2 MODE 1 63
16.3 MODE 2 65
16.4 MODE 3 66
16.5 Framing Error Detection 67
16.6 Multiprocessor Communications 67
17 PULSE WIDTH MODULATED OUTPUTS (PWM) 69
18 ANALOG COMPARATORS 71
18.1 Comparator Interrupt with Debouncing 72
18.2 Application circuit 73
19 TIME ACCESS PROCTECTION 74
20 I/O PORT MODE SETTING 76
20.1 Quasi-Bidirectional Output Configuration 76
20.2 Open Drain Output Configuration 77
21 OSCILLATOR 78
21.1 On-Chip RC Oscillator Option 78
21.2 External Clock Input Option 78
22 POWER MONITORING FUNCTION 79
22.1 Brownout Detect and Reset 79
23 ICP (IN-CIRCUIT PROGRAM) FLASH MODE 81
24 CONFIG BITS 82
24.1 CONFIG0 82
24.2 CONFIG1 83
25 ELECTRICAL CHARACTERISTICS 84
25.1 Absolute Maximum Ratings 84

4 PIN CONFIGURATION

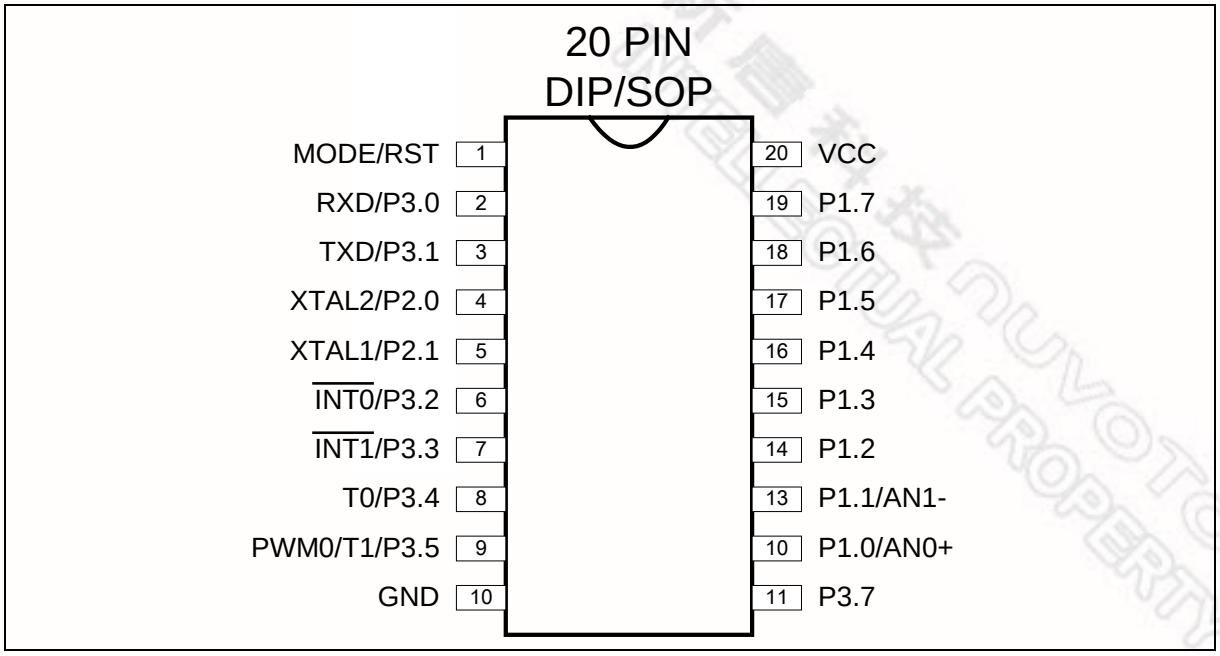

Table 4-1: Pin Configuration

Table 6-1: Data Pointer

6.7 Architecture

The W79E4051/2051 is based on the standard MCS-51 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard MCS-51 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E4051/2051. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump address. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E4051/2051. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E4051/2051 has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E4051/2051 has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E4051/2051. Hence the size of the stack is limited by the size of this RAM.

7.3 Scratch-pad RAM and Register Map

As mentioned before the W79E4051/2051 series have separate Program and Data Memory areas. The on-chip **256** bytes scratch pad RAM is built in W79E4051/2051. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

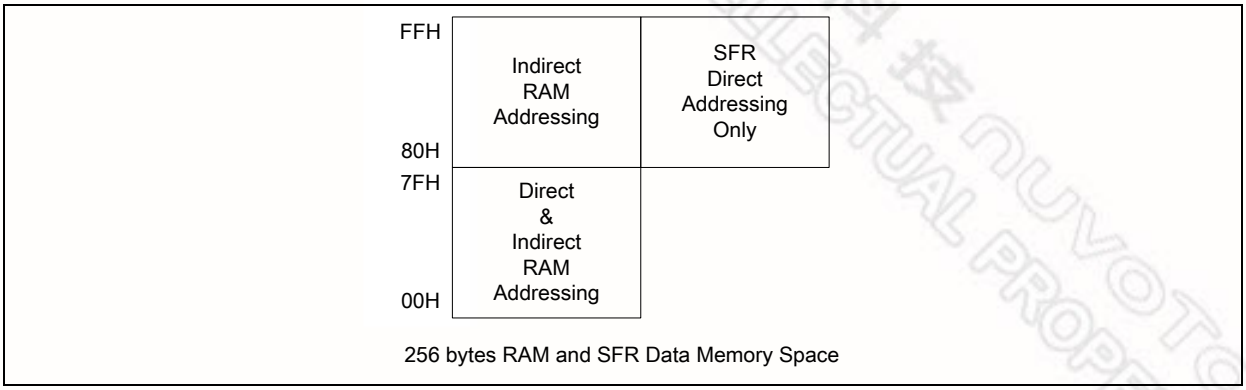

Table 7-2 W79E4051/2051 256 bytes RAM and SFR memory map

Since the scratch-pad RAM is **256** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

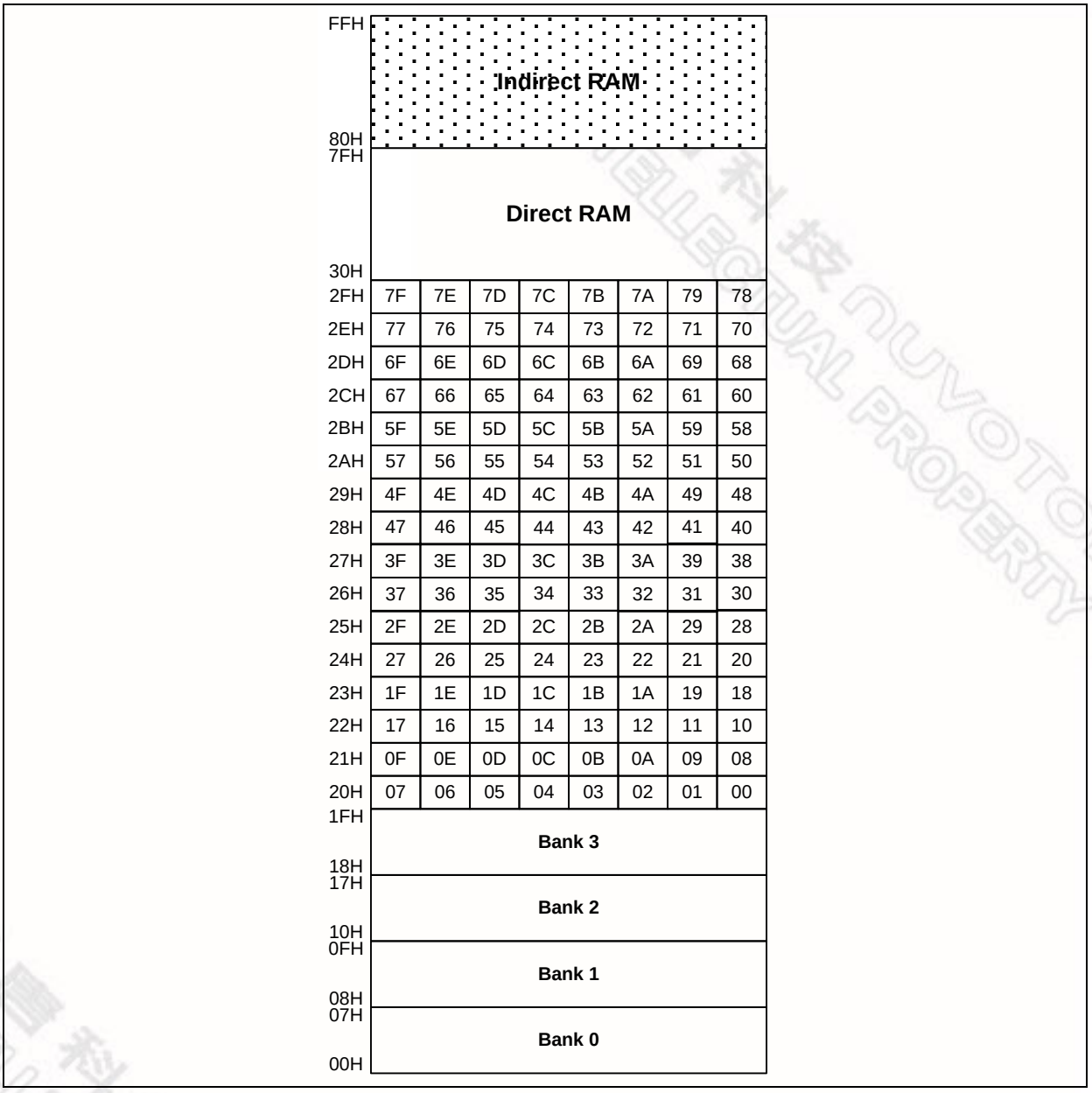

Table 7-3 Scratch-pad RAM

7.4 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E4051/2051 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	CIPE	Comparator Enabled in Idle and Power down Mode. 0: Comparator disabled in idle and power down mode. (default) 1: Comparator enabled in idle and power down mode.
4	CF	Comparator Interrupt Flag. Set by hardware when the comparator output meet the conditions specified by the CM[2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
3	CEN	Enable Comparator. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
2	CM2	See as below table.
1	CM1	See as below table.
0	CM0	See as below table.

Comparator Interrupt Mode Setting:

CM2	CM1	CM0	Interrupt Mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1

1	1	Brownout voltage is 4.5V

All the bits in this SFR have unrestricted read access. **SRST** require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

AUX FUNCTION REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS

Mnemonic: AUXR2 Address: A3h

BIT	NAME	FUNCTION
7-1	-	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EC	-	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EC	Enable analog comparator interrupt.
5	-	Reserved.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5

11 RESET CONDITIONS

The user has several hardware related options for placing the W79E4051/2051 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

11.1.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST pin is high and remains high up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

If the power supply falls below V_{RST}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. V_{RST} is about 2.0V.

11.1.3 Brown-Out Reset (BOR)

If the power supply falls below brownout voltage of V_{BOV}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a brownout reset.

11.1.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

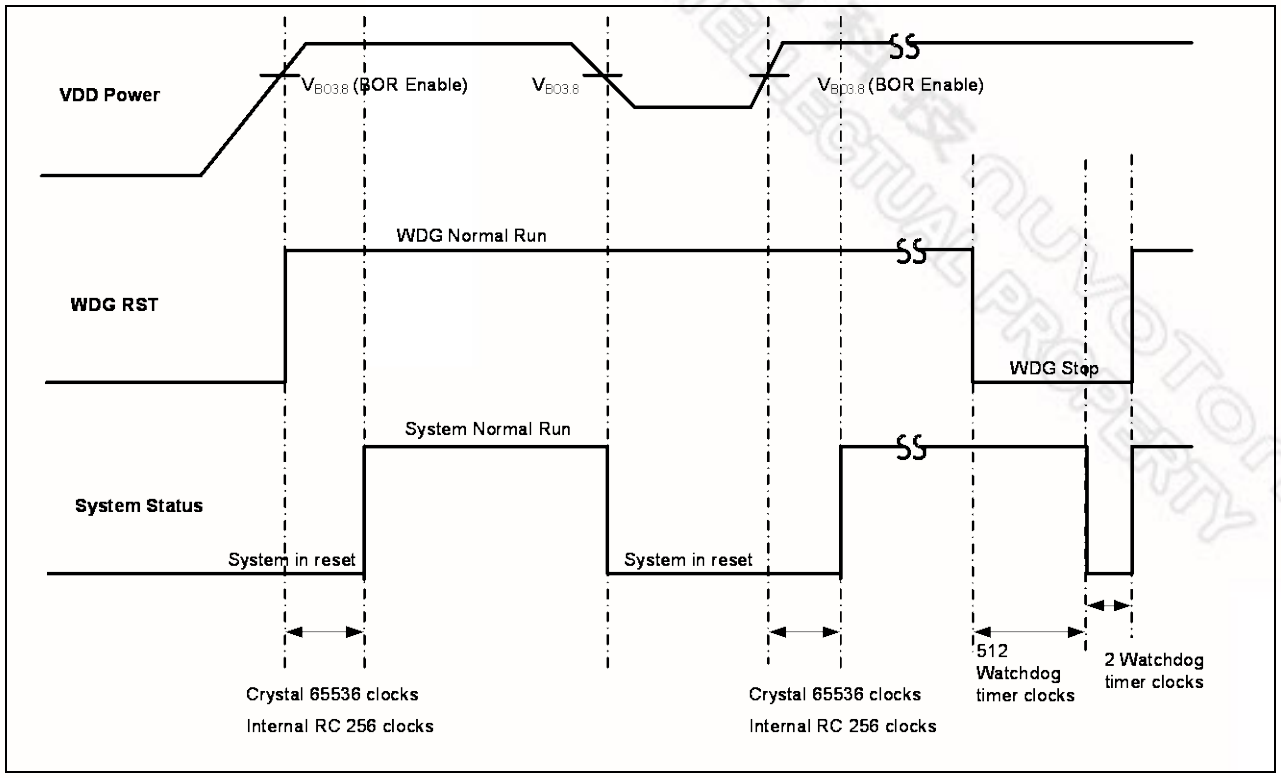

Figure 11-1: Internal reset and VDD monitor timing diagram

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being execute.
3. The current instruction does not involve a write to IE, IP and IPH, registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as follows:

VECTOR LOCATIONS FOR INTERRUPT SOURCES

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Brownout Interrupt	002Bh
Analog Comparator	0033h	-	003Bh
-	0043h	-	004Bh
Watchdog Timer	0053h	-	005Bh
-	0063h	PWM Period Interrupt	006Bh

Table 12-1: Vector locations for interrupt sources

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

12.2 Priority Level Structure

The W79E4051/2051 series uses a four priority level interrupt structure (highest, high, low and lowest) and supports up to 9 interrupt sources. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as table below. This allows great flexibility in controlling and handling many interrupt sources.

Priority Bits		Interrupt Priority Level
IPxH	IPx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 12-2: Four-level interrupt priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IPx and IPxH registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	Edge: Hardware, Software; Level: Follow the inverse of pin	1(highest)	Yes
Brownout Detect	BOF	002BH	EBOV (EIE.6)	IP1H.6, IP1.6	Software	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	IP1H.4, IP1.4	Software	3	Yes(1)
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	IP0H.1, IP0.1	Hardware, Software	4	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IP0H.2, IP0.2	Edge: Hardware, Software; Level:	5	Yes

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
					Follow the inverse of pin		
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	Hardware, Software	6	No
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	IP0H.4, IP0.4	Software	7	No
Comparator Interrupt	CF	0033H	EC (IE.6)	IP0H.6, IP0.6	Software	8	Yes(2)
PWM Period Interrupt	PWMF	006BH	EPWM (EIE.5)	IP1H.5, IP1.5	Software	9(lowest)	No

Table 12-3: Vector location for Interrupt sources and power down wakeup

Note:

1. The Watchdog Timer can wake up Power Down Mode when its clock source is from internal RC.
2. The comparator can wake up Power Down Mode when bit ACSR.5(CIPE) is set to high.

12.3 Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ to RI+TI, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W79E4051/2051 series are performing a write to IE, IP and IPH and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP or IPH access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycles is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

18.1 Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs maybe cause the comparator output toggle excessively, especially applying slow moving analog inputs. Table 18-2: Comparator Interrupt Mode shows the 8 comparator interrupt modes set by CM[2:0] in ACSR(97H). A built-in configurable debouncing timer provides 8 debouncing timing controlled by CPCK[2:0] for widely applications. The debouncing timing is shown in Table 18-1. If CPU is in normal/Idle mode F_{DB} is from Fosc; if CPU is in power-down mode F_{DB} is from internal RC 22M/11M Hz oscillator.

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$
1	1	1	$(3/F_{DB})*256$~$(4/F_{DB})*256$

Table 18-1: Comparator Debouncing Time

CM2	CM1	CM0	Comparator interrupt mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

Table 18-2: Comparator Interrupt Mode

Three debouncing modes are provided to filter out this noise. In debouncing mode when the comparator output matches one of three debouncing mode condition, the debouncing timer resets and starts up-counting. The end of debouncing triggers the hardware to check if the comparator output matches the mode condition or not. If it is compliant with the mode condition the comparator flag CF is set by hardware, otherwise CF keeps low. Refer to Figure 18-2.

20 I/O PORT MODE SETTING

W79E4051/2051 has maximum one 8-bit(P1), one 7-bit(P3) and one 2-bit(P2) ports. Except P1.0 and P1.1, all pins are quasi-bidirectional mode, which are common with standard 80C51, that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0 and P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset. The P2.0 (XTAL2) can be configured as clock output by setting bit ENCLK to high when CPU clock source is from on-chip RC or external Oscillator, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports except P1.0 and P1.1 output are in this mode, and output is common with the MCS-51. This mode can be used as both an input and output without the need to reconfigure the port. P1.0~P1.1 stays in PMOS-off open-drain mode after CPU reset.

P1M1.Y	PORT INPUT/OUTPUT MODE
0	Open Drain
1	Quasi-bidirectional

Table 20-1: I/O port Configuration Table

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current up to about 20mA/10mA at V_{DD}=5V/2.7V.

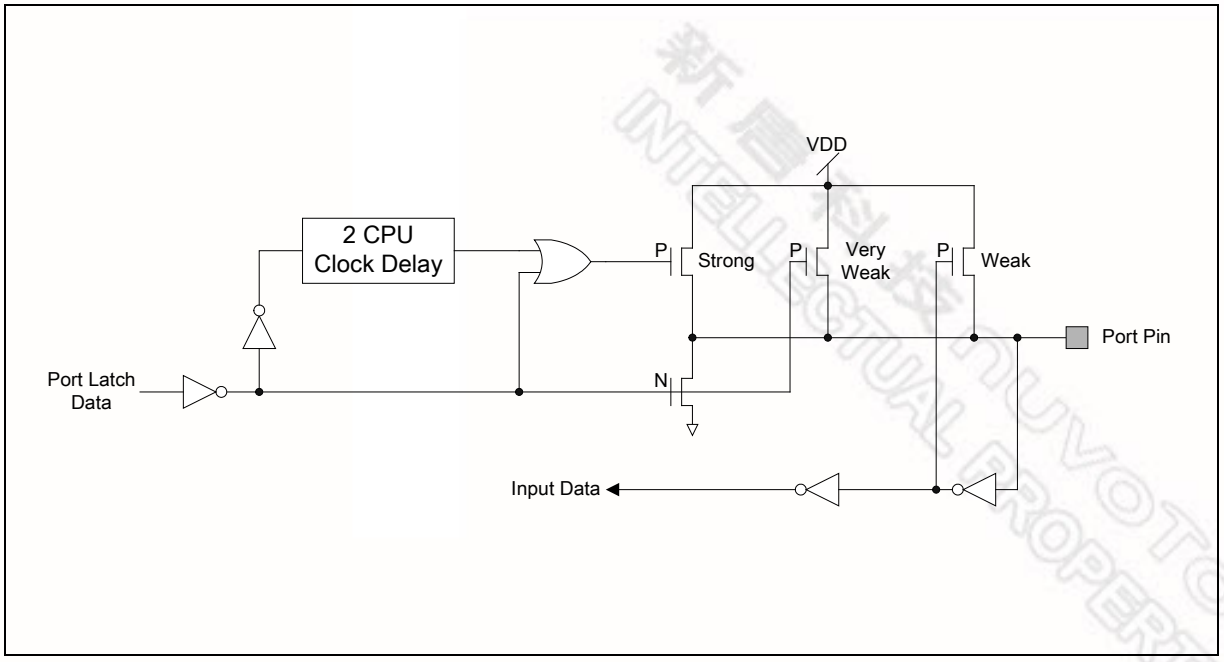

Figure 20-1: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

P1.0 and P1.1 are in open drain type after chip reset. To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

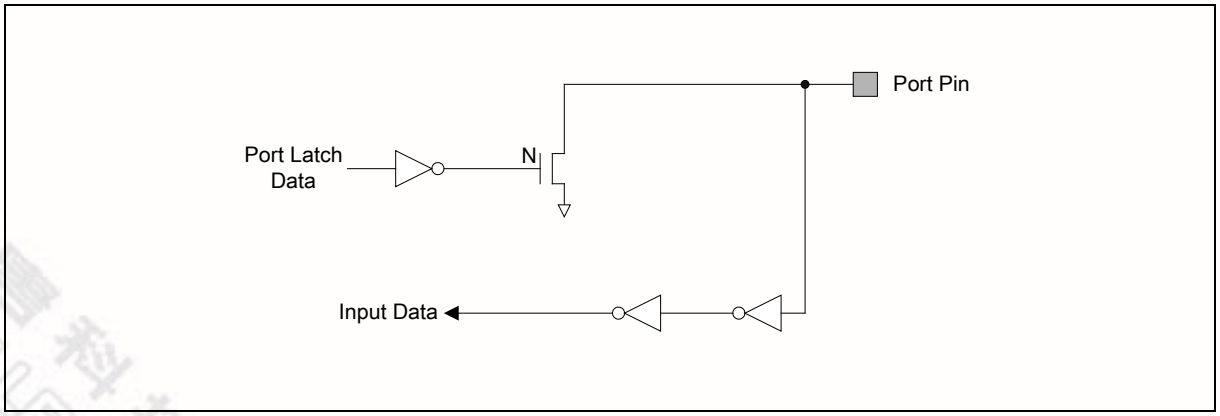

Figure 20-2: Open Drain Output

24.2 CONFIG1

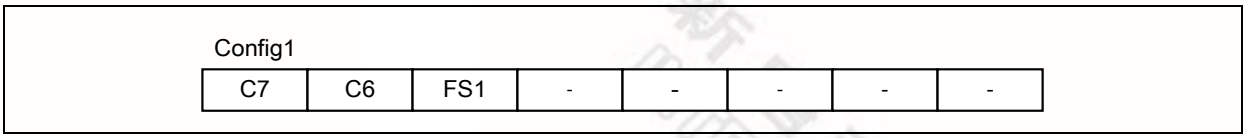

Figure 24-2: Config1 register bits

Bit	Name	Function
7	C7	4K/2K Program Flash EPROM Lock bit This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.
6	C6	128 byte Data Flash EPROM Lock bit This bit is used to protect the customer's 128 bytes of data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the 128 bytes of Flash EPROM data and CONFIG Registers can not be accessed again.
5	FS1	Internal Oscillator 11MHz/22MHz selection bit This bit is used to select 11MHz or 22MHz internal oscillator. 1: Internal oscillator is set to 22MHz 0: Internal oscillator is set to 11MHz
0~4	-	Reserved.

Lock bits C7 and C6:

Bit 7	Bit 6	Function Description
1	1	Both security of **4K/2KB** program code and **128** Bytes data area are not locked. They can be erased, programmed or read by Writer or ICP.
0	1	The **4K/2KB** program code area is locked. It can not be read and written by Writer or ICP. The **128** Bytes data area can be program one time or read.
1	0	Not supported.
0	0	Both security of **4K/2KB** program code and **128** Bytes data area are locked. They can not be read and written by Writer or ICP.

25.6 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
W79E2051/W79E4051 Frequency accuracy of On-chip RC oscillator (Without calibration)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
W79E2051R/W79E4051R On-chip RC oscillator with calibration[1,2] (Fosc = 22.1184MHz with factory calibration)	-2		2	%	V_{DD}=5.0V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		7	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.
2. RC frequency deviation vs. V_{DD} and Temperature is shown below