Nuvoton Technology Corporation - W79E2051ARG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e2051arg

1 GENERAL DESCRIPTION

The W79E4051/2051 series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by **ICP (In Circuit Program) Writer**. The instruction set of the W79E4051/2051 series are fully compatible with the standard 8052. The W79E4051/2051 series contain a **4K/2K** bytes of program Flash EPROM; a **256** bytes of RAM; **128** bytes data Flash EPROM for customer data storage; two 8-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; an enhanced full duplex serial port; 1 channel PWM by 10-bit counter, Brownout voltage detection/reset, Power on reset detection and one analog comparator. These peripherals are supported by **9** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E4051/2051 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

7 MEMORY ORGANIZATION

The W79E4051/2051 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E4051/2051 series can be up to **4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The Data Flash EPROM on the W79E4051/2051 series is **128** bytes long with page size of **16** bytes. The W79E4051/2051 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

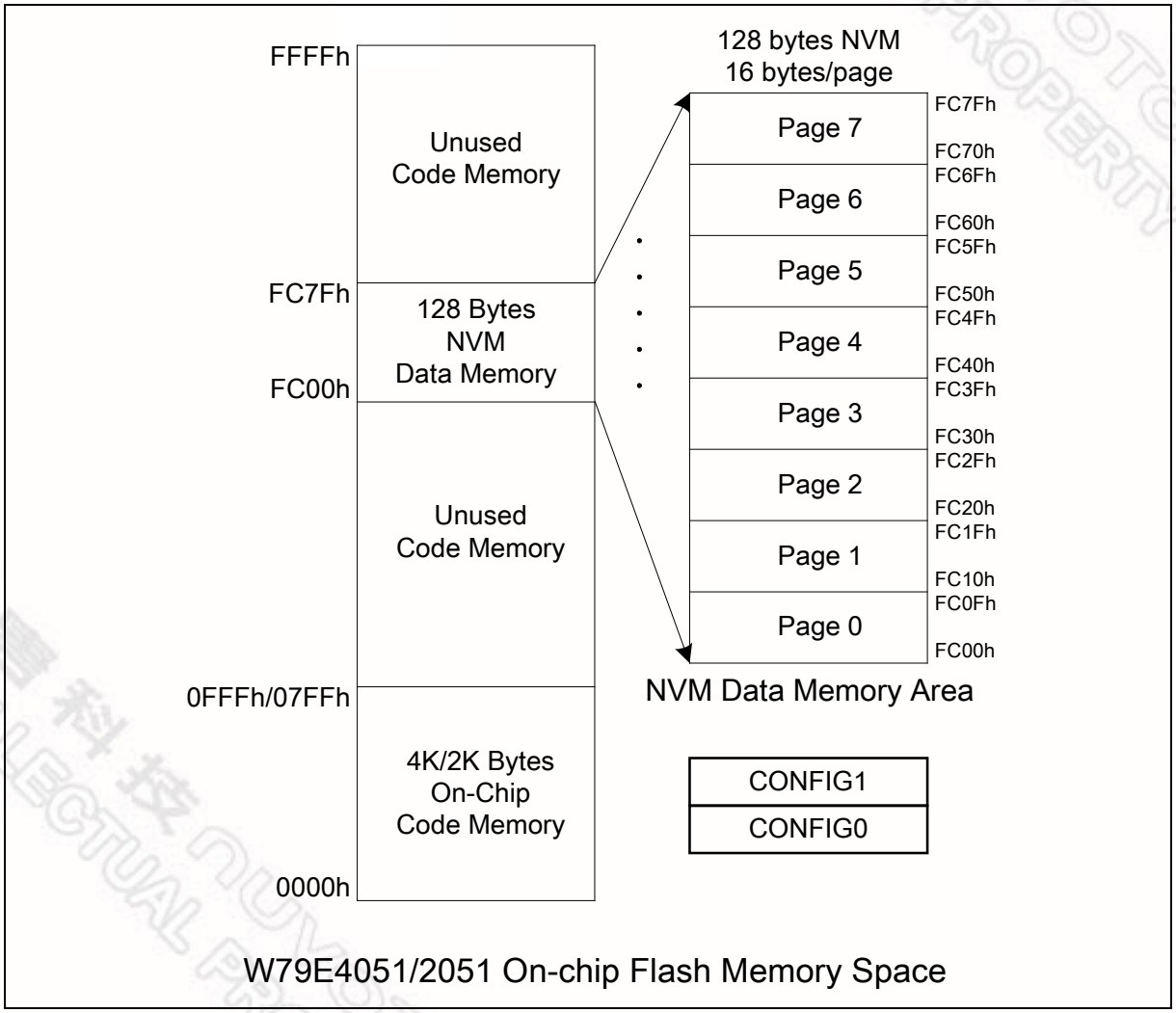


Table 7-1 W79E4051/2051 On-chip Flash Memory Map

8 SPECIAL FUNCTION REGISTERS

The W79E4051/2051 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E4051/2051 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	**IP1**							
F0	**B**						PCMPIDS	IP1H
E8	**EIE**							
E0	**ACC**							
D8	**WDCON**	PWMPL	PWM0L		PWMCON1			
D0	**PSW**	PWMPH	PWM0H					PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	**IP0**	SADEN						
B0	**P3**			P1M1				IP0H
A8	**IE**	SADDR						
A0	**P2**		AUXR1	AUXR2				
98	**SCON**	SBUF						
90	**P1**						ACCK	ACSR
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	CLKREG
80		SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note:
1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.

Note :
1. In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.
2. BOD is initialized at reset with the inversed value of bit CBOD in config0-bits.
3. (BOV1,BOV0) are initialized at reset with the reversed value of config0-bits (CBOV1,CBOV0)

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1

1	1	Brownout voltage is 4.5V

All the bits in this SFR have unrestricted read access. **SRST** require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

AUX FUNCTION REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS

Mnemonic: AUXR2 Address: A3h

BIT	NAME	FUNCTION
7-1	-	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EC	-	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EC	Enable analog comparator interrupt.
5	-	Reserved.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0

9 INSTRUCTION

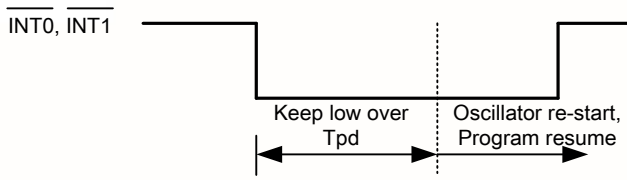
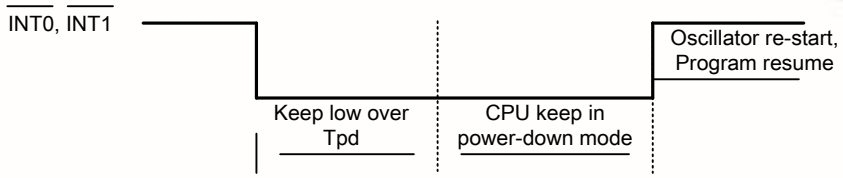
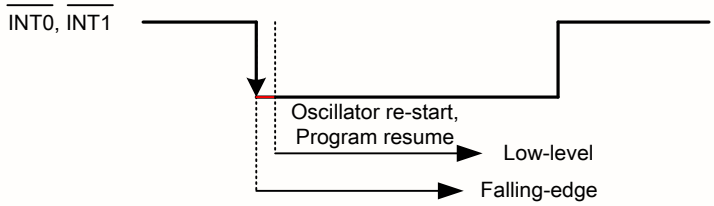
The W79E4051/2051 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the W79E4051/2051 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E4051/2051 series reduces the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/205 1 series vs. 8032 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3

CIPE=1). The W79E4051/2051 series can be waken up from the Power Down mode by forcing the above sources activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then interrupt event will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

In W79E4051/2051 series either a *low-level or a falling-edge at external interrupt pin,* $\overline{\text{INT1}}$ or $\overline{\text{INT0}}$ ***will re-start the oscillator. W79E4051/2051 provides 3 wake-up modes, selected by SFR bits PWDEX1 and PWDEX0, that the external interrupt pins can terminate power-down mode. Refer to the table below.***

PWDEX[1:0]	TRIGGER TYPE	FUNCTION TO TERMINATE POWER-DOWN MODE
0, 0 (Mode1)	Low-level	
0, 1 (Mode2)	Low-level	
1, x (Mode3)	Low-level and Falling-edge	

In mode1 and mode2, the external interrupt pin must keep low longer than Tpd otherwise CPU stays in power-down mode continuously. Tpd is about 2mS counted by built-in RC oscillator.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

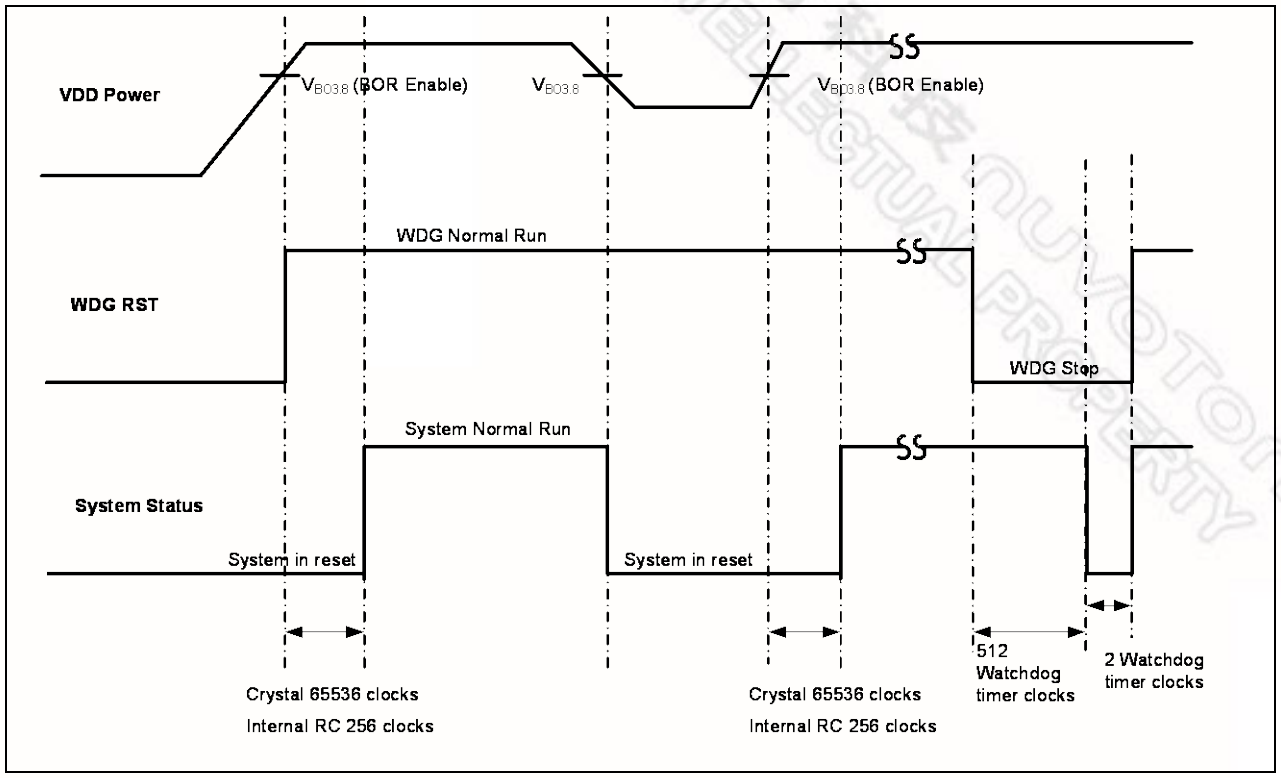


Figure 11-1: Internal reset and VDD monitor timing diagram

15 WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

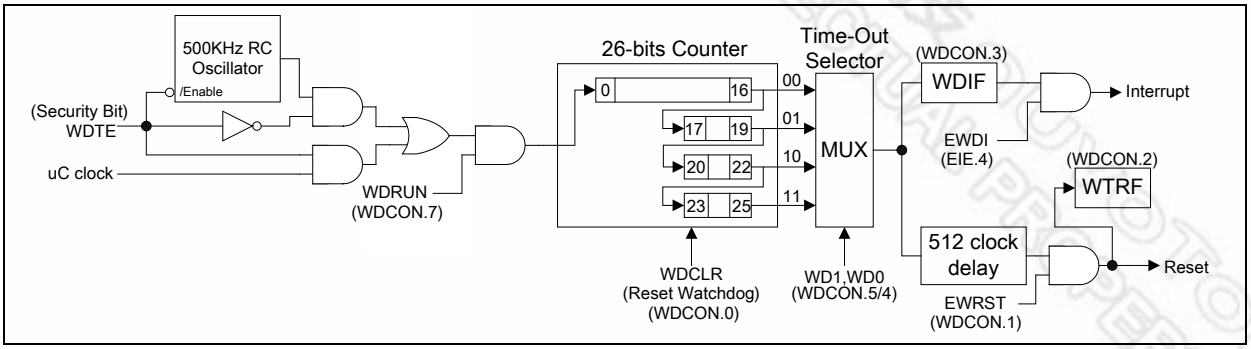


Figure 15-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 WDT clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock

All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111x) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as xxxx xxxx (i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

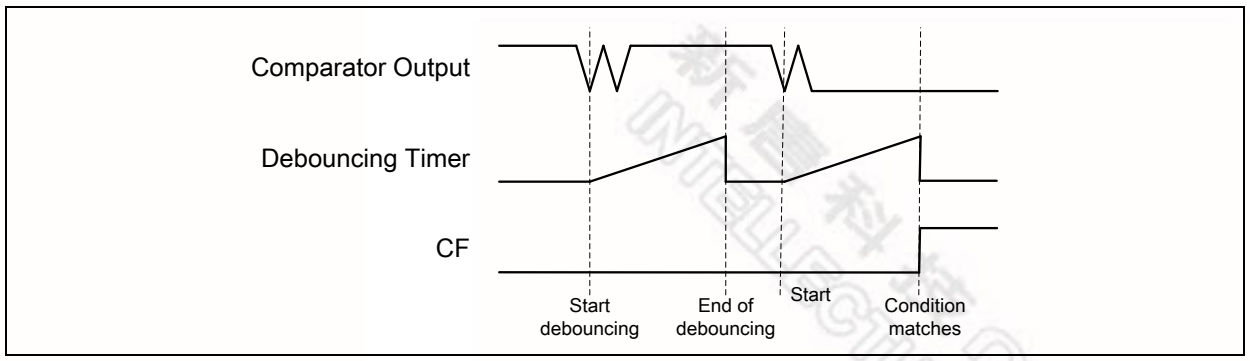


Figure 18-2: Example of Negative Edge Comparator Interrupt with Debouncing

18.2 Application circuit

It is recommended to add a decoupled capacitor as close as port pin for reducing the variation of offset voltage as show in Figure 18-3.

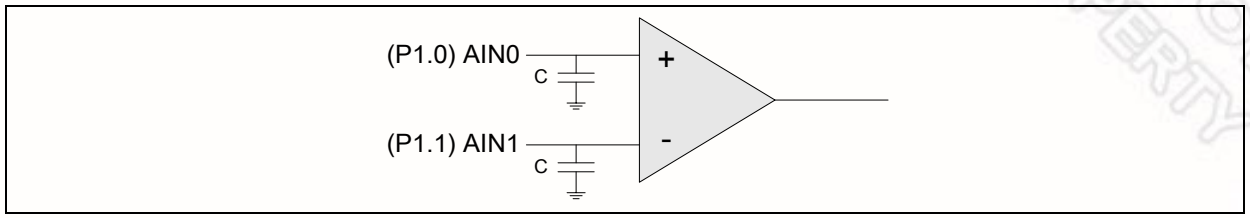


Figure 18-3: Application Circuit of Comparator

```
NOP                                 ;1 M/C
MOV         TA, #055h               ;3 M/C
SETB        EWT                     ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

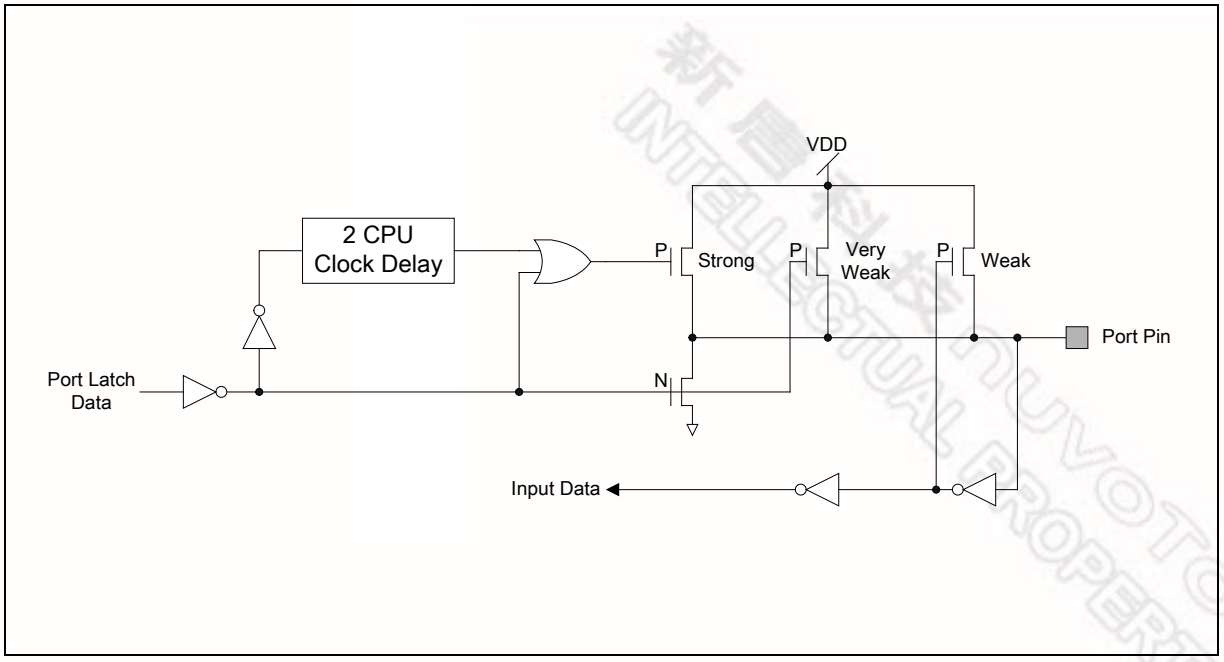


Figure 20-1: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

P1.0 and P1.1 are in open drain type after chip reset. To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

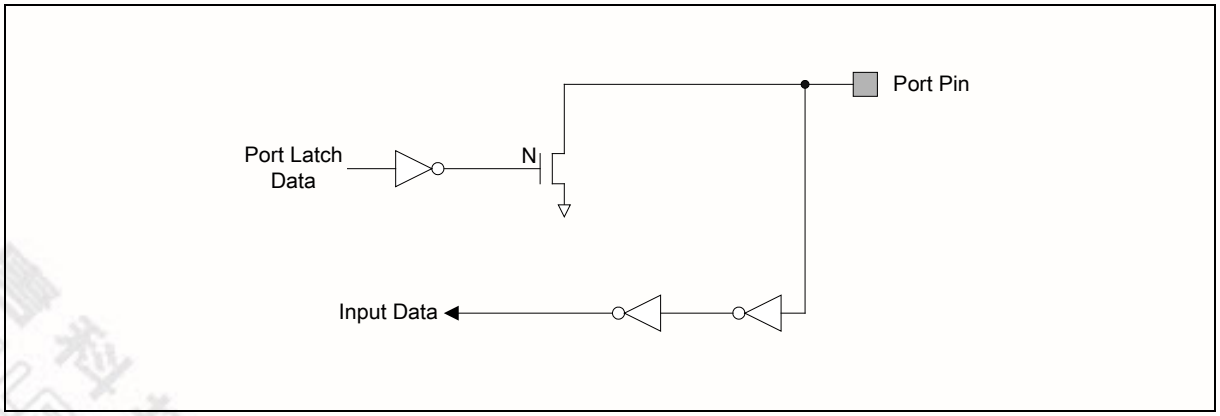


Figure 20-2: Open Drain Output

21 OSCILLATOR

The W79E4051/2051 series provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 24MHz, and without capacitor or resister.

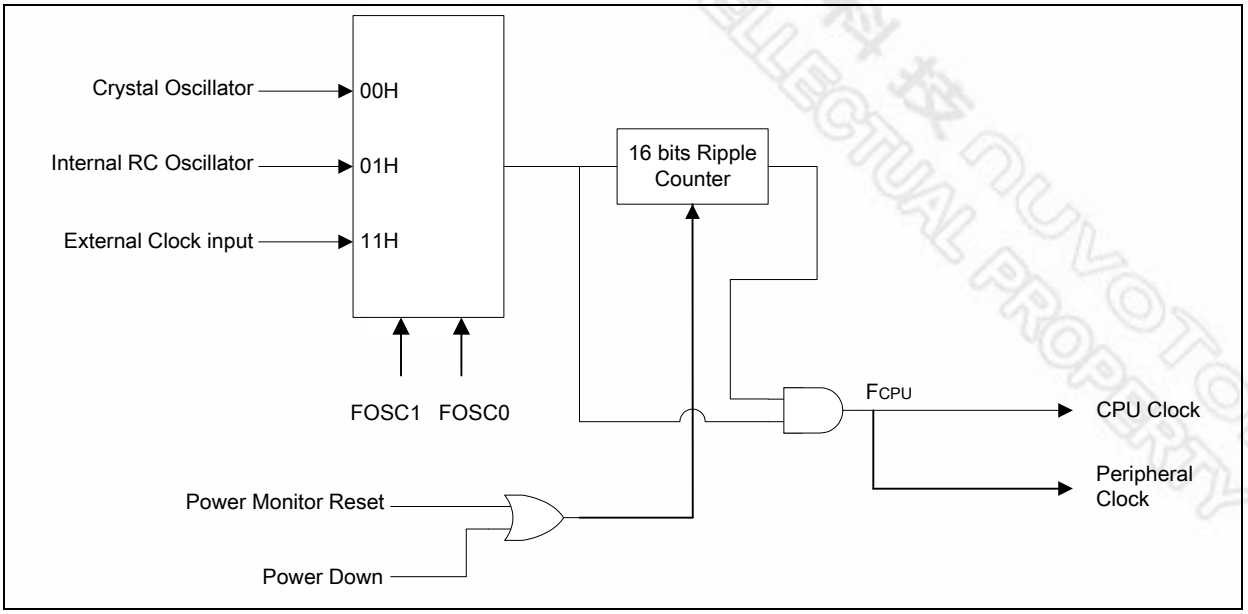


Figure 21-1: Oscillator

21.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator of W79E4051R and W79E2051R is trimmed by factory and is configurable to **11.0592MHz/22.1184MHz ± 2%** (through Configuration-bit FS1 bit) frequency to support clock source. When FOSC1, FOSC0 = 01H, the On-Chip RC Oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

Note:

For the untrimmed parts of W79E2051 and W79E4051, the untrimmed frequency of internal RC oscillator may have ± 25% deviation compared to the nominal frequency in 22.1184Mhz. It maybe has an potential risk that CPU runs over specified speed if the untrimmed frequency is over 24MHz.

21.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11H, and frequency range is form 4MHz up to 24MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The W79E4051/2051 series supports a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the W79E4051/2051 serial. When enabled, via the ENCLK bit in the ACCK.7, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode for saving additional power. The clock output may also be enabled when the external clock input option is selected.

22 POWER MONITORING FUNCTION

In order to prevent incorrect operation during power up and power drop, the W79E4051/2051 is provided a power monitor function, Brownout Detect.

22.1 Brownout Detect and Reset

The W79E4051/2051 has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 4 nominal levels are 2.4V, 2.7V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatedly senses the voltage for 64/f_{BRC} then turn off detector for 960/ f_{BRC} if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator, is approximately 100K* V_{DD} HZ ±50%. The relative control bits are located in SFR AUXR1 @A2h. The Brownout Detect block is shown in Figure 22-1.

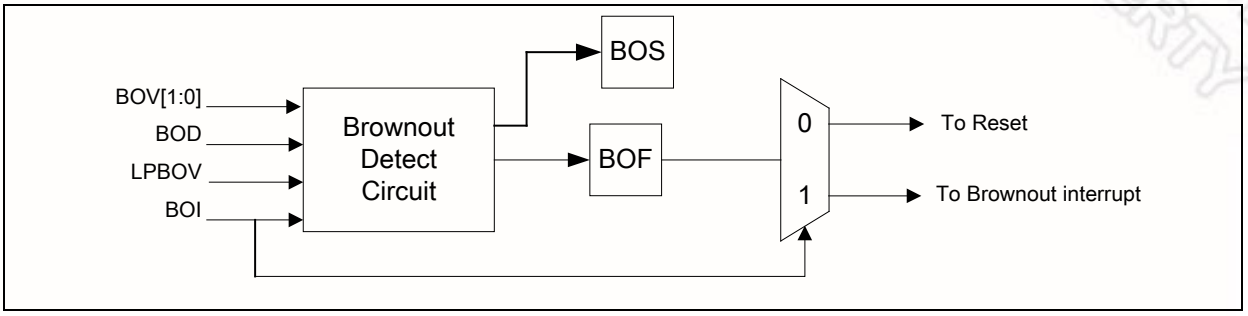


Figure 22-1: Brown-out Detect Block

25.3 The COMPARATOR ELECTRICAL CHARACTERISTICS

(VDD–VSS = 3.0~5V±10%, TA = -40~85°C, Fosc = 24MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	50	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}
Comparator offset voltage	V_{OFF}			20	mV	With decoupled capacitors on inputs

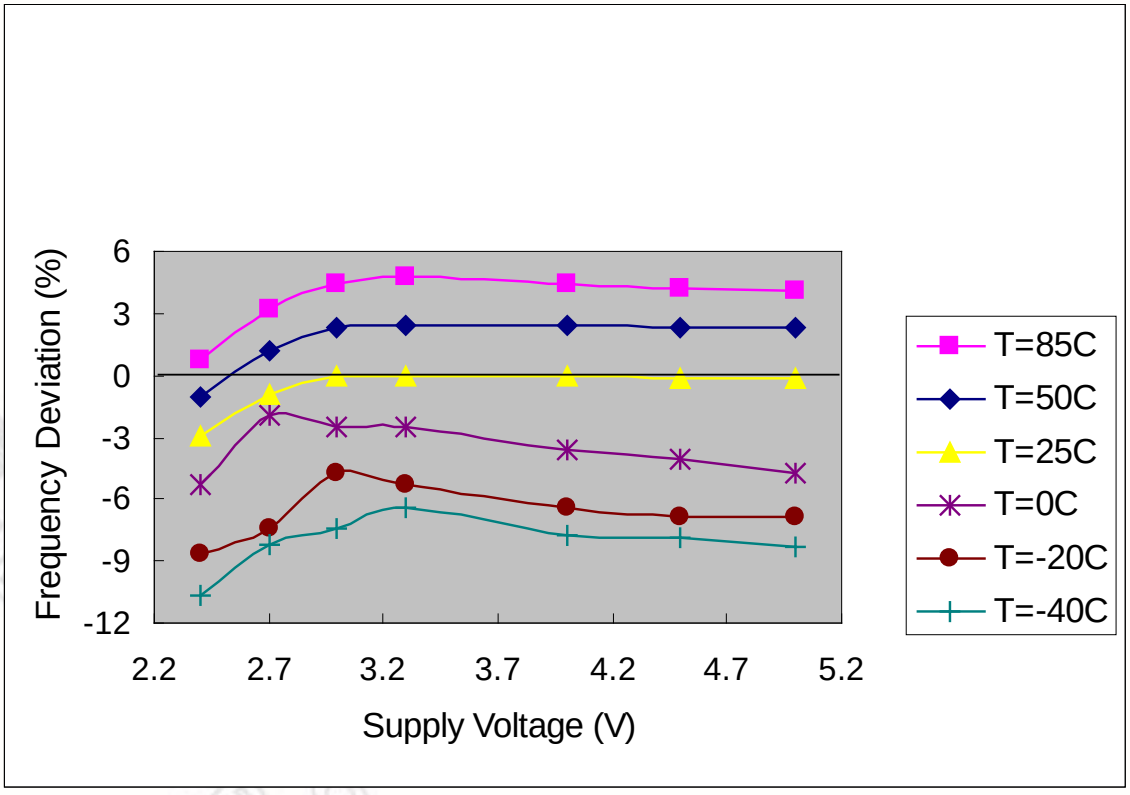
25.6 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

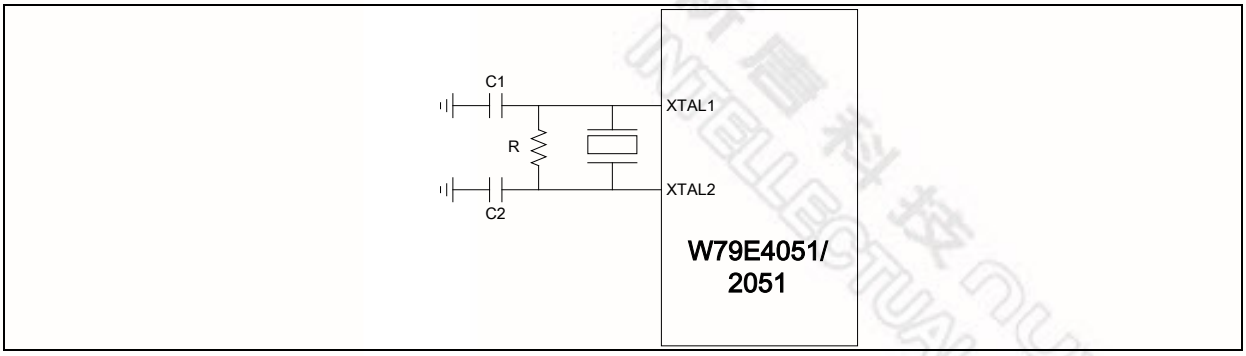
Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
W79E2051/W79E4051 Frequency accuracy of On-chip RC oscillator (Without calibration)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
W79E2051R/W79E4051R On-chip RC oscillator with calibration[1,2] (Fosc = 22.1184MHz with factory calibration)	-2		2	%	V_{DD}=5.0V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		7	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.
2. RC frequency deviation vs. V_{DD} and Temperature is shown below



26 TYPICAL APPLICATION CIRCUITS



The table below shows the reference values for crystal applications.

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

28 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	July 9, 2008	-	Initial Issued
A02	August 4, 2008	78 86 85	1. Add a notice for the untrimmed internal RC OSC. 2. Modify the test condition of “Hysterisis range of BOD voltage” in DC spec. 3. Modify the Max value of power down current.
A03	August 29, 2008	86 91	1. Revised Maximum Current suck by total I/O pins from 75mA to 80mA. 2. Modify “24.6 RC OSC AND AC CHARACTERISTICS”
A04	December 22, 2008	25 88 83	1. Revise the description of SFR bit LPBOV 2. Correct I_{BO2} 3215 with 32/15. 3. Add Chapter 23 ICP
A05	February 25, 2009	5, 84	1. Add DC spec of Data Flash program/erase voltage
A06	April 16, 2009	5,6,7 94	1. Add SSOP20 parts of W79E4051ARG/RARG and W79E2051ARG/RARG. 2. Add SSOP-20 package dimension diagram.