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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e2051rakg

4 PIN CONFIGURATION

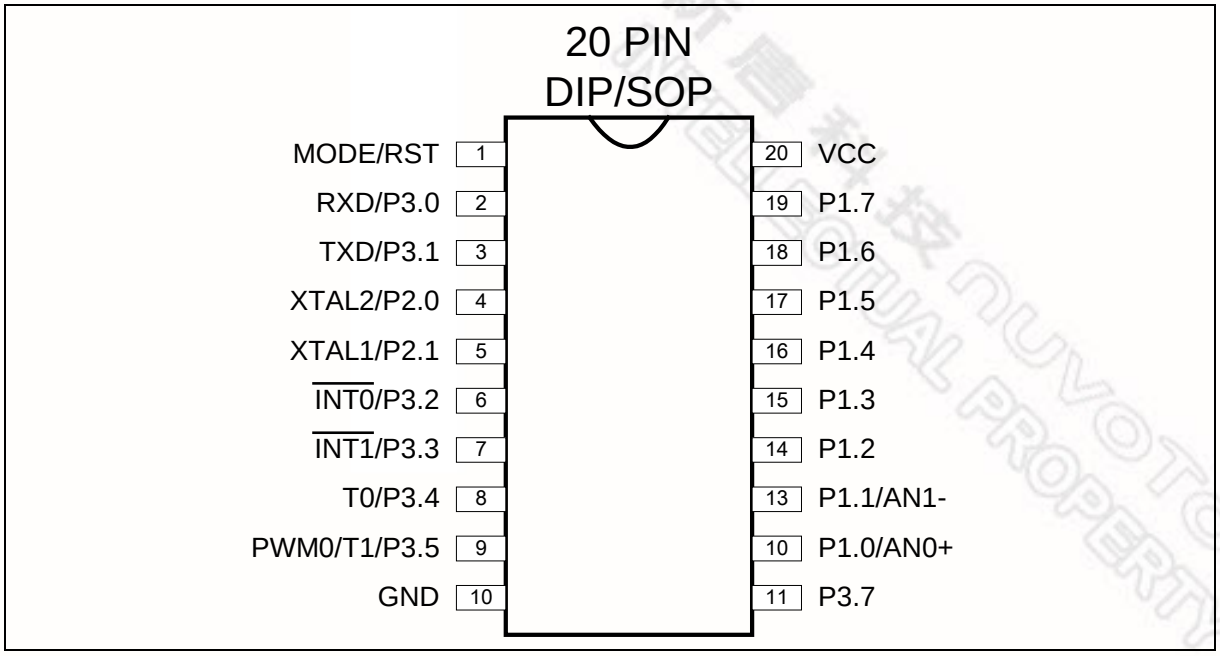


Table 4-1: Pin Configuration

6 FUNCTIONAL DESCRIPTION

The W79E4051/2051 architecture consist of a 4T 8051 core controller surrounded by various registers, **4K/2K** bytes AP Flash EPROM, **256** bytes of RAM, **128** bytes Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E4051/2051 includes one **4K/2K** bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the AP Flash EPROM and Data Flash EPROM.

This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

W79E4051/2051 has one 8-bit, one 7-bit and one 2-bit ports using on-chip oscillator by reset options. Except P1.0 and P1.1, all ports are in quasi-bidirectional structure that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0~P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset.

6.3 Serial I/O

The W79E4051/2051 has one serial port that is functionally similar to the serial port of the original 8051 family. However the serial port on the W79E4051/2051 can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

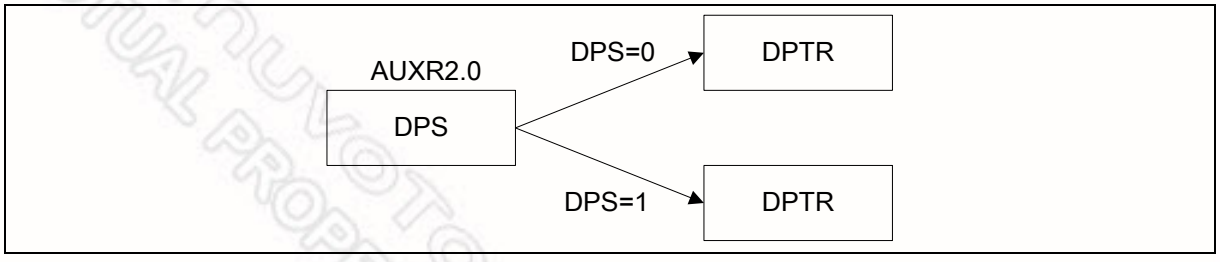
The W79E4051/2051 has two 16-bit timers that are functionally and similar to the timers of the 8051 family. When used as timers, user has a choice to set 12 or 6 clocks per count that emulates the timing of the original 8051. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in the W79E4051/2051 is slightly different from that of the standard 8051. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointer of W79E4051/2051 is similar to standard 8051 but has dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR2.0. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.



7.3 Scratch-pad RAM and Register Map

As mentioned before the W79E4051/2051 series have separate Program and Data Memory areas. The on-chip **256** bytes scratch pad RAM is built in W79E4051/2051. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

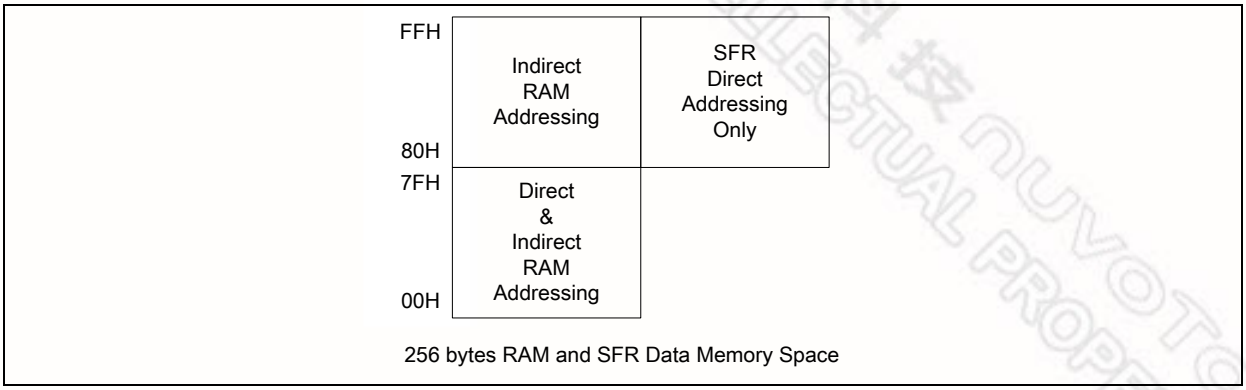


Table 7-2 W79E4051/2051 256 bytes RAM and SFR memory map

Since the scratch-pad RAM is **256** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

8 SPECIAL FUNCTION REGISTERS

The W79E4051/2051 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E4051/2051 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	**IP1**							
F0	**B**						PCMPIDS	IP1H
E8	**EIE**							
E0	**ACC**							
D8	**WDCON**	PWMPL	PWM0L		PWMCON1			
D0	**PSW**	PWMPH	PWM0H					PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	**IP0**	SADEN						
B0	**P3**			P1M1				IP0H
A8	**IE**	SADDR						
A0	**P2**		AUXR1	AUXR2				
98	**SCON**	SBUF						
90	**P1**						ACCK	ACSR
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	CLKREG
80		SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note:
1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
IP1	Interrupt priority 1	F8H	(FF) -	(FE) PBOV	(FD) PPWM	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	x000 xxxxB
IP1H	Interrupt high priority 1	F7H	-	PBOVH	PPWMH	PWDIH	-	-	-	-	x000 xxxxB
PCMPIDS	Port Comparator Input Disable	F6H	-	-	-	-	-	-	B1	B0	xxxx 0000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) EBOV	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	xx000 xxxxB
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	load	PWMF	CLRPWM	-	-	-	PWM0I	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	0X00 0000B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	-	PWM0OE	-	-	FP1	FP0	0000 XX00B
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	XXXX XX00B
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	XXXX XX00B
PSW	Program Status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-		00xxxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM byte address	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	00000000B
SADEN	Slave address mask	B9H									00000000B
IP0	Interrupt priority 0	B8H	(BF) -	(BE) PC	(BD) -	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x0x00000B
IP0H	Interrupt high priority 0	B7H	-	PCH	-	PSH	PT1H	PX1H	PT0H	PX0H	x0x00000B
P1M1	Port1 Mode 1	B3H	-	-	-	-	-	-	P1M1.1	P1M1.0	xxxx xx00B
P3	Port 3	B0H	(B7)	(B6)	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	11111111B
SADDR	Slave address	A9H									00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EC	(AD) -	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	00x00000B
AUXR2	AUX function register 2	A3H								DPS	xxxx xxx0B
AUXR1	AUX function register 1	A2H	BOF	BOD[2]	BOI	LPBOV	SRST	BOV1[3]	BOV0[3]	BOS	0x00 0xx0B
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3) -	(A2) -	(A1) P2.1 XTAL1	(A0) P2.0 XTAL2 CLKOUT	xxxx xxxxB
SBUF	Serial buffer	99H									xxxxxxxxB
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	00000000B
ACSR	Analog Comparator Control & Status Register	97H	-	-	CIPE	CF	CEN	CM2	CM1	CM0	xx000000B
ACCK	Analog Comparator Debounce Clock Control	96H	ENCLK	-	-	-	-	CPCK2	CPCK1	CPCK0	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91)	(90)	11111111B
CLKREG		8FH						PWDEX1	PWDEX0		Xxxx x00xB
CKCON	**Clock control**	**8EH**	**-**	**-**	**-**	**T1M**	**T0M**	**-**	**-**	**-**	**xxx00xxxB**
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T1#	M1	M0	GATE	C/T0#	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	SMOD	SMOD0		POR	GF1	GF0	PD	IDL	00xx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B

Table 8-2: Special Function Registers

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has 8 pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDRL registers, which will automaticly enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5-0	-	Reserved.

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA3	NVMDATA.2	NVMDATA.1	NVMDATA.0

Mnemonic: NVMDATA Address: CFh

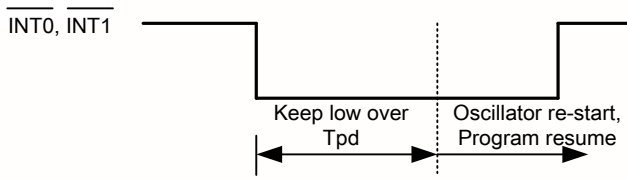
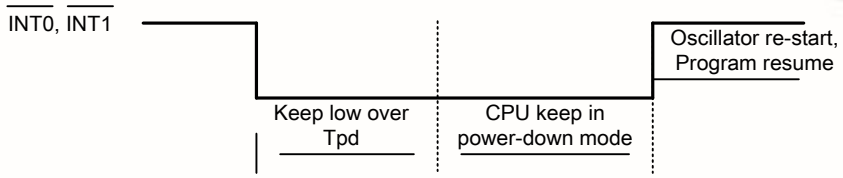
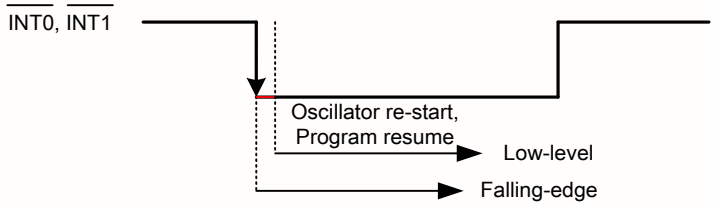
BIT	NAME	FUNCTION
7~0	NVMDATA[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

CIPE=1). The W79E4051/2051 series can be waken up from the Power Down mode by forcing the above sources activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then interrupt event will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

In W79E4051/2051 series either a *low-level or a falling-edge at external interrupt pin,* $\overline{\text{INT1}}$ or $\overline{\text{INT0}}$ ***will re-start the oscillator. W79E4051/2051 provides 3 wake-up modes, selected by SFR bits PWDEX1 and PWDEX0, that the external interrupt pins can terminate power-down mode. Refer to the table below.***

PWDEX[1:0]	TRIGGER TYPE	FUNCTION TO TERMINATE POWER-DOWN MODE
0, 0 (Mode1)	Low-level	
0, 1 (Mode2)	Low-level	
1, x (Mode3)	Low-level and Falling-edge	

In mode1 and mode2, the external interrupt pin must keep low longer than Tpd otherwise CPU stays in power-down mode continuously. Tpd is about 2mS counted by built-in RC oscillator.

11 RESET CONDITIONS

The user has several hardware related options for placing the W79E4051/2051 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

11.1.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST pin is high and remains high up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

If the power supply falls below V_{RST}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. V_{RST} is about 2.0V.

11.1.3 Brown-Out Reset (BOR)

If the power supply falls below brownout voltage of V_{BOV}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a brownout reset.

11.1.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

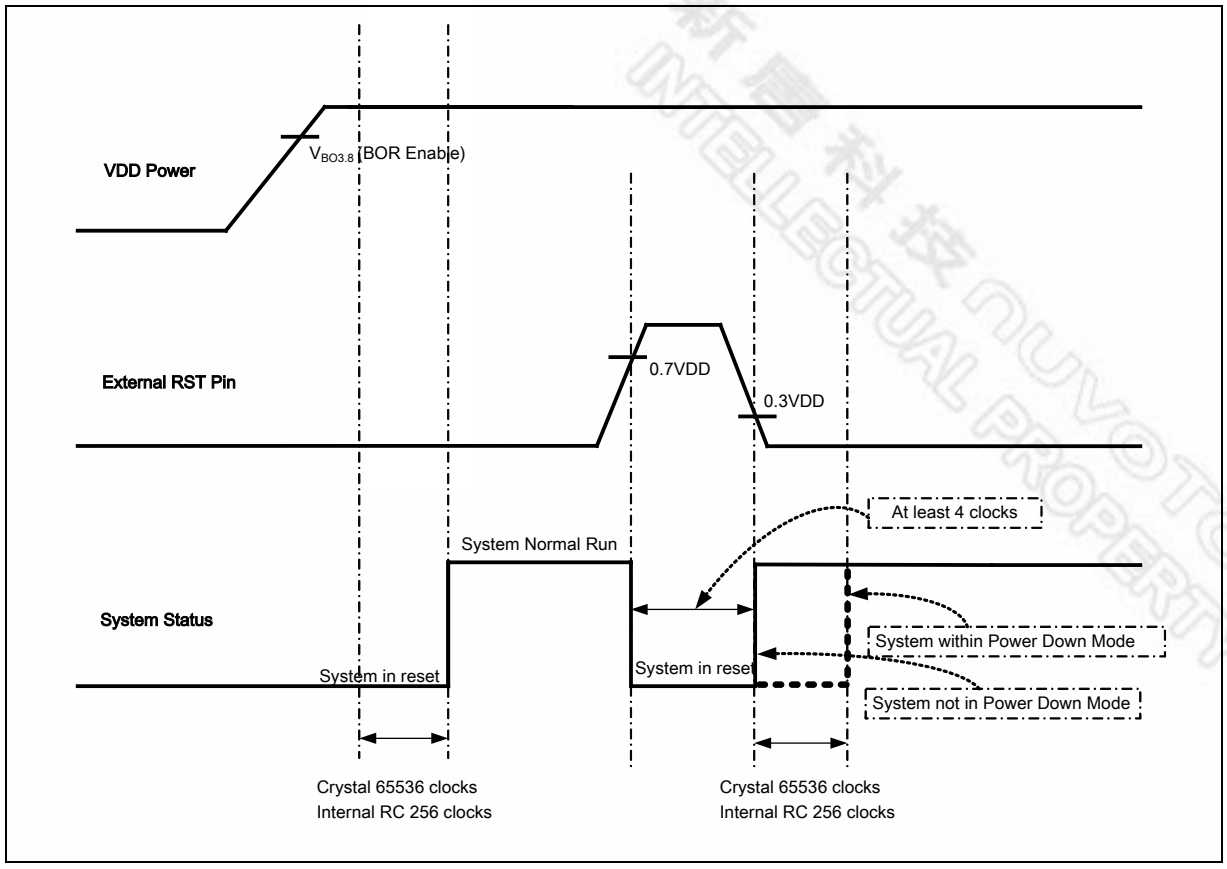


Figure 11-2: External reset timing diagram

WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

16 SERIAL PORT (UART)

The UART in this device is a full duplex port. It provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W79E4051/2051.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

19 TIME ACCESS PROCTECTION

The W79E4051/2051 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E4051/2051 series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h            ;Define new register TA, @0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
        MOV     TA, #0AAh       ;3 M/C  Note: M/C = Machine Cycles
        MOV     TA, #055h       ;3 M/C
        MOV     WDCON, #00h     ;3 M/C
```

Example 2: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        SETB    EWRST           ;2 M/C
```

Example 3: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        ORL     WDCON, #00000010B ;3M/C
```

Example 4: Invalid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        NOP                     ;1 M/C
        CLR     EWT             ;2 M/C
```

Example 5: Invalid Access

```
        MOV     TA, #0AAh       ;3 M/C
```

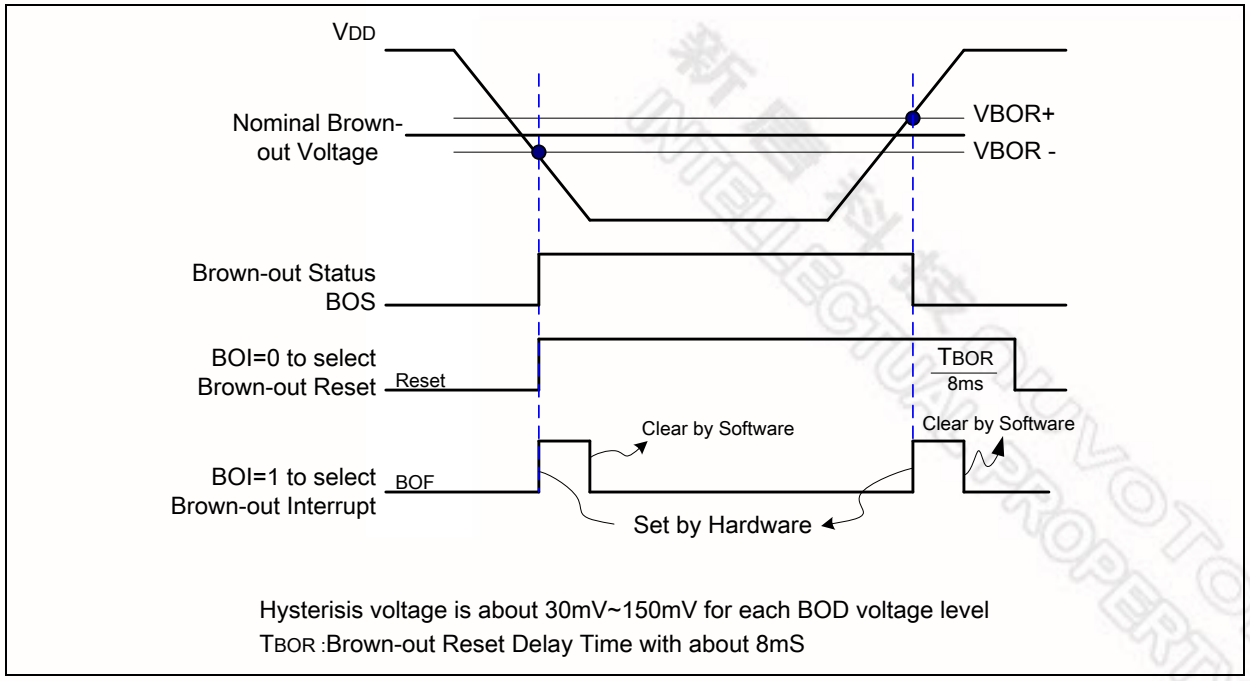


Figure 22-2: Brown-out Voltage Detection

Hysterisis range of brownout detect voltage is about 30mV to 150mV

Sink Current P1, P2, P3 (Quasi-bidirectional Mode)	I_{SK1}	13	20	24	mA	V_{DD} = 4.5V, V_S = 0.45V
		8	13	17	mA	V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV[1:0]=00	$V_{BO2.4}$	2.25	2.4	2.55	V	
Brownout voltage with BOV[1:0]=01	$V_{BO2.7}$	2.55	2.7	2.75	V	
Brownout voltage with BOV[1:0]=10	$V_{BO3.8}$	3.65	3.8	3.90	V	
Brownout voltage with BOV[1:0]=11	$V_{BO4.5}$	4.30	4.5	4.65	V	
Brownout detection current	I_{BO1}		160/135	210/170	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=0)
	I_{BO2}		24/11	32/15	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=1, 1/16 mode)
Hysterisis range of BOD voltage	V_{Bh}	35	-	150	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI) = (0,x) or (1,0)
		10	-	60	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI)=(1,1)
Power On Reset Voltage	V_{POR}	1.45	2.0	2.10	V	With Hysterisis ~= 450mV

Notes: *1. RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

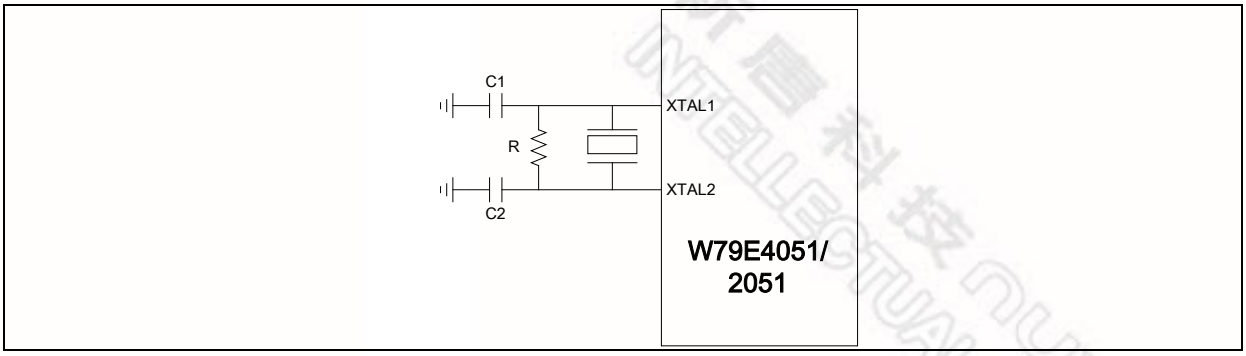
*3. Pins of P1, P2 and P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

25.3 The COMPARATOR ELECTRICAL CHARACTERISTICS

(VDD–VSS = 3.0~5V±10%, TA = -40~85°C, Fosc = 24MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	50	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}
Comparator offset voltage	V_{OFF}			20	mV	With decoupled capacitors on inputs

26 TYPICAL APPLICATION CIRCUITS

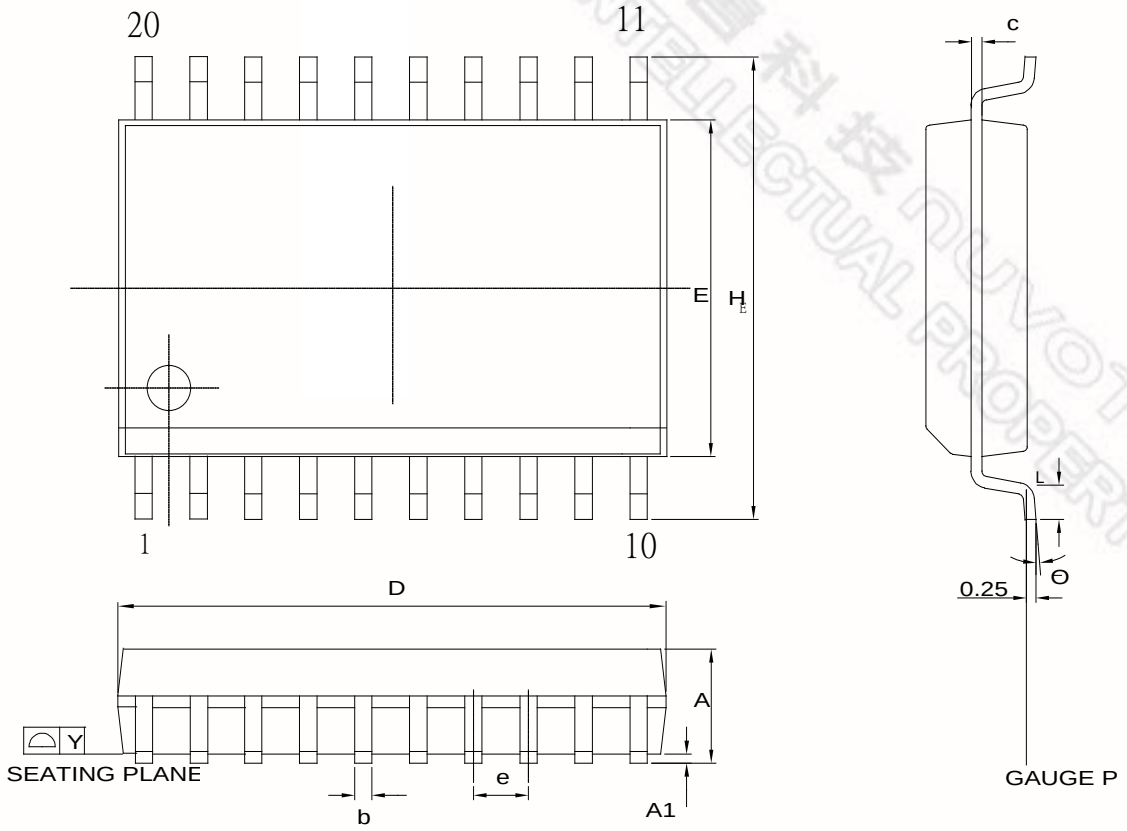


The table below shows the reference values for crystal applications.

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

27 PACKAGE DIMENSIONS

27.1 20-pin SOP

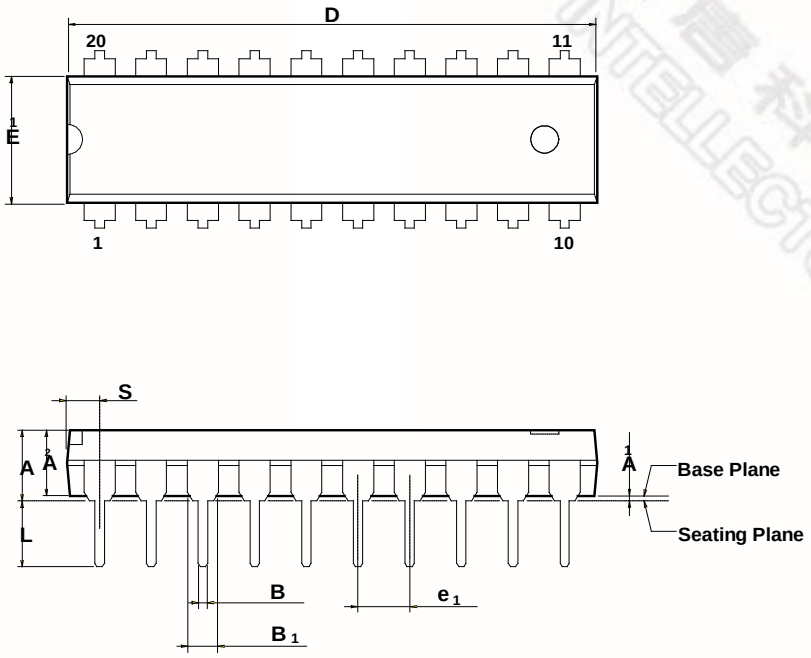


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Figure 27-1: 20L SOP-300mil

27.2 20-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

Figure 27-2: 20L DIP-300mil