Nuvoton Technology Corporation - W79E2051RARG Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e2051rarg

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz
- Single power: 2.4~5.5V Up to 12MHz, 4.5~5.5V up to 24MHz
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 24MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 22.1184/11.0592MHz with ±2% accuracy (selectable by config bit), at 5.0 voltage and 25℃condition, for W79E2051R and W79E4051R
- Instruction-set compatible with MCS-51
- **4K/2K** bytes of Program Flash EPROM, with ICP and external writer programmable mode.
- **256** bytes of on-chip RAM
- W79E4051/2051 supports **128** bytes Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
  - Data Flash program/erase V_{DD}=3.0V to 5.5V
- **One 8-bit** bi-directional port(Port1), **one 7-bit** bi-directional port(Port3) and **one 2-bit** bi-directional port(P2.0 and P2.1 shared with XT1 and XT2 pins)
- I/O capable of driving LED max. 20mA per pin, max to 80mA for total pins.
- **Two** 16-bit timer/counters
- **9** Interrupt source with four levels of priority
- **One** enhanced full duplex serial port with framing error detection and automatic address recognition
- **One** channel 10-bit PWM output
- **One** analog Comparator
- Built-in Power Management
  - Power on reset flag
  - Brownout voltage detect/reset
- Operating Temperature: -40~85℃
- Packages:
  - Lead Free (RoHS) PDIP 20: W79E4051AKG
  - Lead Free (RoHS) SOP 20: W79E4051ASG
  - Lead Free (RoHS) SSOP 20: W79E4051ARG
  - Lead Free (RoHS) PDIP 20: W79E2051AKG
  - Lead Free (RoHS) SOP 20: W79E2051ASG
  - Lead Free (RoHS) SSOP 20: W79E2051ARG
  - Lead Free (RoHS) PDIP 20: W79E4051RAKG
  - Lead Free (RoHS) SOP 20: W79E4051RASG
  - Lead Free (RoHS) SSOP 20: W79E4051RARG

Table 6-1: Data Pointer

6.7 Architecture

The W79E4051/2051 is based on the standard MCS-51 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard MCS-51 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E4051/2051. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump address. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E4051/2051. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E4051/2051 has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E4051/2051 has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E4051/2051. Hence the size of the stack is limited by the size of this RAM.

7 MEMORY ORGANIZATION

The W79E4051/2051 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E4051/2051 series can be up to **4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The Data Flash EPROM on the W79E4051/2051 series is **128** bytes long with page size of **16** bytes. The W79E4051/2051 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

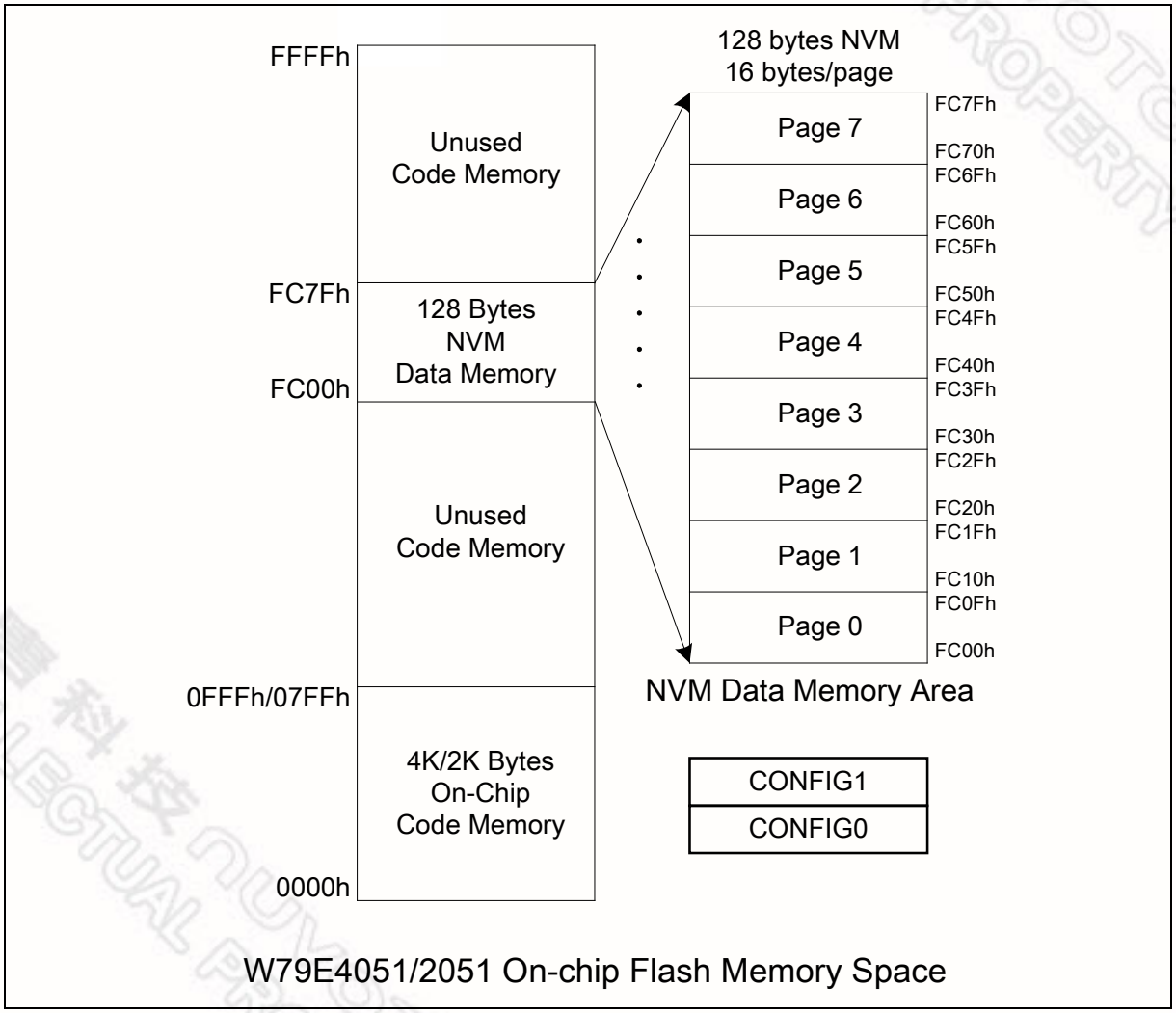


Table 7-1 W79E4051/2051 On-chip Flash Memory Map

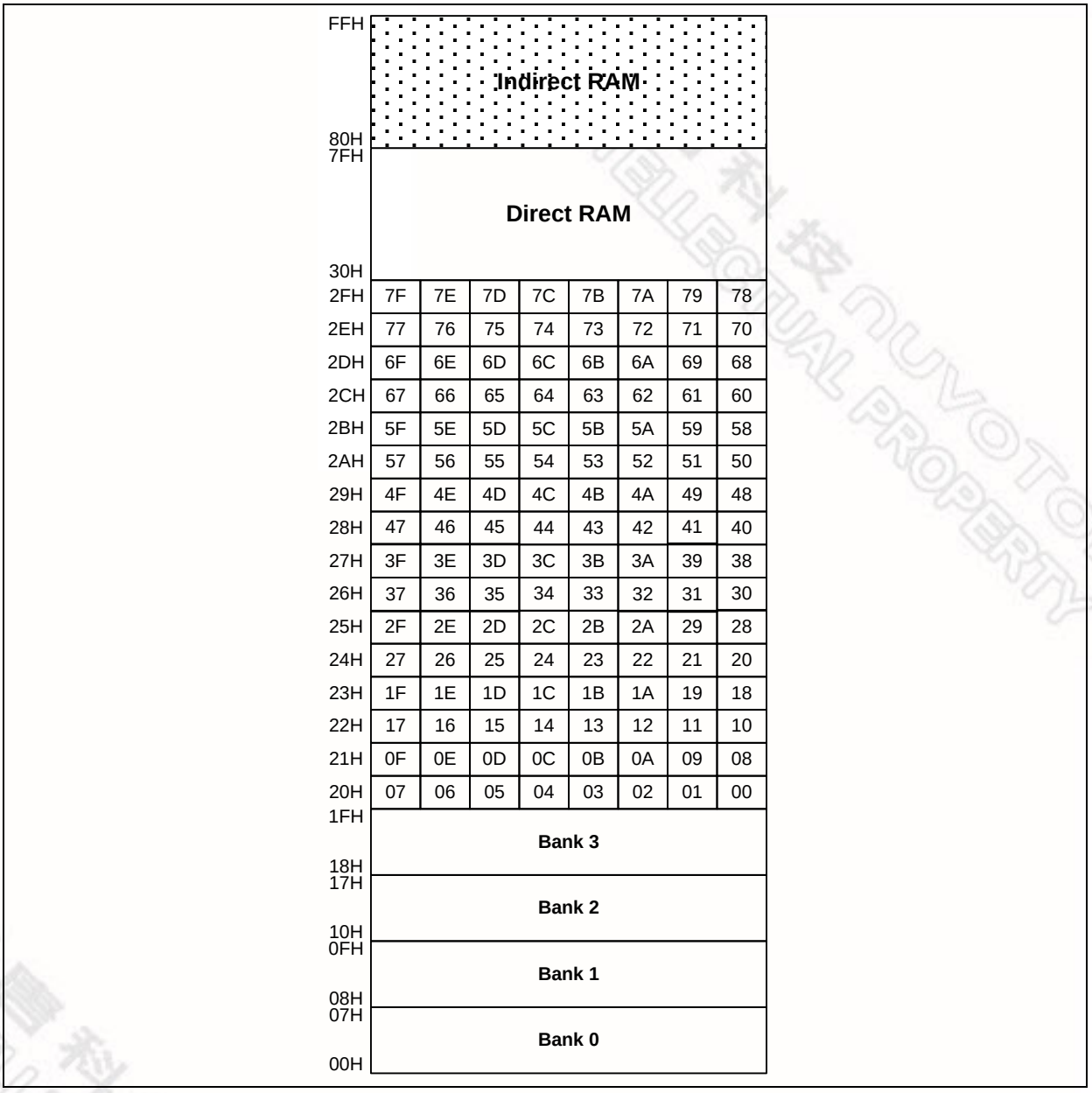


Table 7-3 Scratch-pad RAM

7.4 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E4051/2051 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 6 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 6 clocks.
2-0	-	Reserved.

CLOCK REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWDEX1	PWDEX0	-

Mnemonic: CLDREG Address: 8Fh

BIT	NAME	FUNCTION
7-5	-	Reserved.
2	PWDEX1	Power Down Exit Mode.
1	PWDEX0	Power Down Exit Mode.
0	-	Reserved.

Power Down Exit Mode:

PWDEX1	PWDEX0	Power Down Exit Mode
0	0	Wake up from Power Down is internally timed. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
0	1	Wake up from Power Down is externally controlled. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
1	x	Wake up from Power Down immediately. $\overline{INT0}$ or $\overline{INT1}$ can be configured for low-level or edge trigger mode.

7~2	-	Reserved.
1~0	PWM0.9~8	The PWM 0 Register bit 9~8.

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWM0OE	-	-	FP1	FP0

Mnemonic: PWMCON3 Address: D7h

Bit	Name	Function
7		
6		
5		
4	PWM0OE	PWM0 output enable bit. 0: PWM0 output disabled. 1: PWM0 output enabled. If P3.5 is set to high PWM0 will output through P3.5.
3~2	-	Reserved.
1~0	FP1~0	Select PWM frequency pre-scale select bits. The clock source of pre-scaler is in phase with Fosc if PWMRUN=1, otherwise it is disabled.

FP1~0: PWM Prescaler select bits:

FP[1:0]	Fpwm
00	FOSC
01	FOSC/2
10	FOSC/4
11	FOSC/16

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

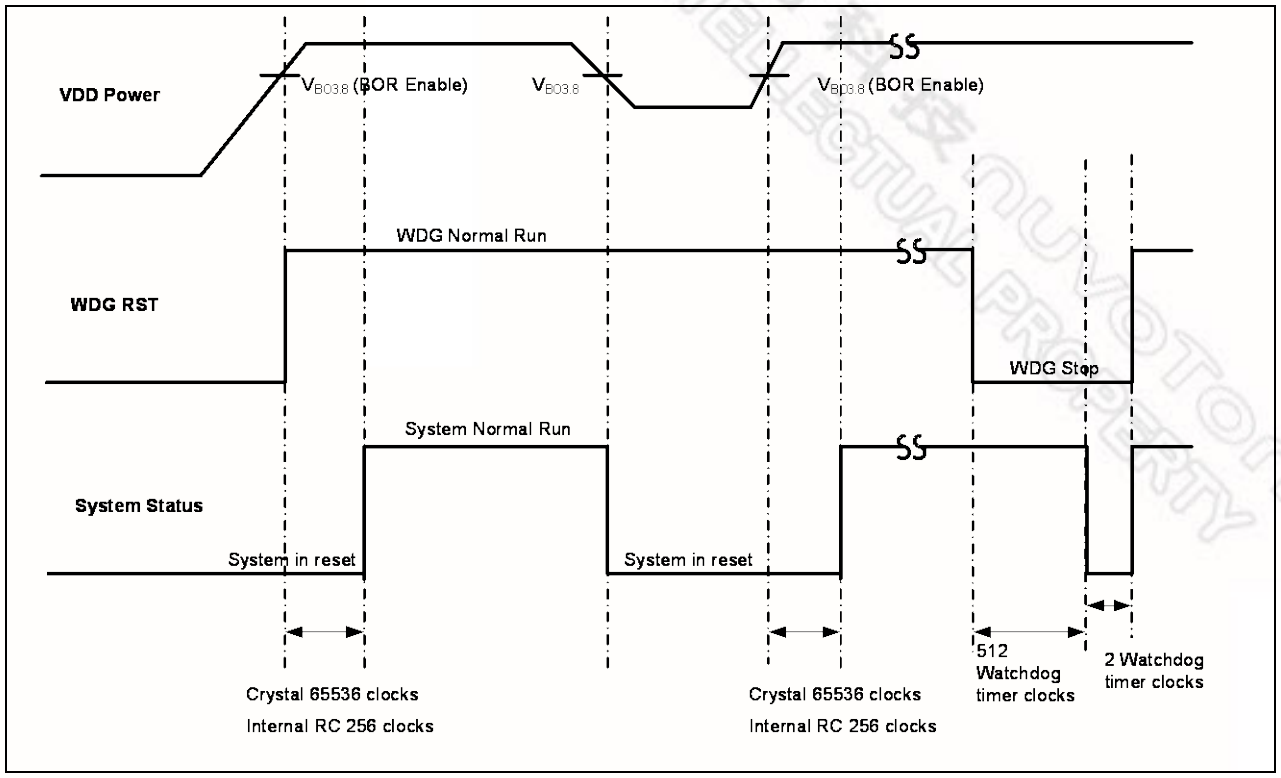


Figure 11-1: Internal reset and VDD monitor timing diagram

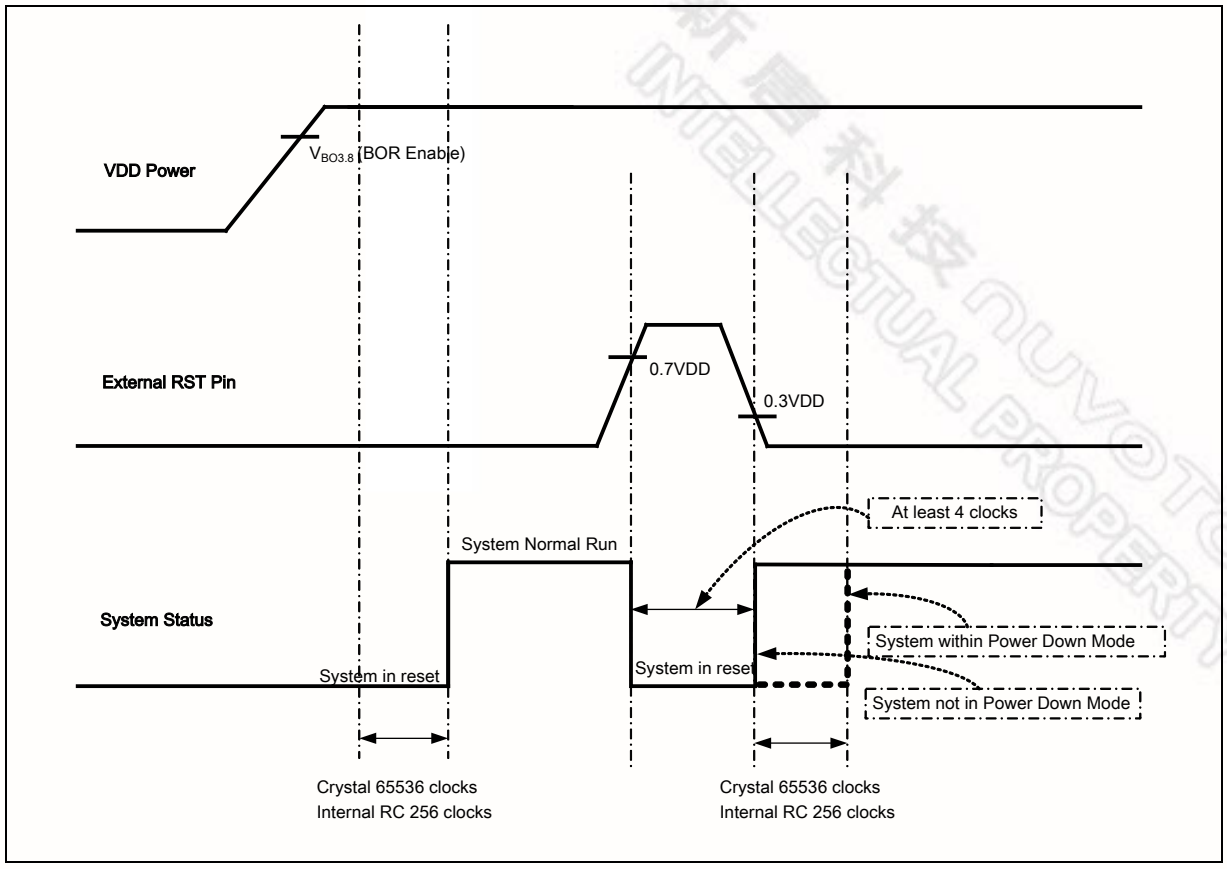


Figure 11-2: External reset timing diagram

speed. The reset, when enabled, will occur when 512 clocks after time-out has occurred.

WD1	WD0	Interrupt time-out	Reset time-out	Number of Clocks	Time @ 10 MHz
0	0	2^{17}	2^{17} + 512	131072	13.11 mS
0	1	2^{20}	2^{20} + 512	1048576	104.86 mS
1	0	2^{23}	2^{23} + 512	8388608	838.86 mS
1	1	2^{26}	2^{26} + 512	67108864	6710.89 mS

Table 15-1: Time-out values for the Watchdog Timer

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state. The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The **WDRUN, WD1, WD0, EWRST, WDIF and WDCLR** bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG register. This bit is used to configure the clock source of watchdog timer from either the internal RC or the uC clock.

When WDTCK bit is cleared and 500KHz clock is used to run the watchdog timer, there is a chance that the watchdog timer would hang as the counter does not increment. This problem arises when the watchdog is set to run, (WDCON.7, WDRUN), the WDCLR bit (WDCON.0) is set to clear the watchdog timer and the next instruction is to set the PCON register for CPU to go into idle or power-down state. The reason this happens because the setting/clearing of WDCLR bit and the watchdog counter are running on different clock domains, CPU clock and internal RC clock respectively. When

WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

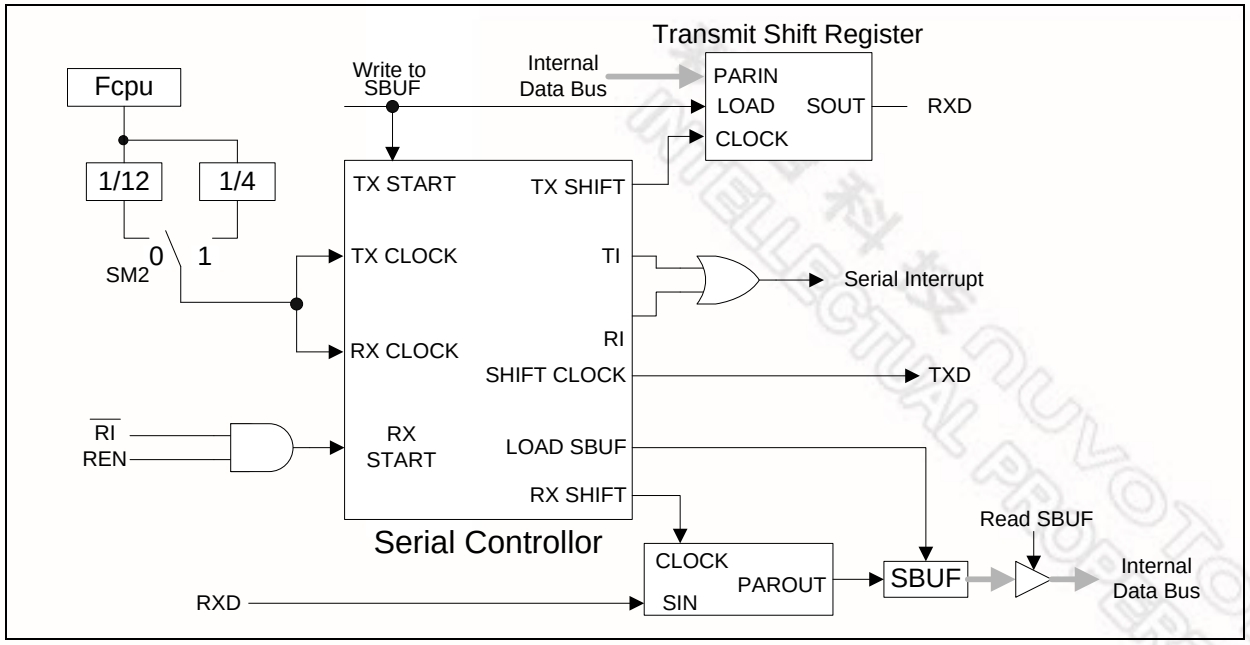


Figure 16-1: Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide-by-16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide–by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all aspects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

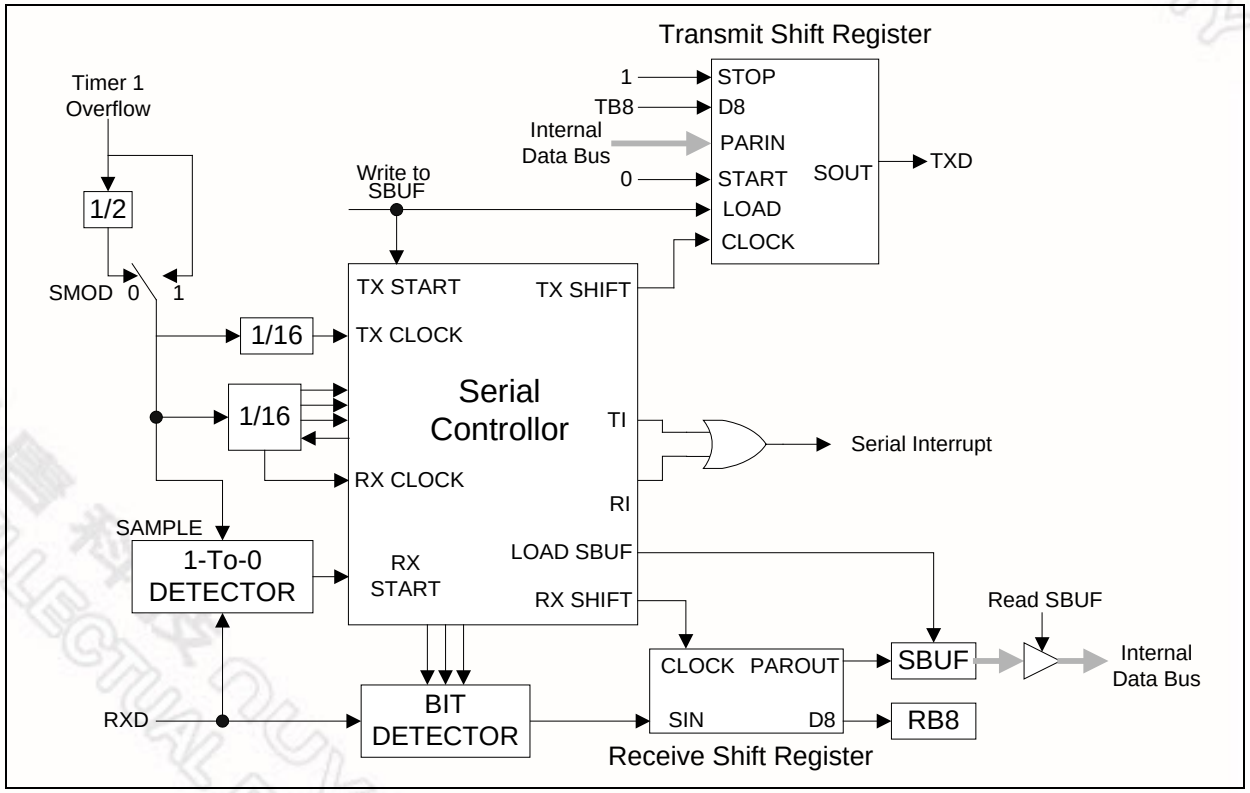


Figure 16-4: Serial Port Mode 3

17 PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E4051/2051 contains one Pulse Width Modulated (PWM) channel which generate pulses of programmable length and interval. The output for PWM0 is on P3.5. After chip reset the internal output of the PWM channel is high. In this case before the pin will reflect the state of the internal PWM output, a "1" must be written to the port bit that serves as a PWM output. A block diagram is shown in Figure 17-1. The interval between successive outputs is controlled by a 10–bit down counter which uses the internal microcontroller clock as its input. The PWM counter clock has the frequency as F_{CPWM} = P_{OSC}/Prescaler. The two pre-scaler selectable bits FP[1:0] are located at PWMCON3[1:0]. When the counter reaches underflow it is reloaded with a user selectable value. This mechanism allows the user to set the PWM frequency at any integer sub–multiple of the microcontroller clock frequency. The repetition frequency of the PWM is given by: f_{PWM} = F_{CPWM} / (PWMP+1) where PWMP is contained in PWMPH and PWMPL SFR.

A compare value greater than the counter reloaded value is in the PWM output being permanently low. In addition there are two special cases. A compare value of all zeroes, 000H, causes the output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remaining permanently low. Again the compare value is loaded into a Compare register. The transfer from this holding register to the actual Compare register is under program control.

The PWMP register fact that writes are not into the Counter register that controls the counter; rather they are into a holding register. As described below the transfer of data from this holding register, into the register which contains the actual reload value, is controlled by the user's program.

The width of PWM output pulse is determined by the value in the appropriate Compare registers, PWM0L and PWM0H. When the counter described above reaches underflow the PWM output is forced high. It remains high until the compare value is reached at which point it goes low and keeps low until the next underflow. The number of microcontroller clock pulses that the PWM0 output is high is given by:

t_{HI} = (PWMP – PWM0+1)

Note :

1. A compare value of all zeroes, 000H, causes the PWM output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remain permanently low. A compare value greater than the counter reloaded value will result in the PWM output being permanently low.
2. When the PWMRUN is cleared, the PWM outputs take on the state prior to the bit being cleared. In general, this state is not known. In order to place the PWM output in a known state when PWMRUN is cleared;
   - Program Compare Registers to either the "always 1" or "always 0" (see note 1).
   - Set Load (and PWMRUN) bits to 1.
   - Wait for PWMF underflow flag or Load bit (=0).
   - Clear PWMRUN.

18.1 Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs maybe cause the comparator output toggle excessively, especially applying slow moving analog inputs. Table 18-2: Comparator Interrupt Mode shows the 8 comparator interrupt modes set by CM[2:0] in ACSR(97H). A built-in configurable debouncing timer provides 8 debouncing timing controlled by CPCK[2:0] for widely applications. The debouncing timing is shown in Table 18-1. If CPU is in normal/Idle mode F_{DB} is from Fosc; if CPU is in power-down mode F_{DB} is from internal RC 22M/11M Hz oscillator.

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$
1	1	1	$(3/F_{DB})*256$~$(4/F_{DB})*256$

Table 18-1: Comparator Debouncing Time

CM2	CM1	CM0	Comparator interrupt mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

Table 18-2: Comparator Interrupt Mode

Three debouncing modes are provided to filter out this noise. In debouncing mode when the comparator output matches one of three debouncing mode condition, the debouncing timer resets and starts up-counting. The end of debouncing triggers the hardware to check if the comparator output matches the mode condition or not. If it is compliant with the mode condition the comparator flag CF is set by hardware, otherwise CF keeps low. Refer to Figure 18-2.

22 POWER MONITORING FUNCTION

In order to prevent incorrect operation during power up and power drop, the W79E4051/2051 is provided a power monitor function, Brownout Detect.

22.1 Brownout Detect and Reset

The W79E4051/2051 has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 4 nominal levels are 2.4V, 2.7V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatedly senses the voltage for 64/f_{BRC} then turn off detector for 960/ f_{BRC} if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator, is approximately 100K* V_{DD} HZ ±50%. The relative control bits are located in SFR AUXR1 @A2h. The Brownout Detect block is shown in Figure 22-1.

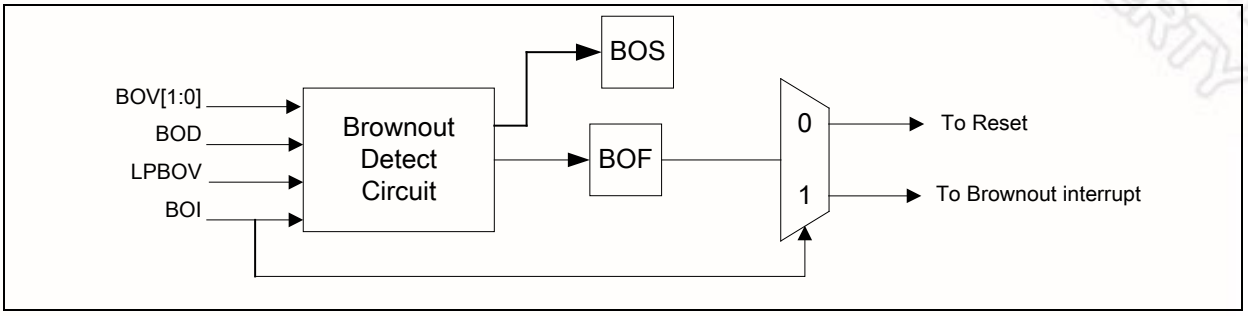


Figure 22-1: Brown-out Detect Block

25.2 DC ELECTRICAL CHARACTERISTICS

(VSS = 0V, TA =-40~85° C, unless otherwise specified; Typical value is test at TA=25° C)

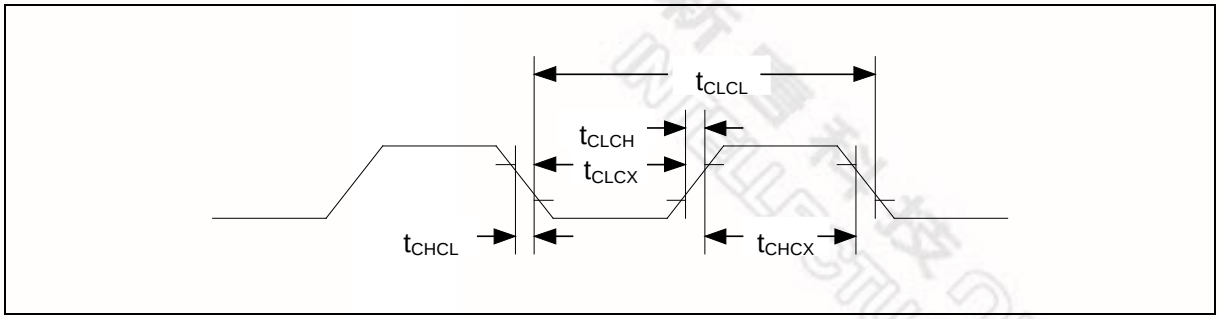
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=2.4V ~ 5.5V @ 12MHz V_{DD}=4.5V ~ 5.5V @ 24MHz
		3.0		5.5		Program and erase Data Flash.
Operating Current	I_{DD1}		2	3.5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 12MHz
	I_{DD2}		8	12	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 24MHz
Idle Current	I_{IDLE1}		1.6	2.5	mA	No load, V_{DD} = 3.0V @ 12MHz
	I_{IDLE2}		6.5	7.5	mA	No load, V_{DD} = 5.0V @ 24MHz
Power Down Current	I_{PWDN1}		0.5	10	µA	No load, V_{DD} = 5.0/3.0V (Brownout detection is disabled)
INPUT / OUTPUT						
Input Current P1, P2, P3	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current RST pin[1]	I_{IN2}	-55	-	-30	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P1.0, P1.1(Open Drain)	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL} [*3]	-450	-	-200	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD} =2.4 Vin = 1.3v
Input Low Voltage P1, P2, P3 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.4V
Input High Voltage P1, P2, P3 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (RST Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (RST Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage (RST Schmitt input)	V_{HY}		0.2V_{DD}		V	
Source Current P1, P2, P3 (Quasi-bidirectional Mode)	I_{SR1}	-150	-210	-360	µA	V_{DD} = 4.5V, V_S = 2.4V
		-18	-27	-40	µA	V_{DD} = 2.4V, V_S = 2.0V

25.3 The COMPARATOR ELECTRICAL CHARACTERISTICS

(VDD–VSS = 3.0~5V±10%, TA = -40~85°C, Fosc = 24MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	50	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}
Comparator offset voltage	V_{OFF}			20	mV	With decoupled capacitors on inputs

25.4 AC ELECTRICAL CHARACTERISTICS



Note: Duty cycle is 50%.

25.5 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	24	MHz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	18.8	-	-	nS	
Clock Low Time	t_{CLCX}	18.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

25.6 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
W79E2051/W79E4051 Frequency accuracy of On-chip RC oscillator (Without calibration)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
W79E2051R/W79E4051R On-chip RC oscillator with calibration[1,2] (Fosc = 22.1184MHz with factory calibration)	-2		2	%	V_{DD}=5.0V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		7	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.
2. RC frequency deviation vs. V_{DD} and Temperature is shown below