Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e4051akg

1 GENERAL DESCRIPTION

The W79E4051/2051 series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by **ICP (In Circuit Program) Writer**. The instruction set of the W79E4051/2051 series are fully compatible with the standard 8052. The W79E4051/2051 series contain a **4K/2K** bytes of program Flash EPROM; a **256** bytes of RAM; **128** bytes data Flash EPROM for customer data storage; two 8-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; an enhanced full duplex serial port; 1 channel PWM by 10-bit counter, Brownout voltage detection/reset, Power on reset detection and one analog comparator. These peripherals are supported by **9** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E4051/2051 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

7 MEMORY ORGANIZATION

The W79E4051/2051 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E4051/2051 series can be up to **4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The Data Flash EPROM on the W79E4051/2051 series is **128** bytes long with page size of **16** bytes. The W79E4051/2051 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

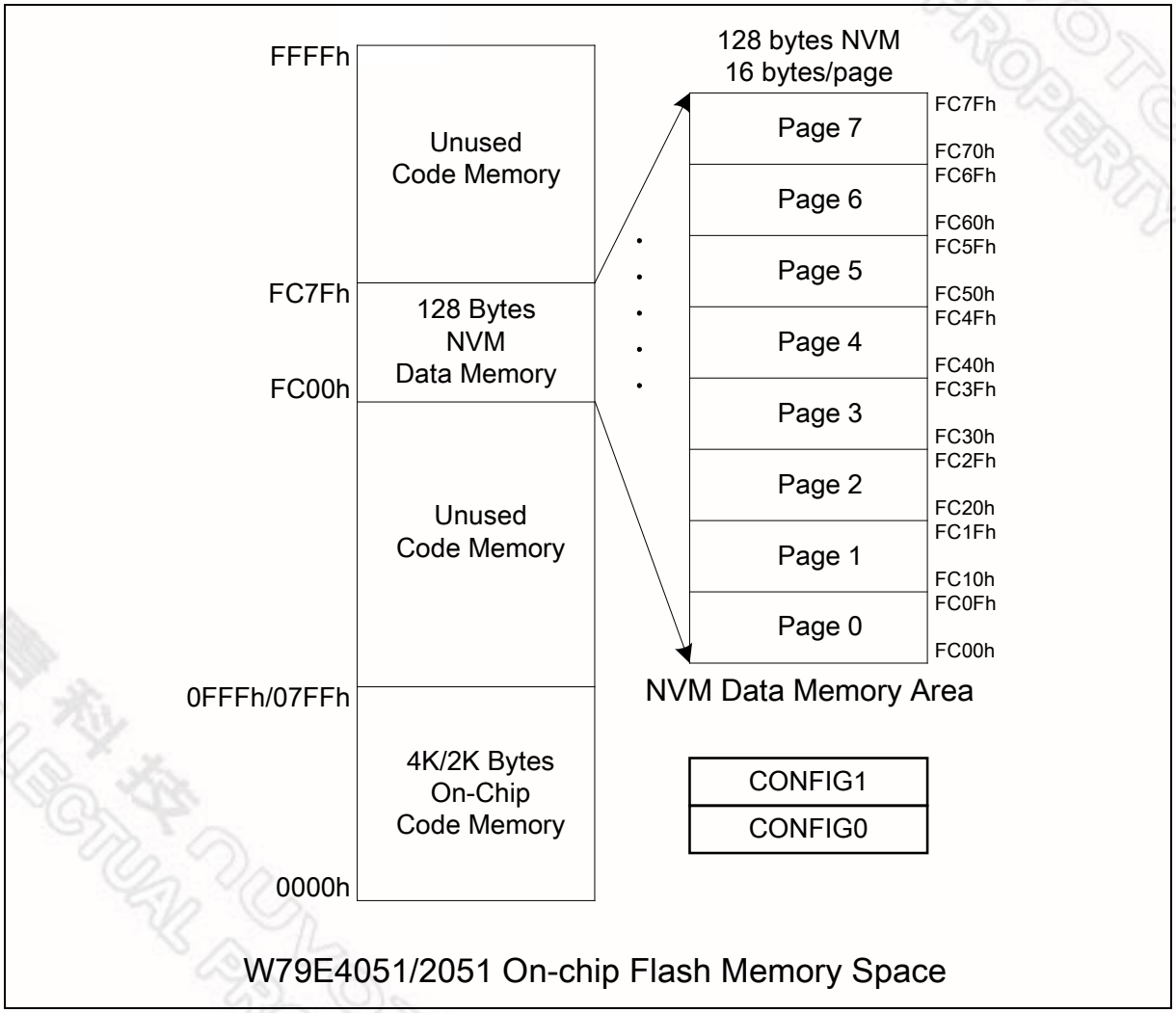

Table 7-1 W79E4051/2051 On-chip Flash Memory Map

Note :
1. In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.
2. BOD is initialized at reset with the inversed value of bit CBOD in config0-bits.
3. (BOV1,BOV0) are initialized at reset with the reversed value of config0-bits (CBOV1,CBOV0)

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	CIPE	Comparator Enabled in Idle and Power down Mode. 0: Comparator disabled in idle and power down mode. (default) 1: Comparator enabled in idle and power down mode.
4	CF	Comparator Interrupt Flag. Set by hardware when the comparator output meet the conditions specified by the CM[2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
3	CEN	Enable Comparator. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
2	CM2	See as below table.
1	CM1	See as below table.
0	CM0	See as below table.

Comparator Interrupt Mode Setting:

CM2	CM1	CM0	Interrupt Mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become

PWM COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

Bit	Name	Function
7~0	PWMP	PWM Counter Low Bits Register.

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

Bit	Name	Function
7~0	PWM0	PWM 0 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	-	PWM0I

Mnemonic: PWMCON1 Address: DCh

Bit	Name	Function
7	PWMRUN	Enable PWM running bit 0: The PWM is not running. 1: The PWM counter is running.
6	Load	Enable PWM counter and register re-load 0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow and hardware will clear by next clock cycle.
5	PWMF	PWM underflow flag. 0: No underflow. 1: PWM 10-bit down counter underflows (PWM interrupt is requested if PWM interrupt is enabled).
4	CLRPWM	Clear PWM counter 1: Clear 10-bit PWM counter to 000H. It is automatically cleared by hardware.
3~1	-	Reserved
0	PWM0I	Inverse PWM output level 0: PWM0 output is non-inverted. 1: PWM0 output is inverted.

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 9-1: Instruction Set for W79E4051/2051

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
					Follow the inverse of pin		
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	Hardware, Software	6	No
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	IP0H.4, IP0.4	Software	7	No
Comparator Interrupt	CF	0033H	EC (IE.6)	IP0H.6, IP0.6	Software	8	Yes(2)
PWM Period Interrupt	PWMF	006BH	EPWM (EIE.5)	IP1H.5, IP1.5	Software	9(lowest)	No

Table 12-3: Vector location for Interrupt sources and power down wakeup

Note:

1. The Watchdog Timer can wake up Power Down Mode when its clock source is from internal RC.
2. The comparator can wake up Power Down Mode when bit ACSR.5(CIPE) is set to high.

12.3 Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ to RI+TI, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W79E4051/2051 series are performing a write to IE, IP and IPH and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP or IPH access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycles is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

15 WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

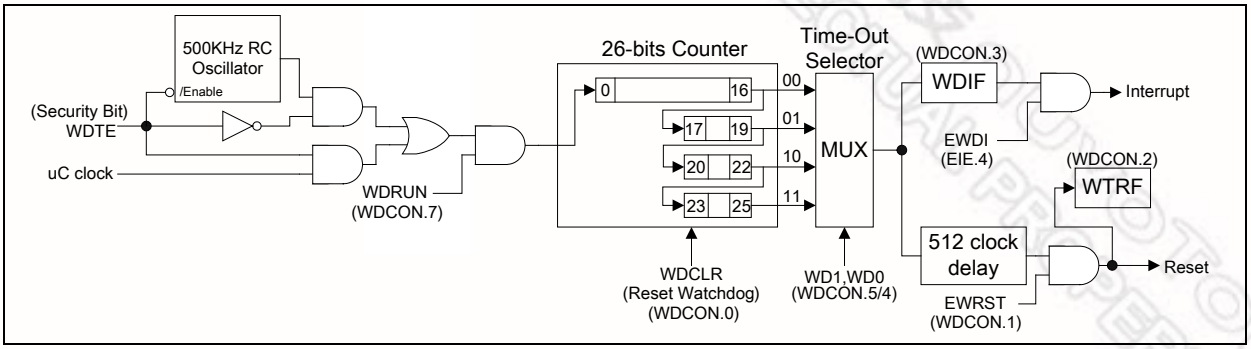

Figure 15-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 WDT clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock

WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

17 PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E4051/2051 contains one Pulse Width Modulated (PWM) channel which generate pulses of programmable length and interval. The output for PWM0 is on P3.5. After chip reset the internal output of the PWM channel is high. In this case before the pin will reflect the state of the internal PWM output, a "1" must be written to the port bit that serves as a PWM output. A block diagram is shown in Figure 17-1. The interval between successive outputs is controlled by a 10–bit down counter which uses the internal microcontroller clock as its input. The PWM counter clock has the frequency as F_{CPWM} = P_{OSC}/Prescaler. The two pre-scaler selectable bits FP[1:0] are located at PWMCON3[1:0]. When the counter reaches underflow it is reloaded with a user selectable value. This mechanism allows the user to set the PWM frequency at any integer sub–multiple of the microcontroller clock frequency. The repetition frequency of the PWM is given by: f_{PWM} = F_{CPWM} / (PWMP+1) where PWMP is contained in PWMPH and PWMPL SFR.

A compare value greater than the counter reloaded value is in the PWM output being permanently low. In addition there are two special cases. A compare value of all zeroes, 000H, causes the output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remaining permanently low. Again the compare value is loaded into a Compare register. The transfer from this holding register to the actual Compare register is under program control.

The PWMP register fact that writes are not into the Counter register that controls the counter; rather they are into a holding register. As described below the transfer of data from this holding register, into the register which contains the actual reload value, is controlled by the user's program.

The width of PWM output pulse is determined by the value in the appropriate Compare registers, PWM0L and PWM0H. When the counter described above reaches underflow the PWM output is forced high. It remains high until the compare value is reached at which point it goes low and keeps low until the next underflow. The number of microcontroller clock pulses that the PWM0 output is high is given by:

t_{HI} = (PWMP – PWM0+1)

Note :

1. A compare value of all zeroes, 000H, causes the PWM output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remain permanently low. A compare value greater than the counter reloaded value will result in the PWM output being permanently low.
2. When the PWMRUN is cleared, the PWM outputs take on the state prior to the bit being cleared. In general, this state is not known. In order to place the PWM output in a known state when PWMRUN is cleared;
   - Program Compare Registers to either the "always 1" or "always 0" (see note 1).
   - Set Load (and PWMRUN) bits to 1.
   - Wait for PWMF underflow flag or Load bit (=0).
   - Clear PWMRUN.

```
NOP                                 ;1 M/C
MOV         TA, #055h               ;3 M/C
SETB        EWT                     ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

20 I/O PORT MODE SETTING

W79E4051/2051 has maximum one 8-bit(P1), one 7-bit(P3) and one 2-bit(P2) ports. Except P1.0 and P1.1, all pins are quasi-bidirectional mode, which are common with standard 80C51, that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0 and P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset. The P2.0 (XTAL2) can be configured as clock output by setting bit ENCLK to high when CPU clock source is from on-chip RC or external Oscillator, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports except P1.0 and P1.1 output are in this mode, and output is common with the MCS-51. This mode can be used as both an input and output without the need to reconfigure the port. P1.0~P1.1 stays in PMOS-off open-drain mode after CPU reset.

P1M1.Y	PORT INPUT/OUTPUT MODE
0	Open Drain
1	Quasi-bidirectional

Table 20-1: I/O port Configuration Table

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current up to about 20mA/10mA at V_{DD}=5V/2.7V.

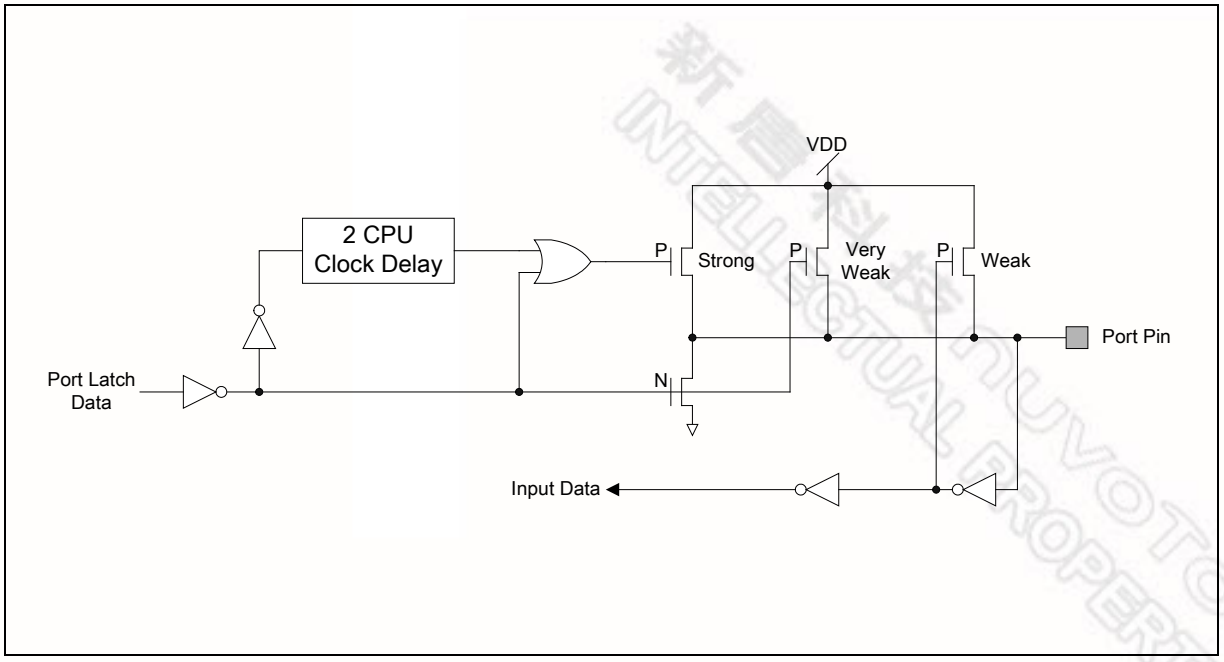

Figure 20-1: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

P1.0 and P1.1 are in open drain type after chip reset. To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

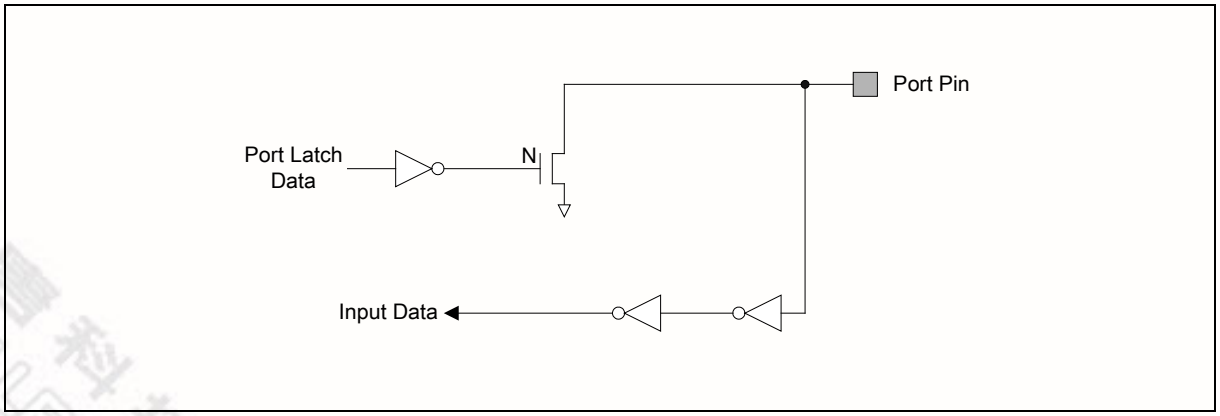

Figure 20-2: Open Drain Output

22 POWER MONITORING FUNCTION

In order to prevent incorrect operation during power up and power drop, the W79E4051/2051 is provided a power monitor function, Brownout Detect.

22.1 Brownout Detect and Reset

The W79E4051/2051 has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 4 nominal levels are 2.4V, 2.7V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatedly senses the voltage for 64/f_{BRC} then turn off detector for 960/ f_{BRC} if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator, is approximately 100K* V_{DD} HZ ±50%. The relative control bits are located in SFR AUXR1 @A2h. The Brownout Detect block is shown in Figure 22-1.

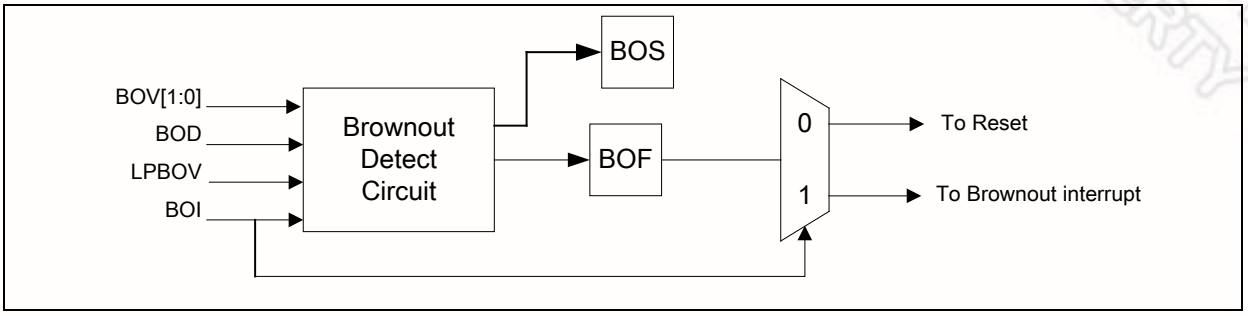

Figure 22-1: Brown-out Detect Block

24 CONFIG BITS

The W79E4051/2051 has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set by the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below.

24.1 CONFIG0

Config0

WDTCK	CBOV1	CBOV0	0	-	BPFR	Fosc1	Fosc0

Figure 24-1: Config0 register bits

Bit	Name	Function
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 500KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6~5	CBOV1 CBOV0	Brownout voltage selection bits: SFR bits (BOV1,BOV0) are initialized at reset with the inversed value of config0-bits (CBOV1,CBOV0)
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.
1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

CBOV.1	**CBOV.0**	**Brownout Voltage**
1	1	Brownout voltage is 2.4V
1	0	Brownout voltage is 2.7V
0	1	Brownout voltage is 3.8V
0	0	Brownout voltage is 4.5V

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 24MHz crystal
0	1	Internal RC Oscillator (FS1 bit in CONFIG1.5 will determine either 11MHz or 22MHZ) XT1 and XT2 function as P2.1 and P2.0
1	0	Reserved
1	1	External Oscillator in XTAL1; XT2 is in Tri-state

25 ELECTRICAL CHARACTERISTICS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
DC Power Supply	V_{DD}	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	TA		-40	+85	°C
Storage Temperature	Tst		-55	+150	°C
Sink current	ISK		-	95	mA
RAM Keep Alive Voltage	V_{RAM}		1.4	+7.0	V
Maximum Current into V_{DD}		-		120	mA
Maximum Current out of V_{SS}				120	mA
Maximum Current suck by a I/O pin				25	mA
Maximum Current sourced by a I/O pin				25	mA
Maximum Current suck by total I/O pins				80	mA
Maximum Current sourced by total I/O pins				80	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability