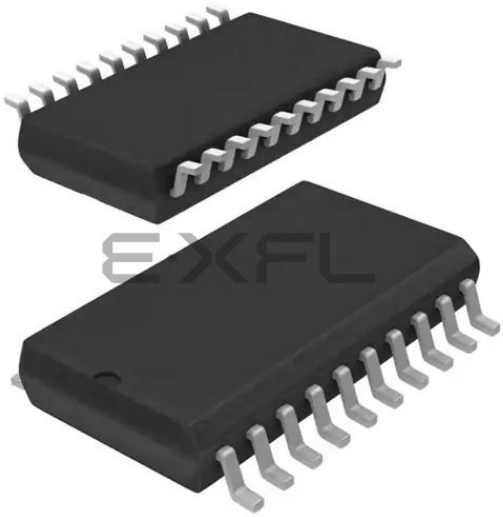

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e4051asg

- Lead Free (RoHS) PDIP 20: W79E2051RAKG
- Lead Free (RoHS) SOP 20: W79E2051RASG
- Lead Free (RoHS) SSOP 20: W79E2051RARG

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
W79E4051AKG	4KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E4051ASG	4KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E4051ARG	4KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E2051AKG	2KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E2051ASG	2KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E2051ARG	2KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E4051RAKG	4KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E4051RASG	4KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E4051RARG	4KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin
W79E2051RAKG	2KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E2051RASG	2KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E2051RARG	2KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin

Note:

1. Factory calibration condition: V_{DD}=5.0V, TA = 25°C

Table 6-1: Data Pointer

6.7 Architecture

The W79E4051/2051 is based on the standard MCS-51 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard MCS-51 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E4051/2051. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump address. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E4051/2051. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E4051/2051 has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E4051/2051 has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E4051/2051. Hence the size of the stack is limited by the size of this RAM.

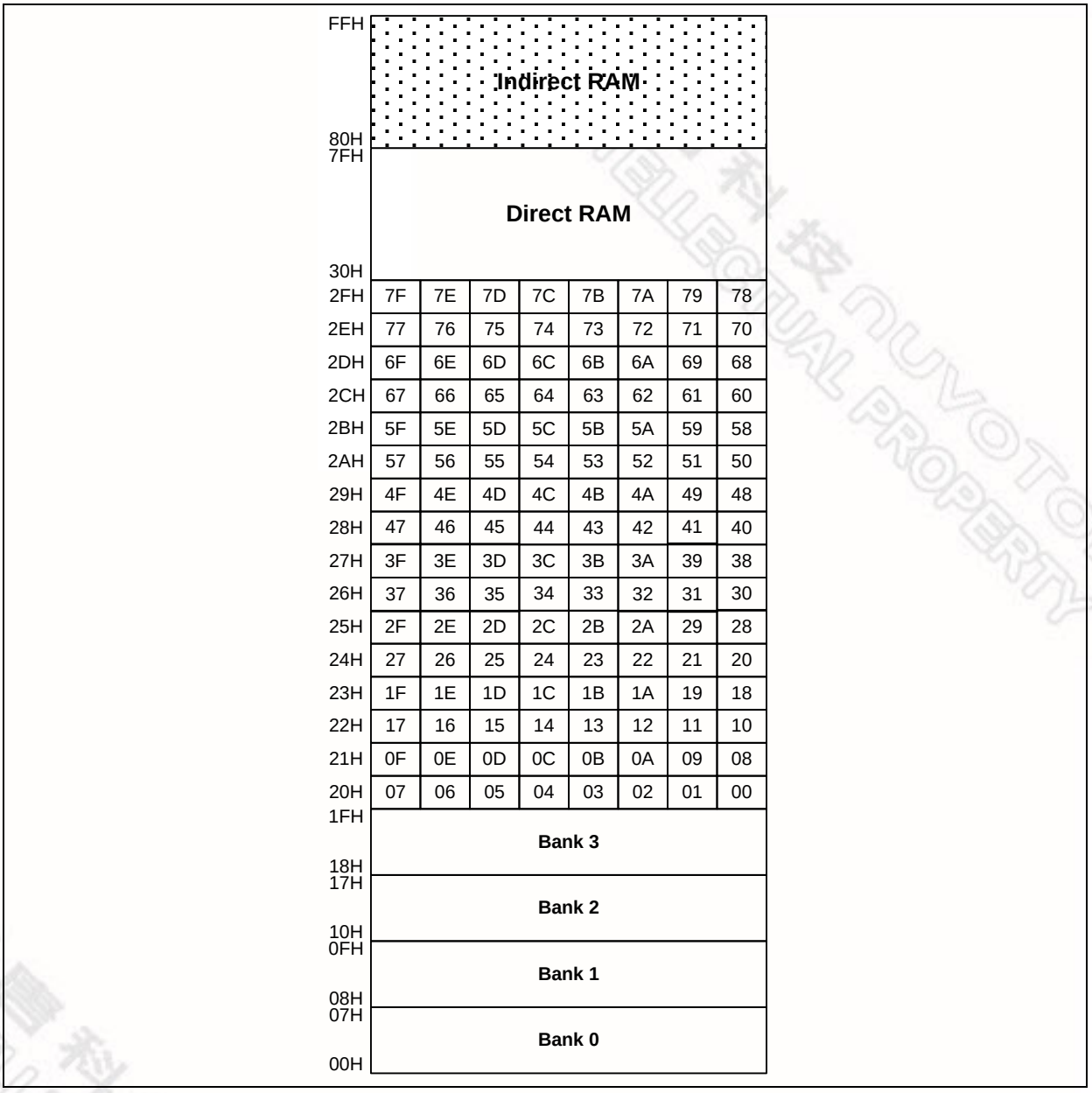


Table 7-3 Scratch-pad RAM

7.4 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E4051/2051 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1

Interrupt Priority 0

Bit:	7	6	5	4	3	2	1	0
	-	PC	-	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PC	1: To set interrupt priority of analog comparator is higher priority level.
5	-	This bit is un-implemented and will read high.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

NVM BYTE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDRL Address: C6h

BIT	NAME	FUNCTION
7	NVMADDR.7	Must be 0.
6~0	NVMADDR.[6:0]	The NVM low byte address: The register indicates NVM data memory address on On-Chip code memory space.

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register bank selection bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	PWMP.[9:8]	The PWM Counter Register bits 9~8.

PWM 0 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION

<table>
<tr><td>5~4</td><td>WD1~WD0</td><td>Watchdog Timer Time-out Select bits. These bits determine the time-out period of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out.
<table>
<tr><th>WD1</th><th>WD0</th><th>Interrupt time-out</th><th>Reset time-out</th></tr>
<tr><td>0</td><td>0</td><td>2^{17}</td><td>2^{17} + 512</td></tr>
<tr><td>0</td><td>1</td><td>2^{20}</td><td>2^{20} + 512</td></tr>
<tr><td>1</td><td>0</td><td>2^{23}</td><td>2^{23} + 512</td></tr>
<tr><td>1</td><td>1</td><td>2^{26}</td><td>2^{26} + 512</td></tr>
</table></td></tr>
<tr><td>3</td><td>WDIF</td><td>Watchdog Timer Interrupt flag:
0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.</td></tr>
<tr><td>2</td><td>WTRF</td><td>Watchdog Timer Reset flag:
1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.</td></tr>
<tr><td>1</td><td>EWRST</td><td>0: Disable Watchdog Timer Reset.
1: Enable Watchdog Timer Reset.</td></tr>
<tr><td>0</td><td>WDCLR</td><td>Reset Watchdog Timer:
This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt (if EWDI (EIE.4) is set), and 512 clocks after that a watchdog timer reset will be generated (if EWRST is set). This bit is self-clearing by hardware.</td></tr>
</table>

The WDCON SFR is set to a 0x000000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

All the bits in this SFR have unrestricted read access. WDRUN, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH                ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0                 ; Reset watchdog timer
ORL     WDCON, #00110000B       ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B       ; Enable watchdog
```

PWM COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

Bit	Name	Function
7~0	PWMP	PWM Counter Low Bits Register.

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

Bit	Name	Function
7~0	PWM0	PWM 0 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	-	PWM0I

Mnemonic: PWMCON1 Address: DCh

Bit	Name	Function
7	PWMRUN	Enable PWM running bit 0: The PWM is not running. 1: The PWM counter is running.
6	Load	Enable PWM counter and register re-load 0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow and hardware will clear by next clock cycle.
5	PWMF	PWM underflow flag. 0: No underflow. 1: PWM 10-bit down counter underflows (PWM interrupt is requested if PWM interrupt is enabled).
4	CLRPWM	Clear PWM counter 1: Clear 10-bit PWM counter to 000H. It is automatically cleared by hardware.
3~1	-	Reserved
0	PWM0I	Inverse PWM output level 0: PWM0 output is non-inverted. 1: PWM0 output is inverted.

0	PCMPIDS.0	P1.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of Comparator Input 1(Positive end)

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	-	PBOVH	PPWMH	PWDIH	-	-	-	-

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	-	Reserved.
6	PBOVH	1: To set interrupt priority of Brownout interrupt is highest priority level.
5	PPWMH	1: To set interrupt priority of PWM underflow is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3-0	-	Reserved.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PBOV	PPWM	PWDI	-	-	-	-

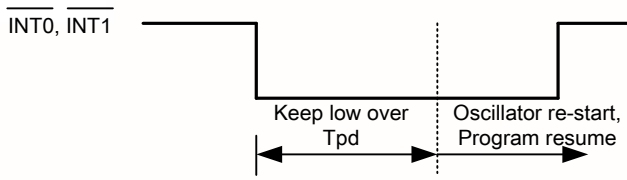
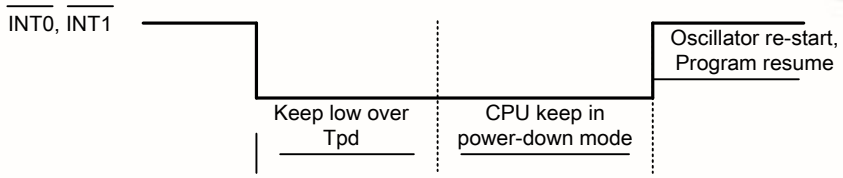
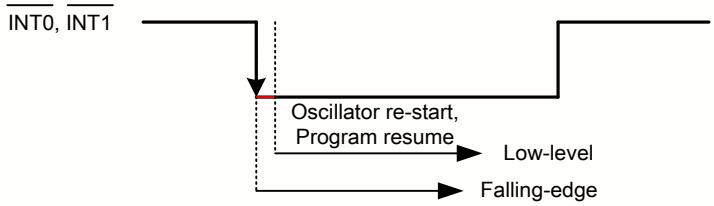
Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	PBOV	1: To set interrupt priority of Brownout interrupt is higher priority level.
5	PPWM	1: To set interrupt priority of PWM underflow is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-0	-	Reserved.

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3

CIPE=1). The W79E4051/2051 series can be waken up from the Power Down mode by forcing the above sources activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then interrupt event will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

In W79E4051/2051 series either a *low-level or a falling-edge at external interrupt pin,* $\overline{\text{INT1}}$ or $\overline{\text{INT0}}$ ***will re-start the oscillator. W79E4051/2051 provides 3 wake-up modes, selected by SFR bits PWDEX1 and PWDEX0, that the external interrupt pins can terminate power-down mode. Refer to the table below.***

PWDEX[1:0]	TRIGGER TYPE	FUNCTION TO TERMINATE POWER-DOWN MODE
0, 0 (Mode1)	Low-level	
0, 1 (Mode2)	Low-level	
1, x (Mode3)	Low-level and Falling-edge	

In mode1 and mode2, the external interrupt pin must keep low longer than Tpd otherwise CPU stays in power-down mode continuously. Tpd is about 2mS counted by built-in RC oscillator.

17 PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E4051/2051 contains one Pulse Width Modulated (PWM) channel which generate pulses of programmable length and interval. The output for PWM0 is on P3.5. After chip reset the internal output of the PWM channel is high. In this case before the pin will reflect the state of the internal PWM output, a "1" must be written to the port bit that serves as a PWM output. A block diagram is shown in Figure 17-1. The interval between successive outputs is controlled by a 10–bit down counter which uses the internal microcontroller clock as its input. The PWM counter clock has the frequency as F_{CPWM} = P_{OSC}/Prescaler. The two pre-scaler selectable bits FP[1:0] are located at PWMCON3[1:0]. When the counter reaches underflow it is reloaded with a user selectable value. This mechanism allows the user to set the PWM frequency at any integer sub–multiple of the microcontroller clock frequency. The repetition frequency of the PWM is given by: f_{PWM} = F_{CPWM} / (PWMP+1) where PWMP is contained in PWMPH and PWMPL SFR.

A compare value greater than the counter reloaded value is in the PWM output being permanently low. In addition there are two special cases. A compare value of all zeroes, 000H, causes the output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remaining permanently low. Again the compare value is loaded into a Compare register. The transfer from this holding register to the actual Compare register is under program control.

The PWMP register fact that writes are not into the Counter register that controls the counter; rather they are into a holding register. As described below the transfer of data from this holding register, into the register which contains the actual reload value, is controlled by the user's program.

The width of PWM output pulse is determined by the value in the appropriate Compare registers, PWM0L and PWM0H. When the counter described above reaches underflow the PWM output is forced high. It remains high until the compare value is reached at which point it goes low and keeps low until the next underflow. The number of microcontroller clock pulses that the PWM0 output is high is given by:

t_{HI} = (PWMP – PWM0+1)

Note :

1. A compare value of all zeroes, 000H, causes the PWM output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remain permanently low. A compare value greater than the counter reloaded value will result in the PWM output being permanently low.
2. When the PWMRUN is cleared, the PWM outputs take on the state prior to the bit being cleared. In general, this state is not known. In order to place the PWM output in a known state when PWMRUN is cleared;
   - Program Compare Registers to either the "always 1" or "always 0" (see note 1).
   - Set Load (and PWMRUN) bits to 1.
   - Wait for PWMF underflow flag or Load bit (=0).
   - Clear PWMRUN.

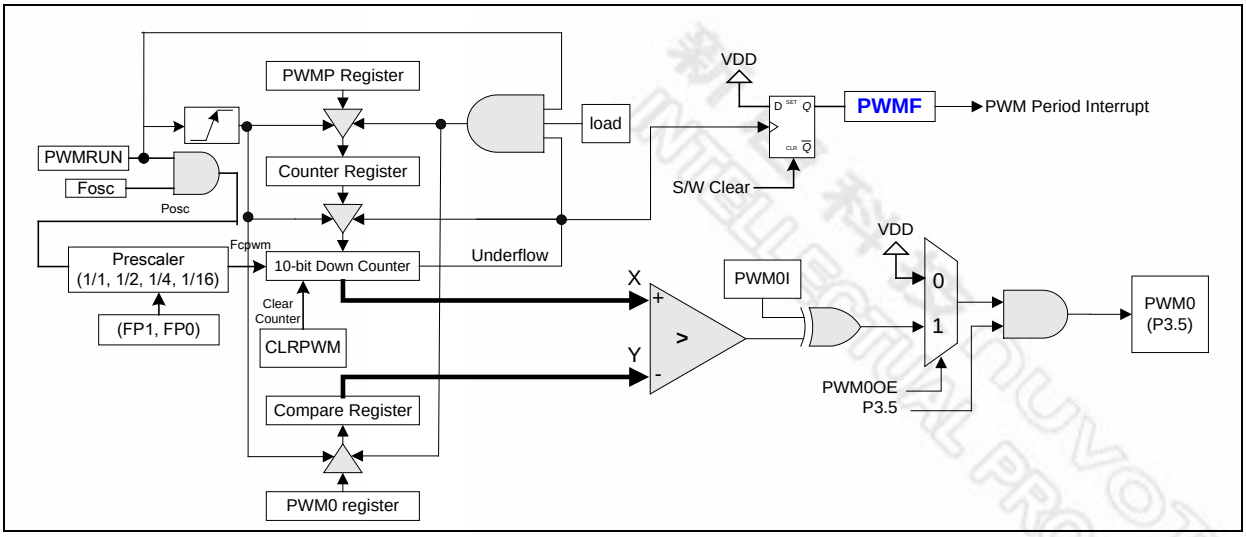


Figure 17-1: PWM block diagram

18 ANALOG COMPARATORS

The W79E4051/2051 is provided an Analog Comparator shown in Figure 18-1. The comparator output is wired to SFR bit P3.6. When the positive input of AIN0(P1.0) is greater than the negative input of AIN1(P1.1), the comparator output is high. Otherwise the output is low.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting bits CM[2:0] in ACSR(97H) register and bits CPCK[2:0] in ACCK(96H) register. The CF flag is set whenever the comparator output is matched the setting condition by CM[2:0].

Setting bit CIPE(Comparator Idle Power-down Enable) in ACSR.5 to high makes the analog comparator is active in power-down and idle mode, therefore the comparator interrupt can wake up CPU from power down and idle mode.

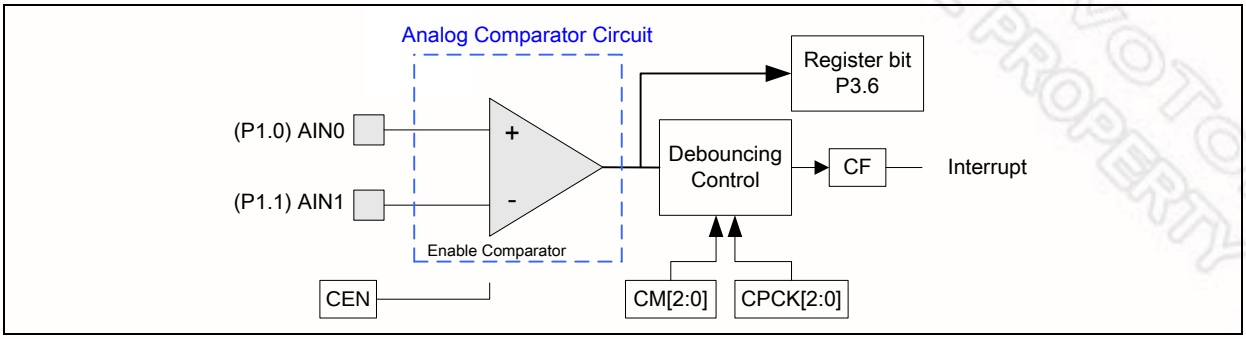


Figure 18-1: Analog Comparator

19 TIME ACCESS PROCTECTION

The W79E4051/2051 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E4051/2051 series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h            ;Define new register TA, @0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
        MOV     TA, #0AAh       ;3 M/C  Note: M/C = Machine Cycles
        MOV     TA, #055h       ;3 M/C
        MOV     WDCON, #00h     ;3 M/C
```

Example 2: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        SETB    EWRST           ;2 M/C
```

Example 3: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        ORL     WDCON, #00000010B ;3M/C
```

Example 4: Invalid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        NOP                     ;1 M/C
        CLR     EWT             ;2 M/C
```

Example 5: Invalid Access

```
        MOV     TA, #0AAh       ;3 M/C
```

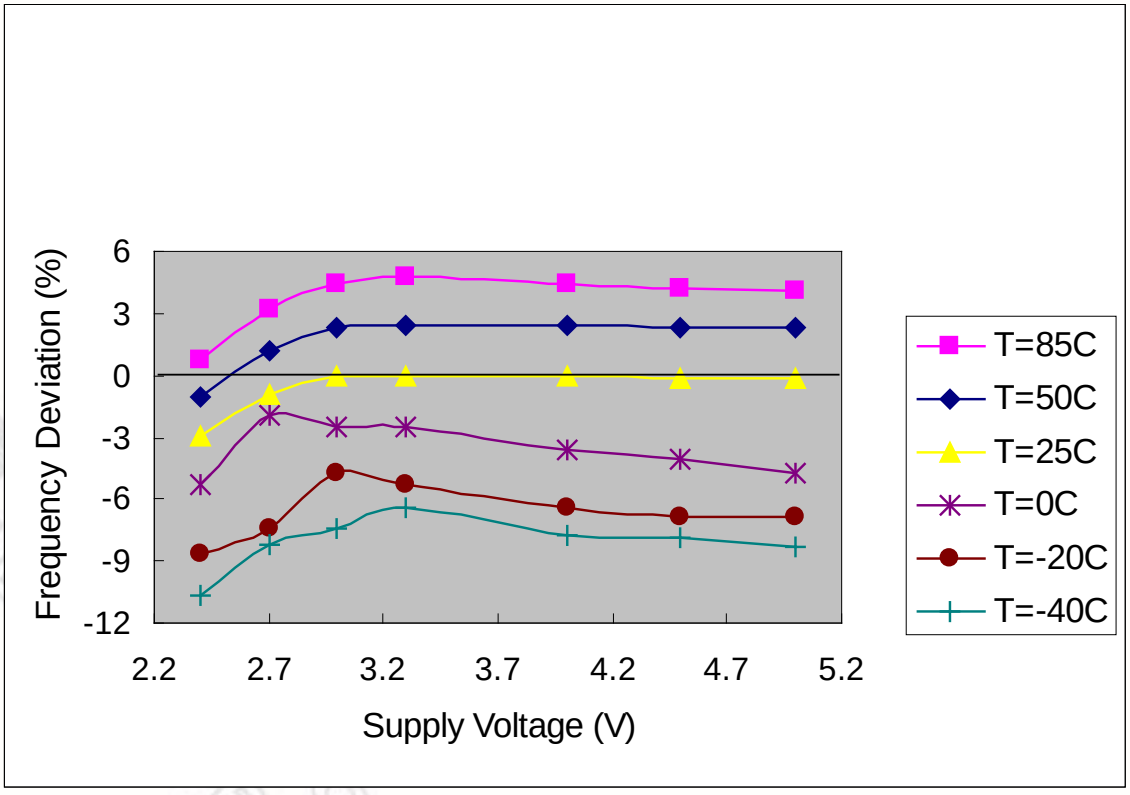
25.6 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

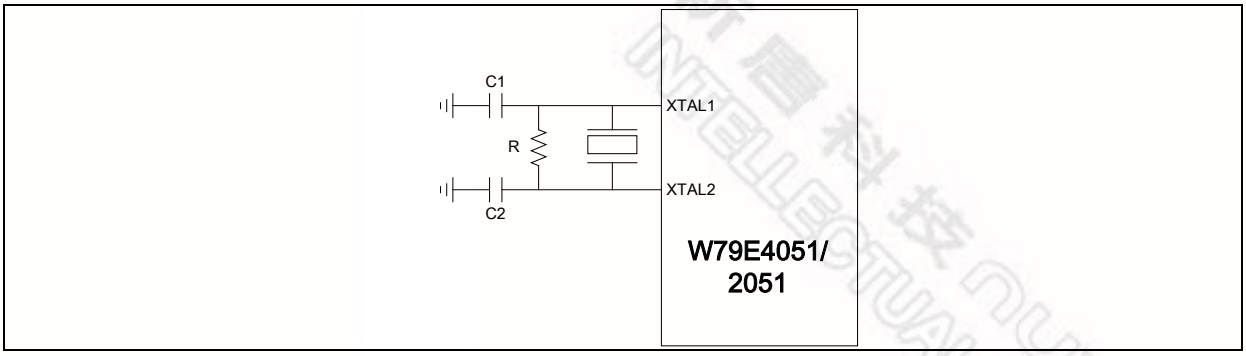
Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
W79E2051/W79E4051 Frequency accuracy of On-chip RC oscillator (Without calibration)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
W79E2051R/W79E4051R On-chip RC oscillator with calibration[1,2] (Fosc = 22.1184MHz with factory calibration)	-2		2	%	V_{DD}=5.0V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		7	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.
2. RC frequency deviation vs. V_{DD} and Temperature is shown below



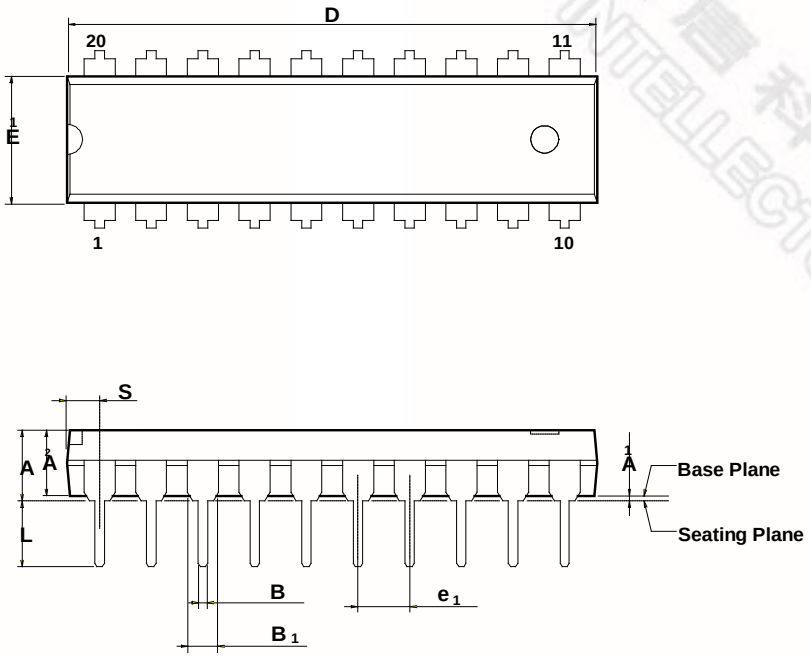
26 TYPICAL APPLICATION CIRCUITS



The table below shows the reference values for crystal applications.

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

27.2 20-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

Figure 27-2: 20L DIP-300mil