Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e4051rakg

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz
- Single power: 2.4~5.5V Up to 12MHz, 4.5~5.5V up to 24MHz
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 24MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 22.1184/11.0592MHz with ±2% accuracy (selectable by config bit), at 5.0 voltage and 25℃condition, for W79E2051R and W79E4051R
- Instruction-set compatible with MCS-51
- **4K/2K** bytes of Program Flash EPROM, with ICP and external writer programmable mode.
- **256** bytes of on-chip RAM
- W79E4051/2051 supports **128** bytes Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
  - Data Flash program/erase V_{DD}=3.0V to 5.5V
- **One 8-bit** bi-directional port(Port1), **one 7-bit** bi-directional port(Port3) and **one 2-bit** bi-directional port(P2.0 and P2.1 shared with XT1 and XT2 pins)
- I/O capable of driving LED max. 20mA per pin, max to 80mA for total pins.
- **Two** 16-bit timer/counters
- **9** Interrupt source with four levels of priority
- **One** enhanced full duplex serial port with framing error detection and automatic address recognition
- **One** channel 10-bit PWM output
- **One** analog Comparator
- Built-in Power Management
  - Power on reset flag
  - Brownout voltage detect/reset
- Operating Temperature: -40~85℃
- Packages:
  - Lead Free (RoHS) PDIP 20: W79E4051AKG
  - Lead Free (RoHS) SOP 20: W79E4051ASG
  - Lead Free (RoHS) SSOP 20: W79E4051ARG
  - Lead Free (RoHS) PDIP 20: W79E2051AKG
  - Lead Free (RoHS) SOP 20: W79E2051ASG
  - Lead Free (RoHS) SSOP 20: W79E2051ARG
  - Lead Free (RoHS) PDIP 20: W79E4051RAKG
  - Lead Free (RoHS) SOP 20: W79E4051RASG
  - Lead Free (RoHS) SSOP 20: W79E4051RARG

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
W79E4051AKG	4KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E4051ASG	4KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E4051ARG	4KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E2051AKG	2KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E2051ASG	2KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E2051ARG	2KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E4051RAKG	4KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E4051RASG	4KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E4051RARG	4KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin
W79E2051RAKG	2KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E2051RASG	2KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E2051RARG	2KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin

Note:

1. Factory calibration condition: V_{DD}=5.0V, TA = 25°C

4 PIN CONFIGURATION

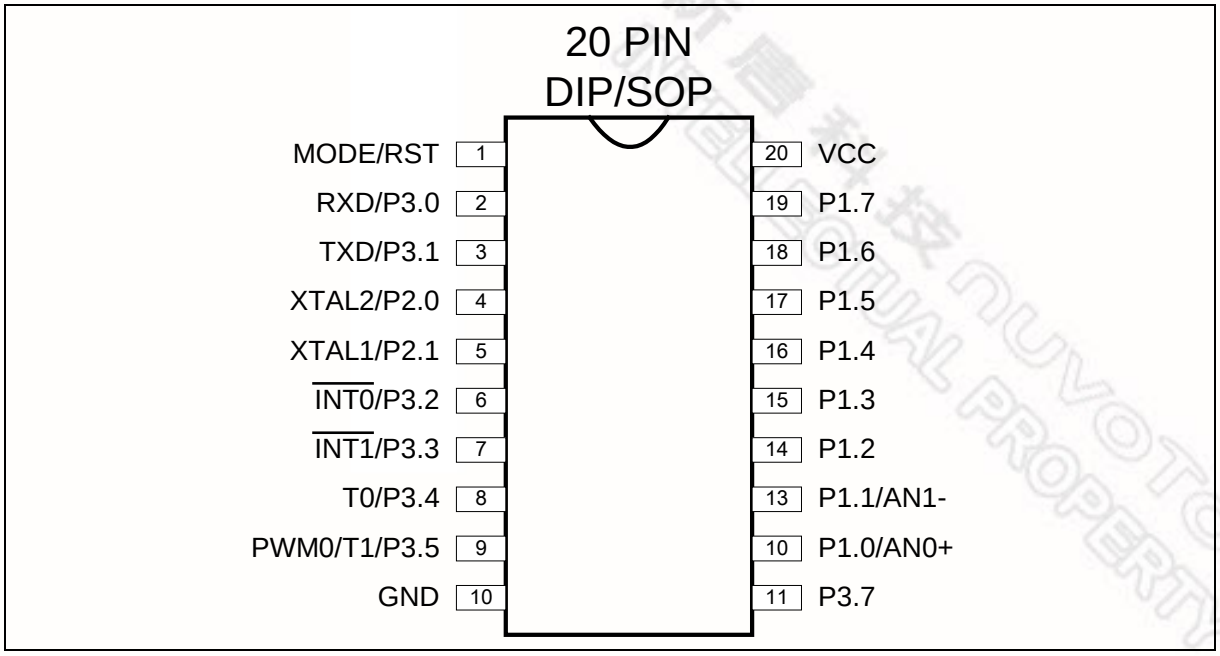


Table 4-1: Pin Configuration

7.3 Scratch-pad RAM and Register Map

As mentioned before the W79E4051/2051 series have separate Program and Data Memory areas. The on-chip **256** bytes scratch pad RAM is built in W79E4051/2051. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

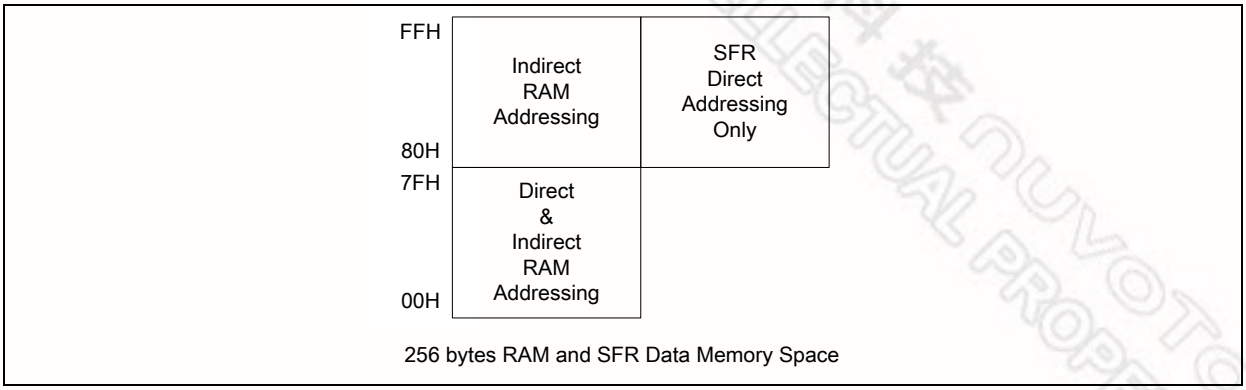


Table 7-2 W79E4051/2051 256 bytes RAM and SFR memory map

Since the scratch-pad RAM is **256** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

1	1	Brownout voltage is 4.5V

All the bits in this SFR have unrestricted read access. **SRST** require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

AUX FUNCTION REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS

Mnemonic: AUXR2 Address: A3h

BIT	NAME	FUNCTION
7-1	-	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EC	-	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EC	Enable analog comparator interrupt.
5	-	Reserved.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3

10 POWER MANAGEMENT

The W79E4051/2051 series has several features that help the user to control the power consumption of the device. These modes are discussed in the next two sections.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer, PWM, Analog Comparator(CIPE=1) and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E4051/2051 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

P1.0 and P1.1 should be set to 1 if external pull-ups are applied, or set to 0 if without external pull-ups, or configured to quasi I/O mode by setting P1M1 bit0 and bit1 to high.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity, exception of Brownout reset, $\overline{INT1}$, $\overline{INT0}$, watchdog timer(Config0.WDTCK=0) and Analog Comparator(CIPE=1), is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

Before CPU enters power-down mode, P1.0 and P1.1 should be set to 1 if external pull-ups are applied, or set to 0 if without external pull-ups, or configured to quasi I/O mode by setting P1M1 bit0 and bit1 to high.

An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, brownout reset (BOR), watchdog timer interrupt (if Config0 bit WDTCK = 0) and Analog Comparator(if SFR bit

speed. The reset, when enabled, will occur when 512 clocks after time-out has occurred.

WD1	WD0	Interrupt time-out	Reset time-out	Number of Clocks	Time @ 10 MHz
0	0	2^{17}	2^{17} + 512	131072	13.11 mS
0	1	2^{20}	2^{20} + 512	1048576	104.86 mS
1	0	2^{23}	2^{23} + 512	8388608	838.86 mS
1	1	2^{26}	2^{26} + 512	67108864	6710.89 mS

Table 15-1: Time-out values for the Watchdog Timer

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state. The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The **WDRUN, WD1, WD0, EWRST, WDIF and WDCLR** bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG register. This bit is used to configure the clock source of watchdog timer from either the internal RC or the uC clock.

When WDTCK bit is cleared and 500KHz clock is used to run the watchdog timer, there is a chance that the watchdog timer would hang as the counter does not increment. This problem arises when the watchdog is set to run, (WDCON.7, WDRUN), the WDCLR bit (WDCON.0) is set to clear the watchdog timer and the next instruction is to set the PCON register for CPU to go into idle or power-down state. The reason this happens because the setting/clearing of WDCLR bit and the watchdog counter are running on different clock domains, CPU clock and internal RC clock respectively. When

16 SERIAL PORT (UART)

The UART in this device is a full duplex port. It provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W79E4051/2051.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

18.1 Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs maybe cause the comparator output toggle excessively, especially applying slow moving analog inputs. Table 18-2: Comparator Interrupt Mode shows the 8 comparator interrupt modes set by CM[2:0] in ACSR(97H). A built-in configurable debouncing timer provides 8 debouncing timing controlled by CPCK[2:0] for widely applications. The debouncing timing is shown in Table 18-1. If CPU is in normal/Idle mode F_{DB} is from Fosc; if CPU is in power-down mode F_{DB} is from internal RC 22M/11M Hz oscillator.

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$
1	1	1	$(3/F_{DB})*256$~$(4/F_{DB})*256$

Table 18-1: Comparator Debouncing Time

CM2	CM1	CM0	Comparator interrupt mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

Table 18-2: Comparator Interrupt Mode

Three debouncing modes are provided to filter out this noise. In debouncing mode when the comparator output matches one of three debouncing mode condition, the debouncing timer resets and starts up-counting. The end of debouncing triggers the hardware to check if the comparator output matches the mode condition or not. If it is compliant with the mode condition the comparator flag CF is set by hardware, otherwise CF keeps low. Refer to Figure 18-2.

22 POWER MONITORING FUNCTION

In order to prevent incorrect operation during power up and power drop, the W79E4051/2051 is provided a power monitor function, Brownout Detect.

22.1 Brownout Detect and Reset

The W79E4051/2051 has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 4 nominal levels are 2.4V, 2.7V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatedly senses the voltage for 64/f_{BRC} then turn off detector for 960/ f_{BRC} if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator, is approximately 100K* V_{DD} HZ ±50%. The relative control bits are located in SFR AUXR1 @A2h. The Brownout Detect block is shown in Figure 22-1.

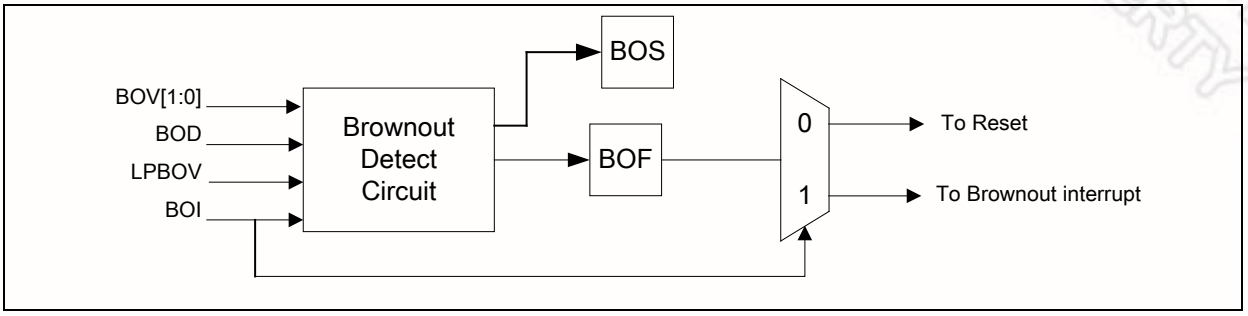


Figure 22-1: Brown-out Detect Block

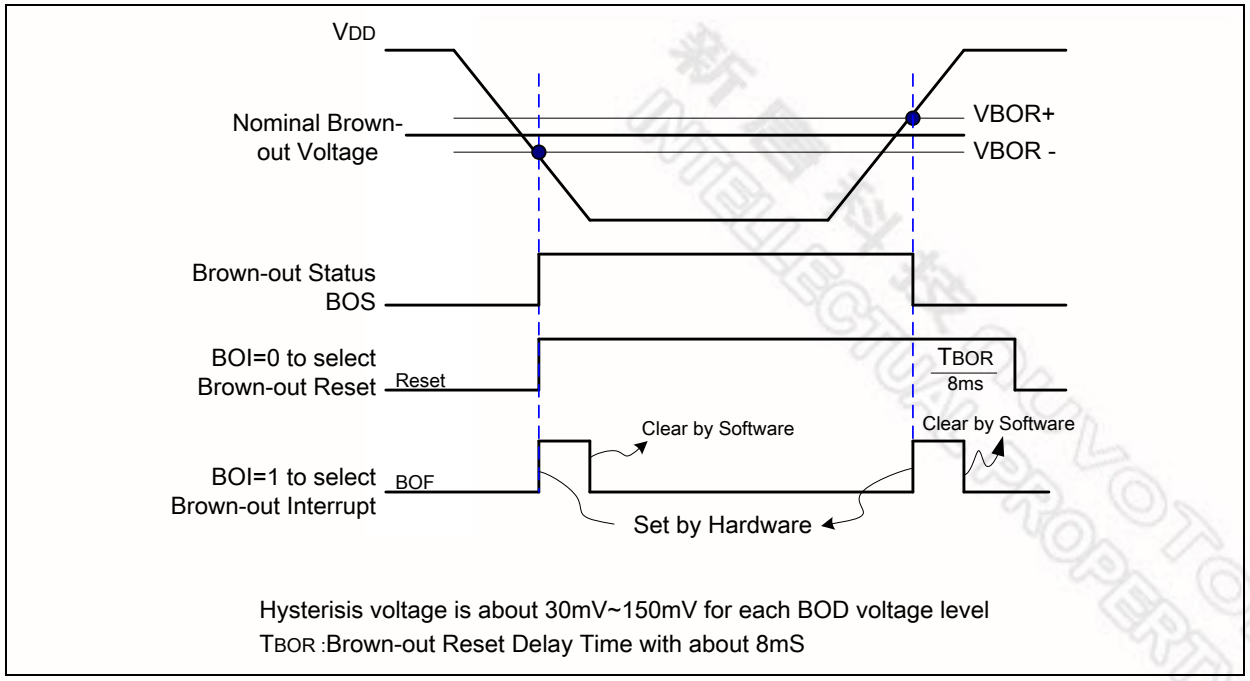


Figure 22-2: Brown-out Voltage Detection

Hysterisis range of brownout detect voltage is about 30mV to 150mV

24 CONFIG BITS

The W79E4051/2051 has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set by the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below.

24.1 CONFIG0

Config0

WDTCK	CBOV1	CBOV0	0	-	BPFR	Fosc1	Fosc0

Figure 24-1: Config0 register bits

Bit	Name	Function
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 500KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6~5	CBOV1 CBOV0	Brownout voltage selection bits: SFR bits (BOV1,BOV0) are initialized at reset with the inversed value of config0-bits (CBOV1,CBOV0)
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.
1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

CBOV.1	**CBOV.0**	**Brownout Voltage**
1	1	Brownout voltage is 2.4V
1	0	Brownout voltage is 2.7V
0	1	Brownout voltage is 3.8V
0	0	Brownout voltage is 4.5V

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 24MHz crystal
0	1	Internal RC Oscillator (FS1 bit in CONFIG1.5 will determine either 11MHz or 22MHZ) XT1 and XT2 function as P2.1 and P2.0
1	0	Reserved
1	1	External Oscillator in XTAL1; XT2 is in Tri-state

25 ELECTRICAL CHARACTERISTICS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
DC Power Supply	V_{DD}	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	TA		-40	+85	°C
Storage Temperature	Tst		-55	+150	°C
Sink current	ISK		-	95	mA
RAM Keep Alive Voltage	V_{RAM}		1.4	+7.0	V
Maximum Current into V_{DD}		-		120	mA
Maximum Current out of V_{SS}				120	mA
Maximum Current suck by a I/O pin				25	mA
Maximum Current sourced by a I/O pin				25	mA
Maximum Current suck by total I/O pins				80	mA
Maximum Current sourced by total I/O pins				80	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability

Sink Current P1, P2, P3 (Quasi-bidirectional Mode)	I_{SK1}	13	20	24	mA	V_{DD} = 4.5V, V_S = 0.45V
		8	13	17	mA	V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV[1:0]=00	$V_{BO2.4}$	2.25	2.4	2.55	V	
Brownout voltage with BOV[1:0]=01	$V_{BO2.7}$	2.55	2.7	2.75	V	
Brownout voltage with BOV[1:0]=10	$V_{BO3.8}$	3.65	3.8	3.90	V	
Brownout voltage with BOV[1:0]=11	$V_{BO4.5}$	4.30	4.5	4.65	V	
Brownout detection current	I_{BO1}		160/135	210/170	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=0)
	I_{BO2}		24/11	32/15	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=1, 1/16 mode)
Hysterisis range of BOD voltage	V_{Bh}	35	-	150	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI) = (0,x) or (1,0)
		10	-	60	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI)=(1,1)
Power On Reset Voltage	V_{POR}	1.45	2.0	2.10	V	With Hysterisis ~= 450mV

Notes: *1. RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P1, P2 and P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

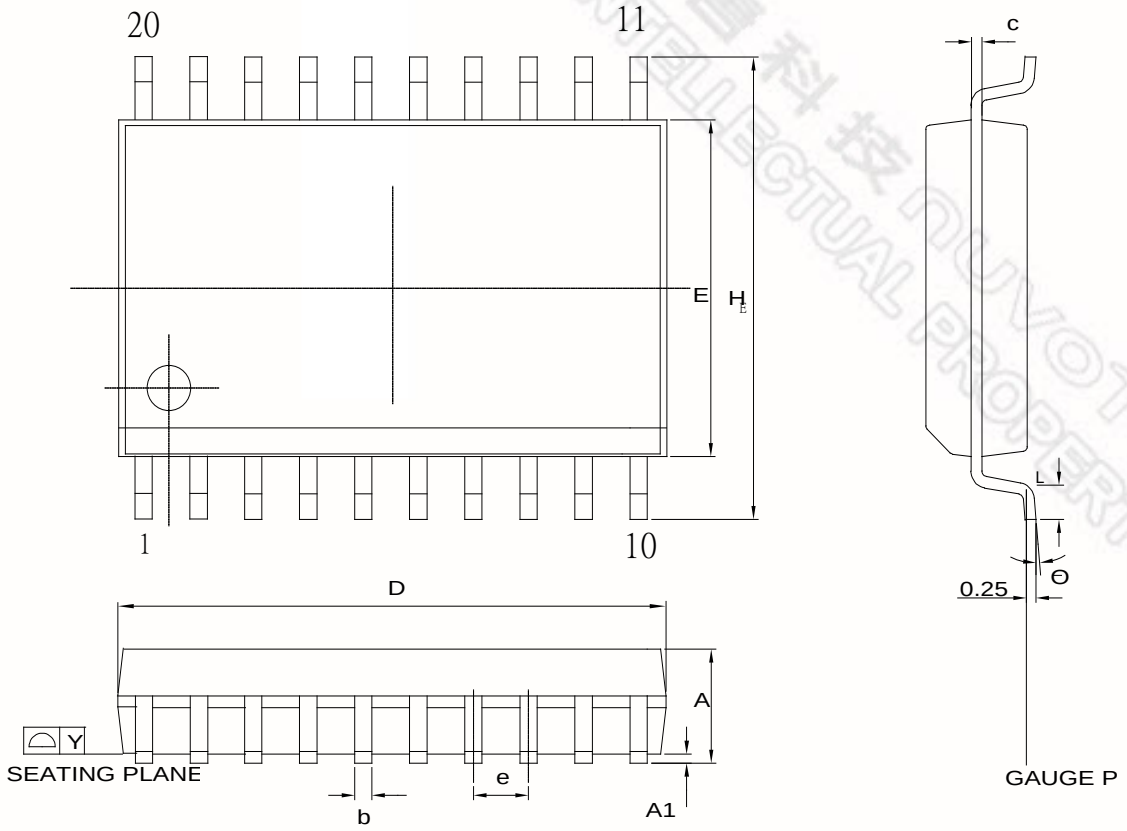
25.3 The COMPARATOR ELECTRICAL CHARACTERISTICS

(VDD–VSS = 3.0~5V±10%, TA = -40~85°C, Fosc = 24MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	50	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}
Comparator offset voltage	V_{OFF}			20	mV	With decoupled capacitors on inputs

27 PACKAGE DIMENSIONS

27.1 20-pin SOP

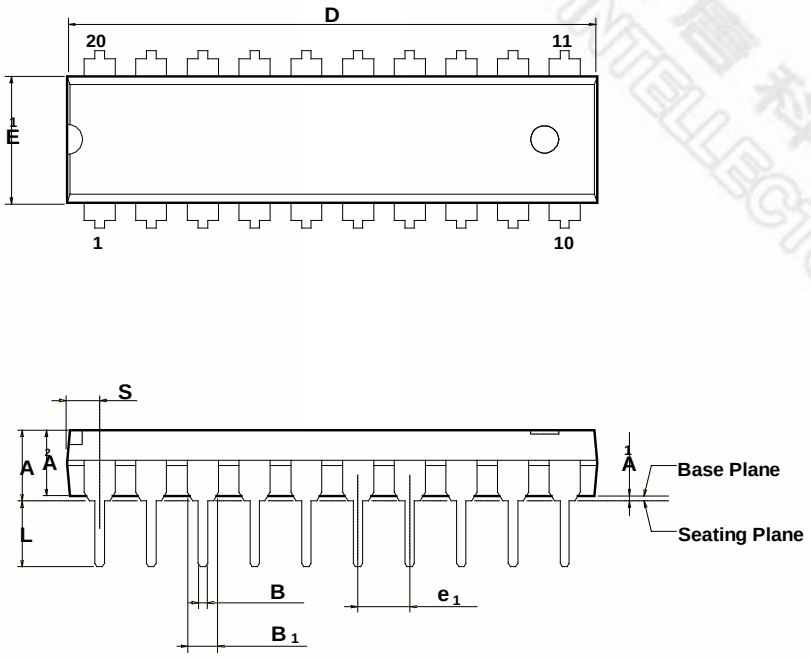


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Figure 27-1: 20L SOP-300mil

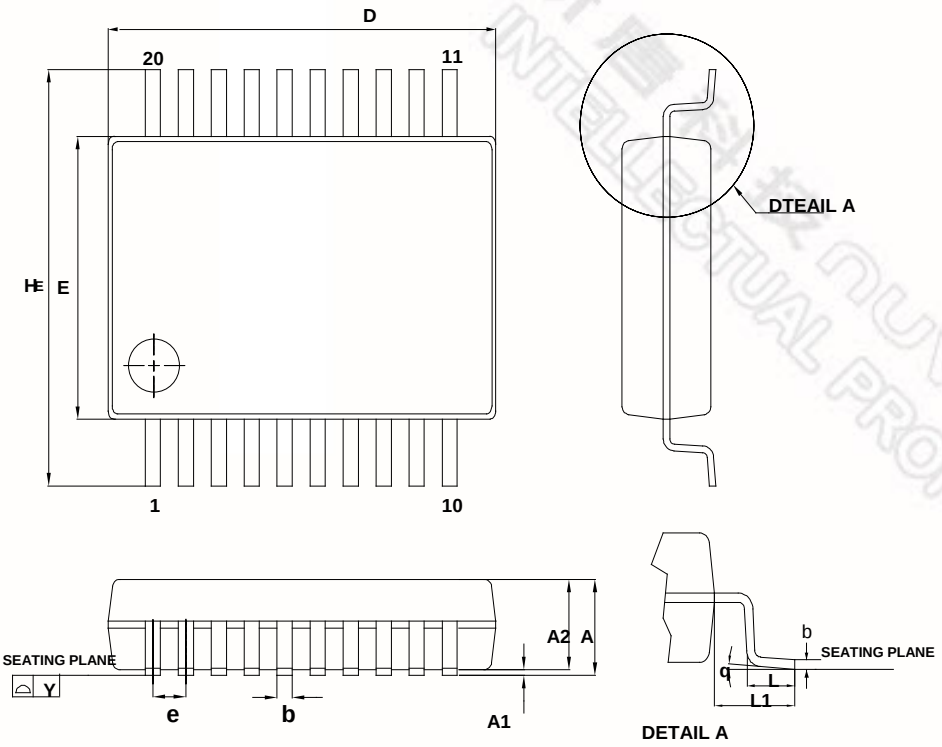
27.2 20-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

Figure 27-2: 20L DIP-300mil

27.3 20-pin SSOP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
HE	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
q	0	—	8	0	—	8

Figure 27-3: 20-Pin SSOP