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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dn512zvmc10

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μΑ

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	Ο°
V _{DD}	3.3 V supply voltage	3.3	V

General

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
I _{IND}	Input leakage current, digital pins					4, 5
	• V _{DD} < V _{IN} < 5.5 V	—	1	50	μA	
Z _{IND}	Input impedance examples, digital pins					4, 7
	• V _{DD} = 3.6 V	—	—	48	kΩ	
	• V _{DD} = 3.0 V	—	—	55	kΩ	
	• V _{DD} = 2.5 V	—	—	57	kΩ	
	• V _{DD} = 1.7 V	_	_	85	kΩ	
R _{PU}	Internal pullup resistors	20	35	50	kΩ	8
R _{PD}	Internal pulldown resistors	20	35	50	kΩ	9

Table 4. Voltage and current operating behaviors (continued)

- 1. Typical values characterized at 25° C and VDD = 3.6 V unless otherwise noted.
- 2. Open drain outputs must be pulled to V_{DD} .
- 3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
- 4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
- 5. Internal pull-up/pull-down resistors disabled.
- 6. Characterized, not tested in production.
- 7. Examples calculated using V_{IL} relation, V_{DD} , and max I_{IND} : $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
- 8. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
- 9. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}



5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.			μs	1
	• V_{DD} slew rate ≥ 5.7 kV/s		300		
	 V_{DD} slew rate < 5.7 kV/s 	_	1.7 V / (V _{DD} slew rate)		
	• VLLS1 → RUN	_	134	μs	
	• VLLS2 → RUN	_	96	μs	
	• VLLS3 → RUN	_	96	μs	
	• LLS → RUN	_	6.2	μs	
	VLPS → RUN	_	5.9	μs	
	• STOP → RUN	—	5.9	μs	

Table 5. Power mode transition operating behaviors

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	45	70	mA	
	• @ 3.0V	—	47	72	mA	
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	_	61	85	mA	
	• @ 3.0V		_			
	• @ 25°C	_	63	71	mA	
	• @ 125°C	_	72	87	mA	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	35	_	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	15	_	mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled		N/A		mA	6

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	_	ns
J7	TCLK low to boundary scan output data valid	_	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	_	22.1	ns
J13	TRST assert time	100	_	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals (continued)



Figure 5. Test clock input timing



Figure 6. Boundary scan (JTAG) timing

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)		V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

 Table 16.
 Oscillator DC electrical specifications (continued)

- 1. V_{DD} =3.3 V, Temperature =25 °C
- 2. See crystal or resonator manufacturer's recommendation
- 3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
- 4. When low power mode is selected, R_F is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	_	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—		50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	_	250	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	•
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

- 1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- 2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- 3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	—	3.6	V
R _F	Internal feedback resistor		100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32		5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation	_	0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t _{start}	Crystal start-up time	_	1000	_	ms	1
f _{ec_extal32}	Externally provided input clock frequency	_	32.768	—	kHz	2
V _{ec_extal32}	Externally provided input clock amplitude	700	_	V _{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.

The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

6.4 Memories and memory interfaces

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

 $Writes_subsystem = \frac{EEPROM - 2 \times EEESPLIT \times EEESIZE}{EEESPLIT \times EEESIZE} \times Write_efficiency \times n_{nvmcycd}$

where

- Writes_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} data flash cycling endurance (the following graph assumes 10,000 cycles)

Peripheral operating requirements and behaviors



Figure 9. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5		ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	_	12	ns

2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 26. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	_	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	_	ns	
FB2	Address, data, and control output valid	_	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and FB_TA input setup	13.7	_	ns	2
FB5	Data and FB_TA input hold	0.5	_	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWEn, FB_CSn, FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB}_{-}\text{TA}}.$

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
EIL	Input leakage error			I _{In} × R _{AS}		mV	I _{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.







Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	≤ 13 bit modes	18.484	—	450	Ksps	7
	rate	No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					
		16 bit modes	37.037	_	250	Ksps	8
		No ADC hardware averaging					
	Ce	Continuous conversions enabled					
		Peripheral clock = 50 MHz					

Table 29. 16-bit ADC with PGA operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. ADC must be configured to use the internal voltage reference (VREF_OUT)
- 3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
- 4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
- 5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
- 7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
- 8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	_	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{\rm PGAD}} \left(\frac{(V_{\rm REFPGA} \times 0.583) - V_{\rm CM}}{({\rm Gain}+1)} \right)$			A	3
		Gain =1, V_{REFPGA} =1.2V, V_{CM} =0.5V	_	1.54	_	μA	
		Gain =64, V_{REFPGA} =1.2V, V_{CM} =0.1V		0.57		μA	

Table continues on the next page ...

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
ENOB	Effective number	Gain=1, Average=4	11.6	13.4	_	bits	16-bit
	of bits	Gain=64, Average=4	7.2	9.6	—	bits	differential
		 Gain=1, Average=32 	12.8	14.5	—	bits	
		 Gain=2, Average=32 	11.0	14.3	—	bits	
		Gain=4, Average=32	7.9	13.8	—	bits	
		Gain=8, Average=32	7.3	13.1	—	bits	
		Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
		• Gain=64, Average=32	7.5	10.6	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	6.02	× ENOB +	1.76	dB	

Table 30. 16-bit ADC with PGA characteristics (continued)

1. Typical values assume V_{DDA} =3.0V, Temp=25°C, f_{ADCK}=6MHz unless otherwise stated.

- 2. This current is a PGA module adder, in addition to ADC conversion currents.
- Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
- 4. Gain = 2^{PGAG}
- 5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
- 6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	—	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	_	—	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	_	_	20	μA
V _{AIN}	Analog input voltage	V _{SS} – 0.3	—	V _{DD}	V
V _{AIO}	Analog input offset voltage		_	20	mV
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	 CR0[HYSTCTR] = 01 	_	10	_	mV
	• CR0[HYSTCTR] = 10	_	20	—	mV
	 CR0[HYSTCTR] = 11 	_	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5	_	—	V
V _{CMPOI}	Output low	_	—	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns

Table continues on the next page...

Symbol	Description	Min.	Тур.	Max.	Unit
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)		7	_	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	_	0.3	LSB

 Table 31. Comparator and 6-bit DAC electrical specifications (continued)

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6 V.

- 2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
- 3. 1 LSB = $V_{reference}/64$



Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)



Peripheral operating requirements and behaviors

Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements Table 32. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
T _A	Temperature	Operating t range of t	emperature he device	°C	
CL	Output load capacitance	_	100	pF	2
١L	Output load current		1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2 12-bit DAC operating behaviors Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	—	—	150	μΑ	
I _{DDA_DACH} P	Supply current — high-speed mode	—	—	700	μΑ	
tDACLP	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode		15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	_	_	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	—	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	—	—	±1	LSB	4
V _{OFFSET}	Offset error	_	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 \text{ V}$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	_	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421	_	%FSR/C	
Rop	Output resistance load = $3 \text{ k}\Omega$	—	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	Low power (SP _{LP})	0.05	0.12	—		
СТ	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	 High power (SP_{HP}) 	550	_	—		
	 Low power (SP_{LP}) 	40	_	—		

1. Settling within ±1 LSB

- 2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
- 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} 100 mV
- V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device





Figure 18. Typical INL error vs. digital code

6.8.10 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t _{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t _{SYS}	_	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	_	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	_	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	_	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	_	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

 Table 46.
 I²S master mode timing (limited voltage range)



Figure 26. I²S timing — master mode

Pinout

121 Map Bga	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E3	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
E2	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
F4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD				
E7	VDD	VDD	VDD								
F7	VSS	VSS	VSS								
H7	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
G4	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
F3	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		I2S0_CLKIN		
E6	VDD	VDD	VDD								
G7	VSS	VSS	VSS								
L6	VSS	VSS	VSS								
F1	USB0_DP	USB0_DP	USB0_DP								
F2	USB0_DM	USB0_DM	USB0_DM								
G1	VOUT33	VOUT33	VOUT33								
G2	VREGIN	VREGIN	VREGIN								
H1	ADC0_DP1	ADC0_DP1	ADC0_DP1								
H2	ADC0_DM1	ADC0_DM1	ADC0_DM1								
J1	ADC1_DP1	ADC1_DP1	ADC1_DP1								
J2	ADC1_DM1	ADC1_DM1	ADC1_DM1								
K1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
K2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
L1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	VDDA	VDDA	VDDA								
G5	VREFH	VREFH	VREFH								
G6	VREFL	VREFL	VREFL								
F6	VSSA	VSSA	VSSA								
J3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
H3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								

Rev. No.	Date	Substantial Changes
6	01/2012	 Added AC electrical specifications. Replaced TBDs with silicon data throughout. In "Power mode transition operating behaviors" table, removed entry times. Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. Updated I_{DD_RUN} numbers in 'Power consumption operating behaviors' section. Clarified 'Diagram: Typical IDD_RUN operating behavior' section and updated 'Run mode supply current vs. core frequency — all peripheral clocks disabled' figure. In 'Voltage reference electrical specifications' section, updated V_{DP_SRC}, I_{DDstby}, and 'V_{Reg33out} values.
7	02/2013	 In "ESD handling ratings", added a note for I_{LAT}. Updated "Voltage and current operating requirements". Updated "Voltage and current operating behaviors". Updated "Power mode transition operating behaviors". Updated "EMC radiated emissions operating behaviors" to add MAPBGA data. In "MCG specifications", updated the description of f_{ints_t}. In "16-bit ADC operating conditions", updated the max spec of V_{ADIN}. In "16-bit ADC electrical characteristics", updated the temp sensor slope and voltage specs. Updated "I2C switching specifications". In "SDHC specifications", removed the operating voltage limits and updated the SD1 and SD6 specs. In "I2S switching specifications", added separate specification tables for the full operating voltage range.

Table 51. Revision History (continued)