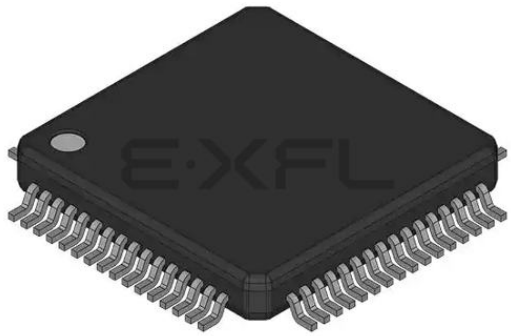

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	40MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	27
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8123vfbe

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Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
V_{REFP}	37	Input/ Output	Analog Input/ Output	**V_{REFP}, V_{REFMID} & V_{REFN}** — Internal pins for voltage reference which are brought off-chip so that they can be bypassed. Connect to a 0.1μF ceramic low ESR capacitor
V_{REFMID}	36			
V_{REFN}	35			
V_{REFLO}	38	Schmitt Input	Analog Input	**V_{REFLO}** — Analog Reference Voltage Low. This should normally be connected to a low-noise V_{SS}.
TEMP_SENSE	34	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and used to monitor the temperature of the die. Must be bypassed with a 0.01μF capacitor
CAN_RX **(GPIOC2)**	61	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is CAN_RX. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
CAN_TX **(GPIOC3)**	62	Open Drain Output Schmitt Input/ Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-up enable at reset.* * **Note**: If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is CAN_TX. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design.

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-1**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

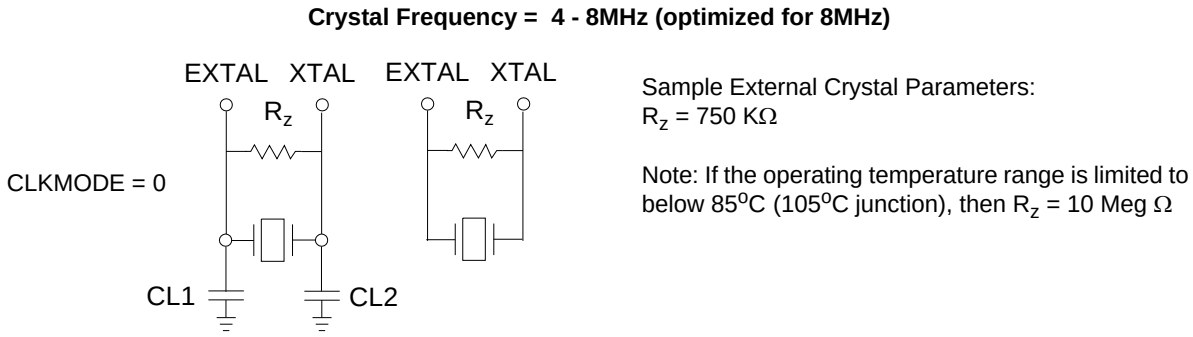

Figure 3-1 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit should be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-2**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

3.5 Registers

When referring to the register definitions for the OCCS in the **56F8300 Peripheral User Manual**, use the register definitions **with** the internal Relaxation Oscillator, since the 56F8323 and 56F8123 contain this oscillator.

Part 4 Memory Map

4.1 Introduction

The 56F8323 and 56F8123 devices are 16-bit motor-control chips based on the 56800E core. These parts use a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM and Flash memories are used in both spaces.

This section provides memory maps for:

- Program Address Space, including the Interrupt Vector Table
- Data Address Space, including the EOnCE Memory and Peripheral Memory Maps

On-chip memory sizes for the device are summarized in **Table 4-1.** Flash memories' restrictions are identified in the "Use Restrictions" column of **Table 4-1.**

Note: *Data Flash and Program RAM are NOT available on the 56F8123 device.*

Table 4-1 Chip Memory Configurations

On-Chip Memory	56F8323	56F8123	Use Restrictions
Program Flash	32KB	32KB	Erase / Program via Flash interface unit and word writes to CDBW
Data Flash	8KB	—	Erase / Program via Flash interface unit and word writes to CDBW. Data Flash can be read via either CDBR or XDB2, but not by both simultaneously
Program RAM	4KB	—	None
Data RAM	8KB	8KB	None
Program Boot Flash	8KB	8KB	Erase / Program via Flash Interface unit and word writes to CDBW

4.2 Program Map

The Program Memory map is located in **Table 4-2**. The operating mode control bits (MA and MB) in the Operating Mode Register (OMR) control the Program Memory map. Because the 56F8323 and 56F8123 do not include EMI, the OMR MA bit, which is used to decide internal or external BOOT, will have no effect on the Program Memory Map. OMR MB reflects the security status of the Program Flash. After reset, changing the OMR MB bit will have no effect on the Program Flash.

Table 4-3 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
SCI1	45	0-2	P:$5A	SCI 1 Receiver Error
SCI1	46	0-2	P:$5C	SCI 1 Receiver Full
				Reserved
DEC0	49	0-2	P:$62	*Quadrature Decoder #0 Home Switch or Watchdog*
DEC0	50	0-2	P:$64	*Quadrature Decoder #0 INDEX Pulse*
				Reserved
TMRC	56	0-2	P:$70	Timer C Channel 0
TMRC	57	0-2	P:$72	Timer C Channel 1
TMRC	58	0-2	P:$74	Timer C Channel 2
TMRC	59	0-2	P:$76	Timer C Channel 3
				Reserved
TMRA	64	0-2	P:$80	Timer A Channel 0
TMRA	65	0-2	P:$82	Timer A Channel 1
TMRA	66	0-2	P:$84	Timer A Channel 2
TMRA	67	0-2	P:$86	Timer A Channel 3
SCI0	68	0-2	P:$88	SCI 0 Transmitter Empty
SCI0	69	0-2	P:$8A	SCI 0 Transmitter Idle
				Reserved
SCI0	71	0-2	P:$8E	SCI 0 Receiver Error
SCI0	72	0-2	P:$90	SCI 0 Receiver Full
				Reserved
ADCA	74	0-2	P:$94	ADC A Conversion Complete / End of Scan
				Reserved
ADCA	76	0-2	P:$98	ADC A Zero Crossing or Limit Error
				Reserved
PWMA	78	0-2	P:$9C	*Reload PWM A*
				Reserved
PWMA	80	0-2	P:$A0	*PWM A Fault*
core	81	- 1	P:$A2	SW Interrupt LP
	82	0 - 2	P:$A4	

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to $0200, the first two locations of the vector table will overlay the chip reset addresses.

Table 4-8 Quad Timer A Registers Address Map (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA0_CMP1	$0	Compare Register 1
TMRA0_CMP2	$1	Compare Register 2
TMRA0_CAP	$2	Capture Register
TMRA0_LOAD	$3	Load Register
TMRA0_HOLD	$4	Hold Register
TMRA0_CNTR	$5	Counter Register
TMRA0_CTRL	$6	Control Register
TMRA0_SCR	$7	Status and Control Register
TMRA0_CMPLD1	$8	Comparator Load Register 1
TMRA0_CMPLD2	$9	Comparator Load Register 2
TMRA0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRA1_CMP1	$10	Compare Register 1
TMRA1_CMP2	$11	Compare Register 2
TMRA1_CAP	$12	Capture Register
TMRA1_LOAD	$13	Load Register
TMRA1_HOLD	$14	Hold Register
TMRA1_CNTR	$15	Counter Register
TMRA1_CTRL	$16	Control Register
TMRA1_SCR	$17	Status and Control Register
TMRA1_CMPLD1	$18	Comparator Load Register 1
TMRA1_CMPLD2	$19	Comparator Load Register 2
TMRA1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRA2_CMP1	$20	Compare Register 1
TMRA2_CMP2	$21	Compare Register 2
TMRA2_CAP	$22	Capture Register
TMRA2_LOAD	$23	Load Register
TMRA2_HOLD	$24	Hold Register
TMRA2_CNTR	$25	Counter Register
TMRA2_CTRL	$26	Control Register
TMRA2_SCR	$27	Status and Control Register
TMRA2_CMPLD1	$28	Comparator Load Register 1

Table 4-23 GPIOC Registers Address Map (GPIOC_BASE = $00 F310)

Register Acronym	Address Offset	Register Description	Reset Value
GPIOC_PUR	$0	Pull-up Enable Register	0 x 007C
GPIOC_DR	$1	Data Register	0 x 0000
GPIOC_DDR	$2	Data Direction Register	0 x 0000
GPIOC_PER	$3	Peripheral Enable Register	0 x 007F
GPIOC_IAR	$4	Interrupt Assert Register	0 x 0000
GPIOC_IENR	$5	Interrupt Enable Register	0 x 0000
GPIOC_IPOLR	$6	Interrupt Polarity Register	0 x 0000
GPIOC_IPR	$7	Interrupt Pending Register	0 x 0000
GPIOC_IESR	$8	Interrupt Edge-Sensitive Register	0 x 0000
GPIOC_PPMODE	$9	Push-Pull Mode Register	0 x 007F
GPIOC_RAWDATA	$A	Raw Data Input Register	—

Table 4-24 System Integration Module Registers Address Map (SIM_BASE = $00 F350)

Register Acronym	Address Offset	Register Description
SIM_CONTROL	$0	Control Register
SIM_RSTSTS	$1	Reset Status Register
SIM_SCR0	$2	Software Control Register 0
SIM_SCR1	$3	Software Control Register 1
SIM_SCR2	$4	Software Control Register 2
SIM_SCR3	$5	Software Control Register 3
SIM_MSH_ID	$6	Most Significant Half JTAG ID
SIM_LSH_ID	$7	Least Significant Half JTAG ID
SIM_PUDR	$8	Pull-up Disable Register
		Reserved
SIM_CLKOSR	$A	Clock Out Select Register
SIM_GPS	$B	GPIO Peripheral Select Register
SIM_PCE	$C	Peripheral Clock Enable Register
SIM_ISALH	$D	I/O Short Address Location High Register
SIM_ISALL	$E	I/O Short Address Location Low Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8123 device

Register Acronym	Address Offset	Register Description
FCMB1_DATA	$4B	Message Buffer 1 Data Register
FCMB1_DATA	$4C	Message Buffer 1 Data Register
FCMB1_DATA	$4D	Message Buffer 1 Data Register
FCMB1_DATA	$4E	Message Buffer 1 Data Register
		Reserved
FCMB2_CONTROL	$50	Message Buffer 2 Control / Status Register
FCMB2_ID_HIGH	$51	Message Buffer 2 ID High Register
FCMB2_ID_LOW	$52	Message Buffer 2 ID Low Register
FCMB2_DATA	$53	Message Buffer 2 Data Register
FCMB2_DATA	$54	Message Buffer 2 Data Register
FCMB2_DATA	$55	Message Buffer 2 Data Register
FCMB2_DATA	$56	Message Buffer 2 Data Register
		Reserved
FCMB3_CONTROL	$58	Message Buffer 3 Control / Status Register
FCMB3_ID_HIGH	$59	Message Buffer 3 ID High Register
FCMB3_ID_LOW	$5A	Message Buffer 3 ID Low Register
FCMB3_DATA	$5B	Message Buffer 3 Data Register
FCMB3_DATA	$5C	Message Buffer 3 Data Register
FCMB3_DATA	$5D	Message Buffer 3 Data Register
FCMB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FCMB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FCMB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FCMB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FCMB4_DATA	$63	Message Buffer 4 Data Register
FCMB4_DATA	$64	Message Buffer 4 Data Register
FCMB4_DATA	$65	Message Buffer 4 Data Register
FCMB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FCMB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FCMB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FCMB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FCMB5_DATA	$6B	Message Buffer 5 Data Register

5.6.6.3 SCI1 Receiver Error Interrupt Priority Level (SCI1_RERR IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.4 Reserved—Bits 7–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.5 SCI1 Transmitter Idle Interrupt Priority Level (SCI1_TIDL IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.6 SCI1 Transmitter Empty Interrupt Priority Level (SCI1_XMIT IPL)— Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6.7 SPI0 Transmitter Empty Interrupt Priority Level (SPI0_XMIT IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Interrupt Priority Register 7 (IPR7)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	TMRA0 IPL		0	0	0	0	0	0	0	0	TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Interrupt Priority Register (IPR7)

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.2 Reserved—Bits 13–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.8.3 Timer C, Channel 3 Interrupt Priority Level (TMRC3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.4 Timer C, Channel 2 Interrupt Priority Level (TMRC2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.21.1 IRQ Pending (PENDING)—Bits 64–49

This register combines with the other five to represent the pending IRQs for interrupt vector numbers two through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.23 IRQ Pending 5 Register (IRQP5)

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PEND-ING [81]
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-25 IRQ Pending Register 5 (IRQP5)

5.6.23.1 Reserved—Bits 96–82

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

5.6.23.2 IRQ Pending (PENDING)—Bit 81

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

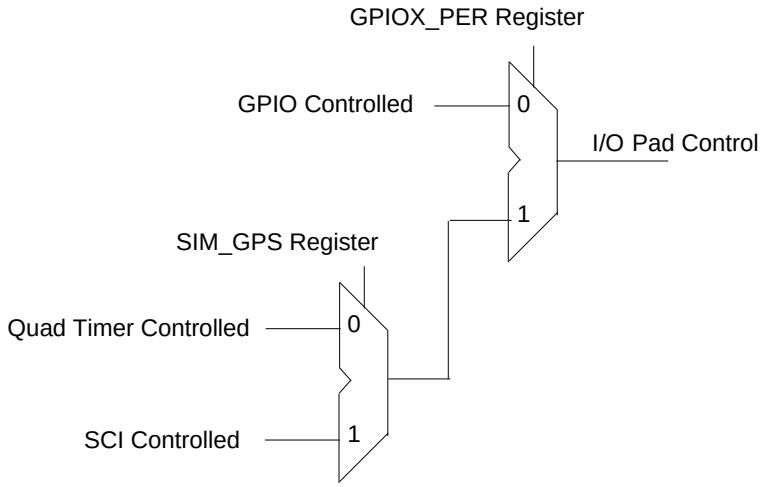

Figure 6-10 Overall Control of Pads Using SIM_GPS Control

Base + $B	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	C6	C5	B1	B0	A5	A4	A3	A2
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 GPIO Peripheral Select Register (SIM_GPS)

6.5.8.1 Reserved—Bits 15–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.8.2 GPIOC6 (C6)—Bit 7

This bit selects the alternate function for GPIOC6.

- 0 = TC0 (default)
- 1 = TXD0

6.5.8.3 GPIOC5 (C5)—Bit 6

This bit selects the alternate function for GPIOC5.

- 0 = TC1 (default)
- 1 = RXD0

6.5.8.4 GPIOB1 (B1)—Bit 5

This bit selects the alternate function for GPIOB1.

- 0 = MISO0 (default)
- 1 = RXD1

6.5.10.2 Input/Output Short Address Low (ISAL[21:6])—Bit 15–0

This field represents the lower 16 address bits of the “hard coded” I/O short address.

6.6 Clock Generation Overview

The SIM uses an internal master clock from the OCCS (CLKGEN) module to produce the peripheral and system (core and memory) clocks. The maximum master clock frequency is 120MHz. Peripheral and system clocks are generated at half the master clock frequency and therefore at a maximum 60MHz. The SIM provides power modes (Stop, Wait) and clock enables (SIM_PCE register, CLK_DIS, ONCE_EBL) to control which clocks are in operation. The OCCS, power modes, and clock enables provide a flexible means to manage power consumption.

Power utilization can be minimized in several ways. In the OCCS, the relaxation oscillator, crystal oscillator, and PLL may be shut down when not in use. When the PLL is in use, its prescaler and postscaler can be used to limit PLL and master clock frequency. Power modes permit system and/or peripheral clocks to be disabled when unused. Clock enables provide the means to disable individual clocks. Some peripherals provide further controls to disable unused subfunctions. Refer to **Part 3 On-Chip Clock Synthesis (OCCS)**, and the **56F8300 Peripheral User Manual** for further details.

The memory, peripheral and core clocks all operate at the same frequency (60MHz max).

6.7 Power-Down Modes

The 56F8323/56F8123 operate in one of three power-down modes, as shown in **Table 6-2**.

Table 6-2 Clock Operation in Power-Down Modes

Mode	Core Clocks	Peripheral Clocks	Description
Run	Active	Active	Device is fully functional
Wait	Core and memory clocks disabled	Active	Peripherals are active and can produce interrupts if they have not been masked off. Interrupts will cause the core to come out of its suspended state and resume normal operation. Typically used for power-conscious applications.
Stop	System clocks continue to be generated in the SIM, but most are gated prior to reaching memory, core and peripherals.		The only possible recoveries from Stop mode are: 1. CAN traffic (1st message will be lost) 2. Non-clocked interrupts ($\overline{\text{IRQA}}$) 3. COP reset 4. External reset 5. Power-on reset

All peripherals, except the COP/watchdog timer, run off the IPBus clock frequency, which is the same as the main processor frequency in this architecture. The maximum frequency of operation is SYS_CLK = 60MHz.

Refer to the PCE register in **Part 6.5.9** and ADC power modes. Power is a function of the system frequency, which can be controlled through the OCCS.

Part 7 Security Features

The 56F8323/56F8123 offer security features intended to prevent unauthorized users from reading the contents of the Flash memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the EOnCE interface, preventing access to internal code. Normal program execurtion is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8323/56F8123 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

7.2.3 Flash Lockout Recovery

If a user inadvertently enables Flash security on the device, a built-in lockout recovery mechanism can be used to reenable access to the device. This mechanism completely reases all on-chip Flash, thus disabling Flash security. Access to this recovery mechanism is built into CodeWarrior via an instruction in memory configuration (*.cfg*) files. Add, or uncomment the following configuration command:

unlock_flash_on_connect 1

For more information, please see **CodeWarrior MC56F83xx/DSP5685x Family Targeting Manual**.

The LOCKOUT_RECOVERY instruction has an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

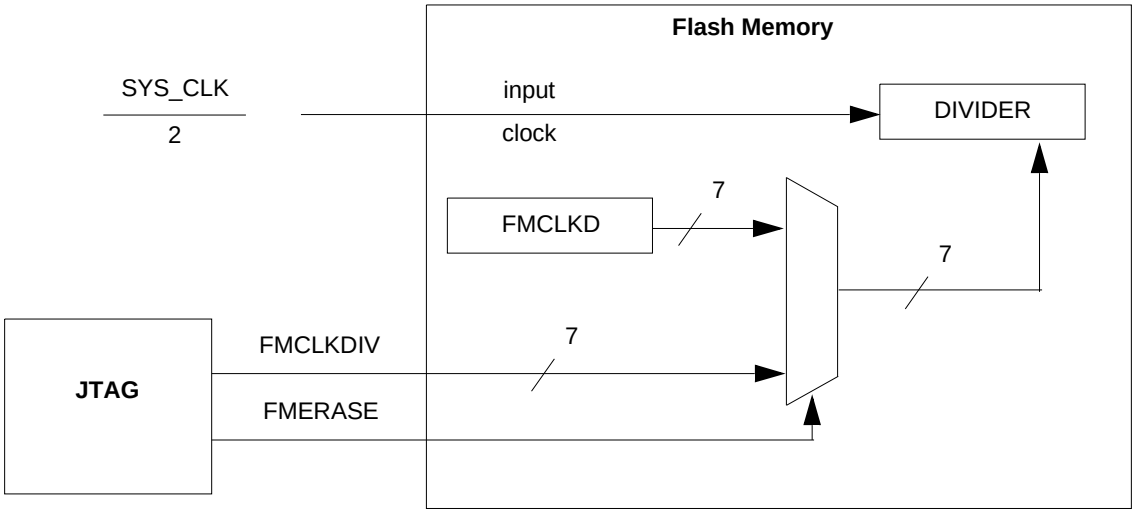

Figure 7-1 JTAG to FM Connection for Lockout Recovery

Two examples of FM_CLKDIV calculations follow.

Table 8-3 GPIO External Signals Map

GPIO Function	Peripheral Function	Package Pin	Notes
GPIOA0	*PWMA0*	3	*PWM is NOT available in 56F8123*
GPIOA1	*PWMA1*	4	*PWM is NOT available in 56F8123*
GPIOA2	*PWMA2* / $\overline{SSI}$	7	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA3	*PWMA3* / MISO1	8	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA4	*PWMA4* / MOSI1	9	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA5	*PWMA5* / SCLK1	10	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA6	*FAULTA0*	13	
GPIOA7	*FAULTA1*	14	
GPIOA8	*FAULTA2*	15	
GPIOA9	*ISA0*	16	
GPIOA10	*ISA0*	18	
GPIOA11	*ISA2*	19	
GPIOB0	$\overline{SS0}$ / TXD1	21	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB1	MISO0 / RXD1	22	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB2	MOSI0	24	
GPIOB3	SCLK0	25	
GPIOB4	*HOME0* / TA3	49	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*
GPIOB5	*INDEX0* / TA2	50	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*
GPIOB6	*PHASEB0* / TA1	51	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*

Table 10-15 Crystal Oscillator Parameters (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Resonator Min-Max Period Variation	T_{RP}	—	—	300	ps
Bias Current, high-drive mode	I_{BIASH}	—	250	290	μA
Bias Current, low-drive mode	I_{BIASL}	—	80	110	μA
Quiescent Current, power-down mode	I_{PD}	—	0	1	μA

Table 10-16 Relaxation Oscillator Parameters

Characteristic	Min	Typ	Max	Units
Center Frequency	—	8	—	MHz
Minimum Tuning Step Size (See Note)	—	82	—	ps
Maximum Tuning Step Size (See Note)	—	41	—	ns
Frequency Accuracy -50°C to +150°C (See **Figure 10-4**)	—	+/- 1.78	+2 /-3	%
Maximum Cycle-to-Cycle Jitter	—	—	500	ps
Stabilization Time from Power-up	—	—	4	μs

Note: An LSB change in the tuning code results in an 82ps shift in the frequency period, while an MSB change in the tuning code results in a 41ns shift in the frequency period.

10.15 Analog-to-Digital Converter (ADC) Parameters

Table 10-24 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	µA
Uncalibrated Gain Error (ideal = 1)	E_{GAIN}	—	+/- .004	+/- .01	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 26	+/- 32	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-21**	—	LSBs
Calibration Factor 1[7]	CF1	—	0.008597	—	—
Calibration Factor 2[7]	CF2	—	-2.8	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db

- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA} and V_{SSA} pins
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or EOnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- Because the Flash memory is programmed through the JTAG/EOnCE port, the designer should provide an interface to this port to allow in-circuit Flash programming

12.3 Power Distribution and I/O Ring Implementation

Figure 12-1 illustrates the general power control incorporated in the 56F8323/56F8123. This chip contains two internal power regulators. One of them is powered from the $V_{DDA\_OSC\_PLL}$ pin and cannot be turned off. This regulator controls power to the internal clock generation circuitry. The other regulator is powered from the V_{DD_IO} pins and provides power to all of the internal digital logic of the core, all peripherals and the internal memories. This regulator can be turned off, if an external V_{DD_CORE} voltage is externally applied to the V_{CAP} pins.

In summary, the entire chip can be supplied from a single 3.3 volt supply if the large core regulator is enabled. If the regulator is not enabled, a dual supply 3.3V/2.5V configuration can also be used.

Notes:

- Flash, RAM and internal logic are powered from the core regulator output
- $V_{PP}1$ and $V_{PP}2$ are not connected in the customer system
- All circuitry, analog *and* digital, shares a common V_{SS} bus

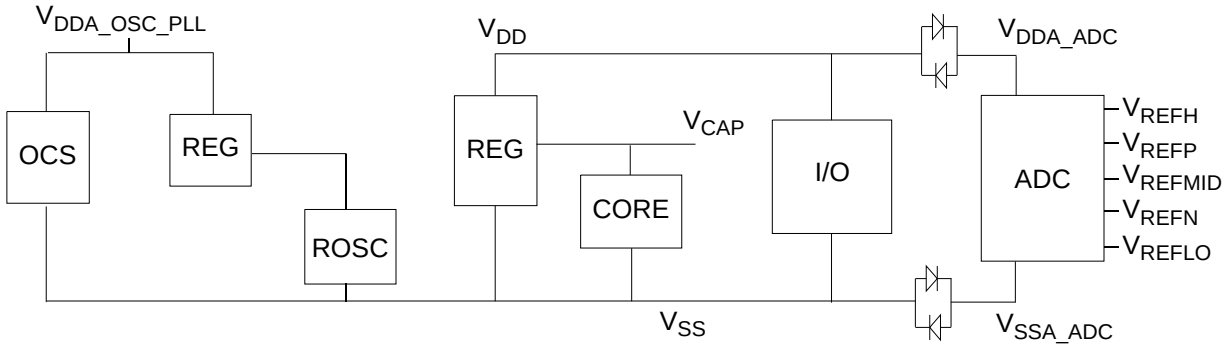

Figure 12-1 Power Management

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