Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	27
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8323mfbe

Document Revision History

Version History	Description of Change
Rev 14.0	Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz.
Rev 15.0	Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**.
Rev. 16	• Added the following note to the description of the TMS signal in **Table 2-2**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor. • Added the following note to the description of the $\overline{\text{TRST}}$ signal in **Table 2-2**: **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
Rev. 17	Changed the “Frequency Accuracy” specification in **Table 10-16** (was ±2.0%, is +2 / -3%).

Please see http://www.freescale.com for the most current data sheet revision.

synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1/2 (center-aligned mode only) to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters (ADCs) through Quad Timer C, Channel 2.

The 56F8323 incorporates one Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), two Quad Timers, and FlexCAN. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. A Flex Controller Area Network (FlexCAN) interface (CAN Version 2.0 B-compliant) and an internal interrupt controller are also a part of the 56F8323.

1.2.2 56F8123 Features

The 56F8123 controller includes 32KB of Program Flash, programmable through the JTAG port, and 8KB of Data RAM. A total of 8KB of Boot Flash is incorporated for easy customer inclusion of field-programmable software routines that can be used to program the main Program Flash memory area. The Program Flash memory can be independently bulk erased or erased in pages; Program Flash page erase size is 1KB. The Boot Flash memory can also be either bulk or page erased.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs), two Serial Peripheral Interfaces (SPIs), and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8123.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
ISA0 **(GPIOA9)**	16	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISA0** — This input current status pin is used for top/bottom pulse width correction in complementary channel operation for PWMA. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is ISA0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
ISA1 **(GPIOA10)**	18	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISA1** — This input current status pin is used for top/bottom pulse width correction in complementary channel operation for PWMA. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is ISA1. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
ISA2 **(GPIOA11)**	19	Schmitt Input Schmitt Input/ Output	Input, pull-up enabled	**ISA2** — This input current status pin is used for top/bottom pulse width correction in complementary channel operation for PWMA. **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. In the 56F8323, the default state after reset is ISA2. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
ANA0	26	Input	Analog Input	**ANA0 - 3** — Analog inputs to ADCA, Channel 0
ANA1	27			
ANA2	28			
ANA3	29			
ANA4	30	Input	Analog Input	**ANA4 - 7** — Analog inputs to ADCA, Channel 1
ANA5	31			
ANA6	32			
ANA7	33			
V_{REFH}	40	Schmitt Input	Analog Input	**V_{REFH}** — Analog Reference Voltage High

Table 4-3 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
core	4	3	P:$08	HW Stack Overflow
core	5	3	P:$0A	Misaligned Long Word Access
core	6	1-3	P:$0C	OnCE Step Counter
core	7	1-3	P:$0E	OnCE Breakpoint Unit 0
				Reserved
core	9	1-3	P:$12	OnCE Trace Buffer
core	10	1-3	P:$14	OnCE Transmit Register Empty
core	11	1-3	P:$16	OnCE Receive Register Full
				Reserved
core	14	2	P:$1C	SW Interrupt 2
core	15	1	P:$1E	SW Interrupt 1
core	16	0	P:$20	SW Interrupt 0
core	17	0-2	P:$22	IRQA
				Reserved
LVI	20	0-2	P:$28	Low-Voltage Detector (power sense)
PLL	21	0-2	P:$2A	PLL
FM	22	0-2	P:$2C	FM Access Error Interrupt
FM	23	0-2	P:$2E	FM Command Complete
FM	24	0-2	P:$30	FM Command, data and address Buffers Empty
				Reserved
FLEXCAN	26	0-2	P:$34	*FLEXCAN Bus Off*
FLEXCAN	27	0-2	P:$36	*FLEXCAN Error*
FLEXCAN	28	0-2	P:$38	*FLEXCAN Wake Up*
FLEXCAN	29	0-2	P:$3A	*FLEXCAN Message Buffer Interrupt*
				Reserved
GPIOC	33	0-2	P:$42	GPIO C
GPIOB	34	0-2	P:$44	GPIO B
GPIOA	35	0-2	P:$46	GPIO A
				Reserved
SPI1	38	0-2	P:$4C	SPI 1 Receiver Full
SPI1	39	0-2	P:$4E	SPI 1 Transmitter Empty
SPI0	40	0-2	P:$50	SPI 0 Receiver Full
SPI0	41	0-2	P:$52	SPI 0 Transmitter Empty
SCI1	42	0-2	P:$54	SCI 1 Transmitter Empty
SCI1	43	0-2	P:$56	SCI 1Transmitter Idle
				Reserved

Table 4-8 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRA3_CMP1	$30	Compare Register 1
TMRA3_CMP2	$31	Compare Register 2
TMRA3_CAP	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCR	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_COMSCR	$3A	Comparator Status and Control Register

Table 4-9 Quad Timer C Registers Address Map (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CMP1	$0	Compare Register 1
TMRC0_CMP2	$1	Compare Register 2
TMRC0_CAP	$2	Capture Register
TMRC0_LOAD	$3	Load Register
TMRC0_HOLD	$4	Hold Register
TMRC0_CNTR	$5	Counter Register
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register

Table 4-27 FlexCAN Registers Address Map (FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8123 device

Register Acronym	Address Offset	Register Description
FCMCR	$0	Module Configuration Register
		Reserved
FCCTL0	$3	Control Register 0 Register
FCCTL1	$4	Control Register 1 Register
FCTMR	$5	Free-Running Timer Register
FCMAXMB	$6	Maximum Message Buffer Configuration Register
		Reserved
FCRXGMASK_H	$8	Receive Global Mask High Register
FCRXGMASK_L	$9	Receive Global Mask Low Register
FCRX14MASK_H	$A	Receive Buffer 14 Mask High Register
FCRX14MASK_L	$B	Receive Buffer 14 Mask Low Register
FCRX15MASK_H	$C	Receive Buffer 15 Mask High Register
FCRX15MASK_L	$D	Receive Buffer 15 Mask Low Register
		Reserved
FCSTATUS	$10	Error and Status Register
FCIMASK1	$11	Interrupt Masks 1 Register
FCIFLAG1	$12	Interrupt Flags 1 Register
FCR/T_ERROR_CNTRS	$13	Receive and Transmit Error Counters Register
		Reserved
		Reserved
		Reserved
FCMB0_CONTROL	$40	Message Buffer 0 Control / Status Register
FCMB0_ID_HIGH	$41	Message Buffer 0 ID High Register
FCMB0_ID_LOW	$42	Message Buffer 0 ID Low Register
FCMB0_DATA	$43	Message Buffer 0 Data Register
FCMB0_DATA	$44	Message Buffer 0 Data Register
FCMB0_DATA	$45	Message Buffer 0 Data Register
FCMB0_DATA	$46	Message Buffer 0 Data Register
		Reserved
FCMSB1_CONTROL	$48	Message Buffer 1 Control / Status Register
FCMSB1_ID_HIGH	$49	Message Buffer 1 ID High Register
FCMSB1_ID_LOW	$4A	Message Buffer 1 ID Low Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8123 device

Register Acronym	Address Offset	Register Description
FCMB1_DATA	$4B	Message Buffer 1 Data Register
FCMB1_DATA	$4C	Message Buffer 1 Data Register
FCMB1_DATA	$4D	Message Buffer 1 Data Register
FCMB1_DATA	$4E	Message Buffer 1 Data Register
		Reserved
FCMB2_CONTROL	$50	Message Buffer 2 Control / Status Register
FCMB2_ID_HIGH	$51	Message Buffer 2 ID High Register
FCMB2_ID_LOW	$52	Message Buffer 2 ID Low Register
FCMB2_DATA	$53	Message Buffer 2 Data Register
FCMB2_DATA	$54	Message Buffer 2 Data Register
FCMB2_DATA	$55	Message Buffer 2 Data Register
FCMB2_DATA	$56	Message Buffer 2 Data Register
		Reserved
FCMB3_CONTROL	$58	Message Buffer 3 Control / Status Register
FCMB3_ID_HIGH	$59	Message Buffer 3 ID High Register
FCMB3_ID_LOW	$5A	Message Buffer 3 ID Low Register
FCMB3_DATA	$5B	Message Buffer 3 Data Register
FCMB3_DATA	$5C	Message Buffer 3 Data Register
FCMB3_DATA	$5D	Message Buffer 3 Data Register
FCMB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FCMB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FCMB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FCMB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FCMB4_DATA	$63	Message Buffer 4 Data Register
FCMB4_DATA	$64	Message Buffer 4 Data Register
FCMB4_DATA	$65	Message Buffer 4 Data Register
FCMB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FCMB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FCMB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FCMB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FCMB5_DATA	$6B	Message Buffer 5 Data Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8123 device

Register Acronym	Address Offset	Register Description
FCMB9_DATA	$8D	Message Buffer 9 Data Register
FCMB9_DATA	$8E	Message Buffer 9 Data Register
		Reserved
FCMB10_CONTROL	$90	Message Buffer 10 Control / Status Register
FCMB10_ID_HIGH	$91	Message Buffer 10 ID High Register
FCMB10_ID_LOW	$92	Message Buffer 10 ID Low Register
FCMB10_DATA	$93	Message Buffer 10 Data Register
FCMB10_DATA	$94	Message Buffer 10 Data Register
FCMB10_DATA	$95	Message Buffer 10 Data Register
FCMB10_DATA	$96	Message Buffer 10 Data Register
		Reserved
FCMB11_CONTROL	$98	Message Buffer 11 Control / Status Register
FCMB11_ID_HIGH	$99	Message Buffer 11 ID High Register
FCMB11_ID_LOW	$9A	Message Buffer 11 ID Low Register
FCMB11_DATA	$9B	Message Buffer 11 Data Register
FCMB11_DATA	$9C	Message Buffer 11 Data Register
FCMB11_DATA	$9D	Message Buffer 11 Data Register
FCMB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved
FCMB12_CONTROL	$A0	Message Buffer 12 Control / Status Register
FCMB12_ID_HIGH	$A1	Message Buffer 12 ID High Register
FCMB12_ID_LOW	$A2	Message Buffer 12 ID Low Register
FCMB12_DATA	$A3	Message Buffer 12 Data Register
FCMB12_DATA	$A4	Message Buffer 12 Data Register
FCMB12_DATA	$A5	Message Buffer 12 Data Register
FCMB12_DATA	$A6	Message Buffer 12 Data Register
		Reserved
FCMB13_CONTROL	$A8	Message Buffer 13 Control / Status Register
FCMB13_ID_HIGH	$A9	Message Buffer 13 ID High Register
FCMB13_ID_LOW	$AA	Message Buffer 13 ID Low Register
FCMB13_DATA	$AB	Message Buffer 13 Data Register
FCMB13_DATA	$AC	Message Buffer 13 Data Register
FCMB13_DATA	$AD	Message Buffer 13 Data Register

5.6.3.1 Flash Memory Command, Data, Address Buffers Empty Interrupt Priority Level (FMCBE IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 Flash Memory Command Complete Priority Level (FMCC IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.3 Flash Memory Error Interrupt Priority Level (FMERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 PLL Loss of Lock Interrupt Priority Level (LOCK IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.30.6 Reserved—Bit 3

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.30.7 $\overline{\text{IRQA}}$ State Pin ($\overline{\text{IRQA}}$ STATE)—Bit 2

This *read-only* bit reflects the state of the external $\overline{\text{IRQA}}$ pin.

5.6.30.8 Reserved—Bit 1

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.30.9 $\overline{\text{IRQA}}$ Edge Pin ($\overline{\text{IRQA}}$ Edg)—Bit 0

This bit controls whether the external $\overline{\text{IRQA}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQA}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQA}}$ interrupt is falling-edge sensitive

5.7 Resets

5.7.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address whenever $\overline{\text{RESET}}$ is asserted. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released.

5.7.2 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled except the core IRQs with fixed priorities

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0
- SW Interrupt LP

These interrupts are enabled at their fixed priority levels.

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.7
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.8
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.9
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

6.5.6.3 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ pin.

6.5.6.4 Reserved—Bits 9–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.5 JTAG—Bit 3

This bit controls the pull-up resistors on the $\overline{\text{TRST}}$, TMS, and TDI pins.

6.5.6.6 Reserved—Bits 2–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7 CLKO Select Register (SIM_CLKOSR)

The CLKO select register can be used to multiplex out any one of the clocks generated inside the clock generation and SIM modules. The default value is SYS_CLK. All other clocks primarily muxed out are for test purposes only, and are subject to significant unspecified latencies at high frequencies.

The upper four bits of the GPIOB register can function as GPIO, Quad Decoder #0 signals, or as additional clock output signals. GPIO has priority and is enabled/disabled via the GPIOB_PER. If GPIOB[7:4] are programmed to operate as peripheral outputs, then the choice between Quad Decoder #0 and additional clock outputs is made here in the CLKOSR. The default state is for the peripheral function of GPIOB[7:4] to be programmed as Quad Decoder #0. This can be changed by altering $\overline{\text{PHASE0}}$ through $\overline{\text{INDEX}}$ shown in **Figure 6-9**.

The CLKOUT pin is not bonded out in the device. Instead, it is offered only as a pad for die-level testing.

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	$\overline{\text{PHSA}}$	$\overline{\text{PHSB}}$	$\overline{\text{INDEX}}$	$\overline{\text{HOME}}$	CLK DIS	CLKOSEL				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 6-9 CLKO Select Register (SIM_CLKOSR)

6.5.7.1 Reserved—Bits 15–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.7.2 PHASEA0 ($\overline{\text{PHSA}}$)—Bit 9

- 0 = Peripheral output function of GPIOB[7] is defined to be PHASEA0
- 1 = Peripheral output function of GPIOB[7] is defined to be the oscillator clock (MSTR_OSC, see **Figure 3-4**)

6.5.7.3 PHASEB0 ($\overline{\text{PHSB}}$)—Bit 8

- 0 = Peripheral output function of GPIOB[6] is defined to be PHASEB0
- 1 = Peripheral output function of GPIOB[6] is defined to be SYS_CLK2

6.5.8.5 GPIOB0 (B0)—Bit 4

This bit selects the alternate function for GPIOB0.

- 0 = $\overline{SS0}$ (default)
- 1 = TXD1

6.5.8.6 GPIOA5 (A5)—Bit 3

This bit selects the alternate function for GPIOA5.

- 0 = PWMA5
- 1 = SCLK1

6.5.8.7 GPIOA4 (A4)—Bit 2

This bit selects the alternate function for GPIOA4.

- 0 = PWMA4
- 1 = MOS1

6.5.8.8 GPIOA3 (A3)—Bit 1

This bit selects the alternate function for GPIOA3.

- 0 = PWMA3
- 1 = MISO1

6.5.8.9 GPIOA2 (A2)—Bit 0

This bit selects the alternate function for GPIOA2.

- 0 = PWMA2
- 1 = $\overline{SS1}$

6.5.9 Peripheral Clock Enable Register (SIM_PCE)

The Peripheral Clock Enable register is used to enable or disable clocks to the peripherals as a power savings feature. The clocks can be individually controlled for each peripheral on the chip.

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	ADCA	CAN	1	DEC0	1	TMRC	1	TMRA	SCI 1	SCI 0	SPI1	SPI0	1	PWMA
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 6-12 Peripheral Clock Enable Register (SIM_PCE)

6.5.9.1 Reserved—Bits 15–14

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

Part 7 Security Features

The 56F8323/56F8123 offer security features intended to prevent unauthorized users from reading the contents of the Flash memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the EOnCE interface, preventing access to internal code. Normal program execurtion is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8323/56F8123 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

Table 8-3 GPIO External Signals Map

GPIO Function	Peripheral Function	Package Pin	Notes
GPIOA0	*PWMA0*	3	*PWM is NOT available in 56F8123*
GPIOA1	*PWMA1*	4	*PWM is NOT available in 56F8123*
GPIOA2	*PWMA2* / $\overline{SSI}$	7	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA3	*PWMA3* / MISO1	8	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA4	*PWMA4* / MOSI1	9	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA5	*PWMA5* / SCLK1	10	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis *PWM is NOT available in 56F8123*
GPIOA6	*FAULTA0*	13	
GPIOA7	*FAULTA1*	14	
GPIOA8	*FAULTA2*	15	
GPIOA9	*ISA0*	16	
GPIOA10	*ISA0*	18	
GPIOA11	*ISA2*	19	
GPIOB0	$\overline{SS0}$ / TXD1	21	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB1	MISO0 / RXD1	22	SIM register SIM_GPS is used to select between SPI1 and PWMA on a pin-by-pin basis
GPIOB2	MOSI0	24	
GPIOB3	SCLK0	25	
GPIOB4	*HOME0* / TA3	49	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*
GPIOB5	*INDEX0* / TA2	50	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*
GPIOB6	*PHASEB0* / TA1	51	Quad Decoder 0 register DECCR is used to select between Decoder 0 and Timer A *Quad Decoder is NOT available in 56F8123*

Note: *The 56F8123 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8123 device.*

Table 10-1 Absolute Maximum Ratings

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply voltage	V_{DD_IO}		- 0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	- 0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		- 0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	- 0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 3, 4, 5	-0.3	6.0	V
Input Voltage (analog)	V_{INA}	Pin Groups 7, 8	-0.3	4.0	V
Output Voltage	V_{OUT}	Pin Groups 1, 2, 3	-0.3	4.0 6.0[1]	V
Output Voltage (open drain)	V_{OUTOD}	GPIO pins used in open drain mode	-0.3	6.0	V
Ambient Temperature (Automotive)	T_A		-40	125	°C
Ambient Temperature (Industrial)	T_A		-40	105	°C
Junction Temperature (Automotive)	T_J		-40	150	°C
Junction Temperature (Industrial)	T_J		-40	125	°C
Storage Temperature (Automotive)	T_{STG}		-55	150	°C
Storage Temperature (Industrial)	T_{STG}		-55	150	°C

1. If corresponding GPIO pin is configured as open drain.

Note: *Pins in italics are NOT available in the 56F8123 device.*

Pin Group 1: TC0-1, TC3, *FAULTA0-2*, *ISA0-2*, $\overline{SS0}$, MISO0, MOSI0, SCLK0, *HOME0*, *INDEX0*, *PHASEA0*, *PHASEB0*, *CAN_RX*, *CAN_TX*, GPIOC0-1

Pin Group 2: TDO

Pin Group 3: *PWMA0-5*

Pin Group 4: $\overline{RESET}$, TMS, TDI, $\overline{TRST}$, $\overline{IRQA}$

Pin Group 5: TCK

Pin Group 6: XTAL, EXTAL

Pin Group 7: ANA0-7

Pin Group 8: OCR_DIS

10.2 DC Electrical Characteristics

Note: *The 56F8123 device is specified to meet Industrial requirements only; PWM, CAN and Quad Decoder are NOT available on the 56F8123 device.*

Table 10-5 DC Electrical Characteristics

At Recommended Operating Conditions; see Table 10-4

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}		2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Low Voltage	V_{OL}		—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High pull-up enabled or disabled	I_{IH}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 3.0V to 5.5V
Digital Input Current High with pull-down	I_{IH}	Pin Group 5	40	80	160	µA	V_{IN} = 3.0V to 5.5V
Analog Input Current High	I_{IHA}	Pin Group 8	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$
ADC Input Current High	I_{IHADC}	Pin Group 7	—	0	+/- 3.5	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low pull-up enabled	I_{IL}	Pin Groups 1, 3, 4	-200	-100	-50	µA	V_{IN} = 0V
Digital Input Current Low pull-up disabled	I_{IL}	Pin Groups 1, 3, 4	—	0	+/- 2.5	µA	V_{IN} = 0V
Digital Input Current Low with pull-down	I_{IL}	Pin Group 5	—	0	+/- 2.5	µA	V_{IN} = 0V
Analog Input Current Low	I_{ILA}	Pin Group 8	—	0	+/- 2.5	µA	V_{IN} = 0V
ADC Input Current Low	I_{ILADC}	Pin Group 7	—	0	+/- 3.5	µA	V_{IN} = 0V
EXTAL Input Current Low clock input	I_{EXTAL}		—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
XTAL Input Current Low clock input	I_{XTAL}	CLKMODE = High	—	0	+/- 2.5	µA	$V_{IN} = V_{DDA}$ or 0V
		CLKMODE = Low	—	—	200	µA	$V_{IN} = V_{DDA}$ or 0V
Output Current High Impedance State	I_{OZ}	Pin Groups 1, 2, 3	—	0	+/- 2.5	µA	V_{OUT} = 3.0V to 5.5V or 0V
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 3, 4, 5	—	0.3	—	V	
Input Capacitance (EXTAL/XTAL)	C_{INC}		—	4.5	—	pF	
Output Capacitance (EXTAL/XTAL)	C_{OUTC}		—	5.5	—	pF	
Input Capacitance	C_{IN}		—	6	—	pF	
Output Capacitance	C_{OUT}		—	6	—	pF	

See Pin Groups in Table 10-1

Table 10-6 Power-On Reset Low Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Units
POR Trip Point Rising[1]	POR_R	—	—	—	V
POR Trip Point Falling	POR_F	1.75	1.8	1.9	V
LVI, 2.5V Supply, trip point[2]	$V_{EI2.5}$	—	2.14	—	V
LVI, 3.3V supply, trip point[3]	$V_{EI3.3}$	—	2.7	—	V
Bias Current	I_{bias}	—	110	130	µA

1. Both $V_{EI2.5}$ and $V_{EI3.3}$ thresholds must be met for POR to be released on power-up.
2. When V_{DD_CORE} drops below $V_{EI2.5}$, an interrupt is generated.
3. When V_{DD_CORE} drops below $V_{EI3.3}$, an interrupt is generated.

Table 10-7 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Enabled (OCR_DIS = Low)

Mode	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
RUN1_MAC	115mA	25mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	60mA	35µA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	5.7mA	0µA	360µA	• 4MHz Device Clock • All peripheral clocks are off • Relaxation oscillator is on • ADC powered off • PLL powered off
Stop2	5mA	0µA	145µA	• Relaxation oscillator is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching (Output switching current can be estimated from I = CVf for each output)
2. Includes Processor Core current supplied by internal voltage regulator

Table 10-9. Regulator Parameters (Continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current (output shorted to ground)	Iss	—	—	700	mA
Bias Current	I_{bias}	—	5.8	7	mA
Power-down Current	I_{pd}	—	0	2	µA
Short-Circuit Tolerance (output shorted to ground)	T_{RSC}	—	—	30	minutes

Table 10-10. PLL Parameters

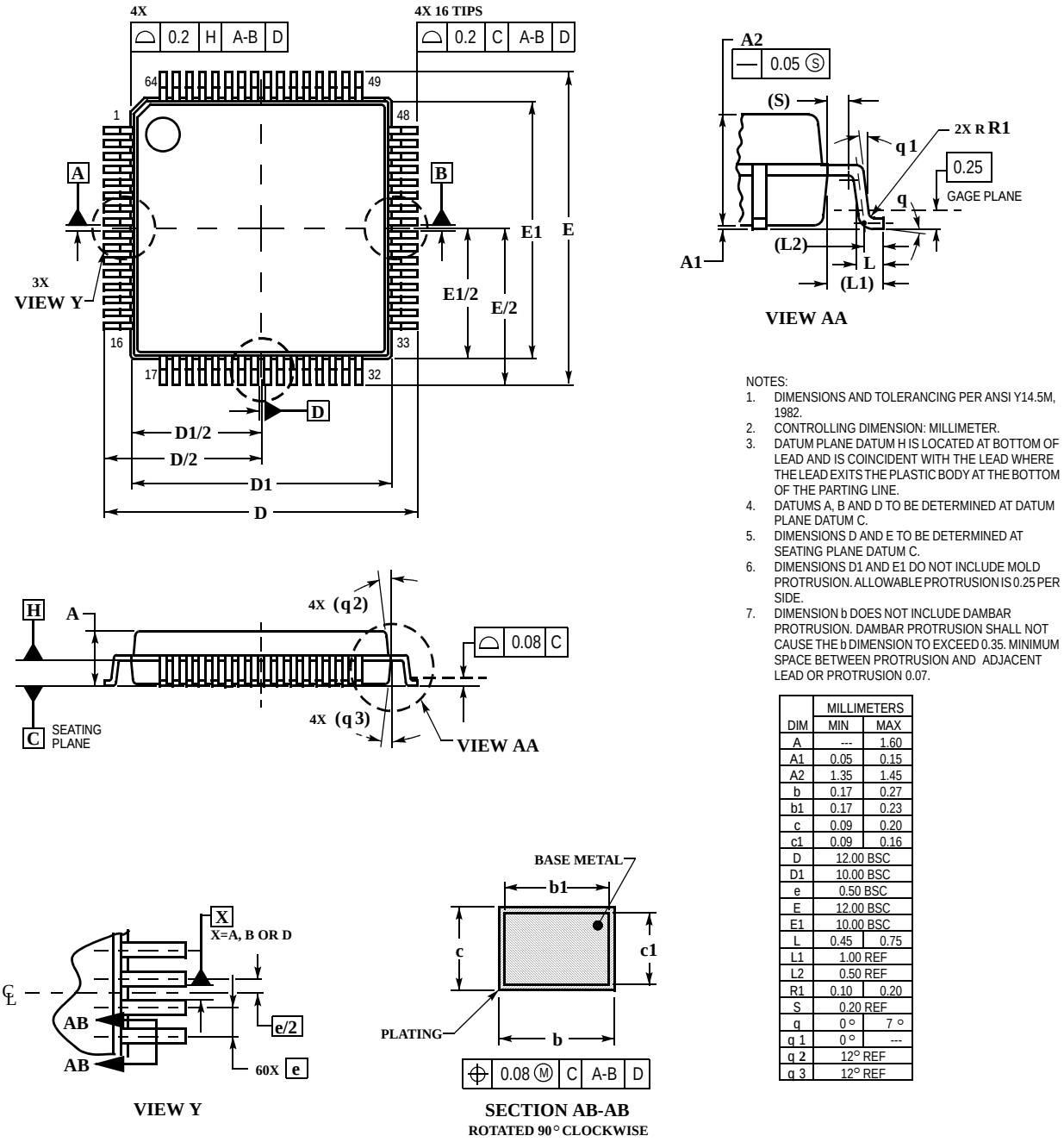
Characteristics	Symbol	Min	Typical	Max	Unit
PLL Start-up time	T_{PS}	0.3	0.5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Min-Max Period Variation	T_{PV}	120	—	200	ps
Peak-to-Peak Jitter	T_{PJ}	—	—	175	ps
Bias Current	I_{BIAS}	—	1.5	2	mA
Quiescent Current, power-down mode	I_{PD}	—	100	150	µA

10.2.2 Temperature Sense

Note: *Temperature Sensor is NOT available in the 56F8123 device.*

Table 10-11 Temperature Sense Parametrics

Characteristics	Symbol	Min	Typical	Max	Unit
Slope (Gain)[1]	m	—	7.762	—	mV/°C
Room Trim Temp. [1, 2]	T_{RT}	24	26	28	°C
Hot Trim Temp. (Industrial)[1,2]	T_{HT}	122	125	128	°C
Hot Trim Temp. (Automotive)[1,2]	T_{HT}	147	150	153	°C
Output Voltage @ V_{DDA_ADC} = 3.3V, T_J =0°C[1]	V_{TS0}	—	1.370	—	V
Supply Voltage	V_{DDA_ADC}	3.0	3.3	3.6	V



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE DATUM C.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	12.00 BSC	
D1	10.00 BSC	
e	0.50 BSC	
E	12.00 BSC	
E1	10.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
R1	0.10	0.20
S	0.20 REF	
q	0°	7°
q 1	0°	---
q 2	12° REF	
q 3	12° REF	

Figure 11-3 64-pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.