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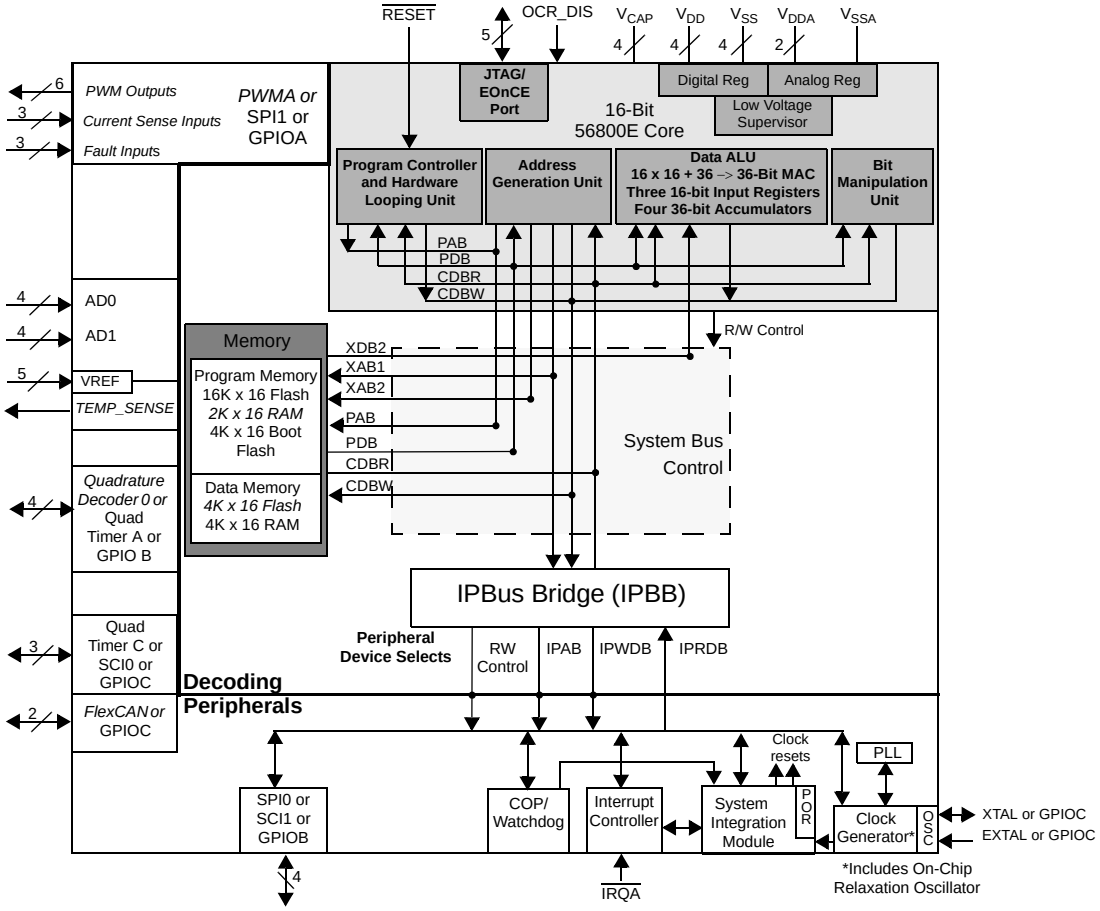
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	27
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8323vfbe

56F8323/56F8123 General Description

Note: *Features in italics are NOT available in the 56F8123 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 32KB Program Flash
- *4KB Program RAM*
- *8KB Data Flash*
- 8KB Data RAM
- 8KB Boot Flash
- *One 6-channel PWM module*
- Two 4-channel 12-bit ADCs
- *Temperature Sensor*
- *One Quadrature Decoder*
- *One FlexCAN module*
- Up to two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interfaces (SPIs)
- Two general-purpose Quad Timers
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 27 GPIO lines
- 64-pin LQFP Package



56F8323/56F8123 Block Diagram

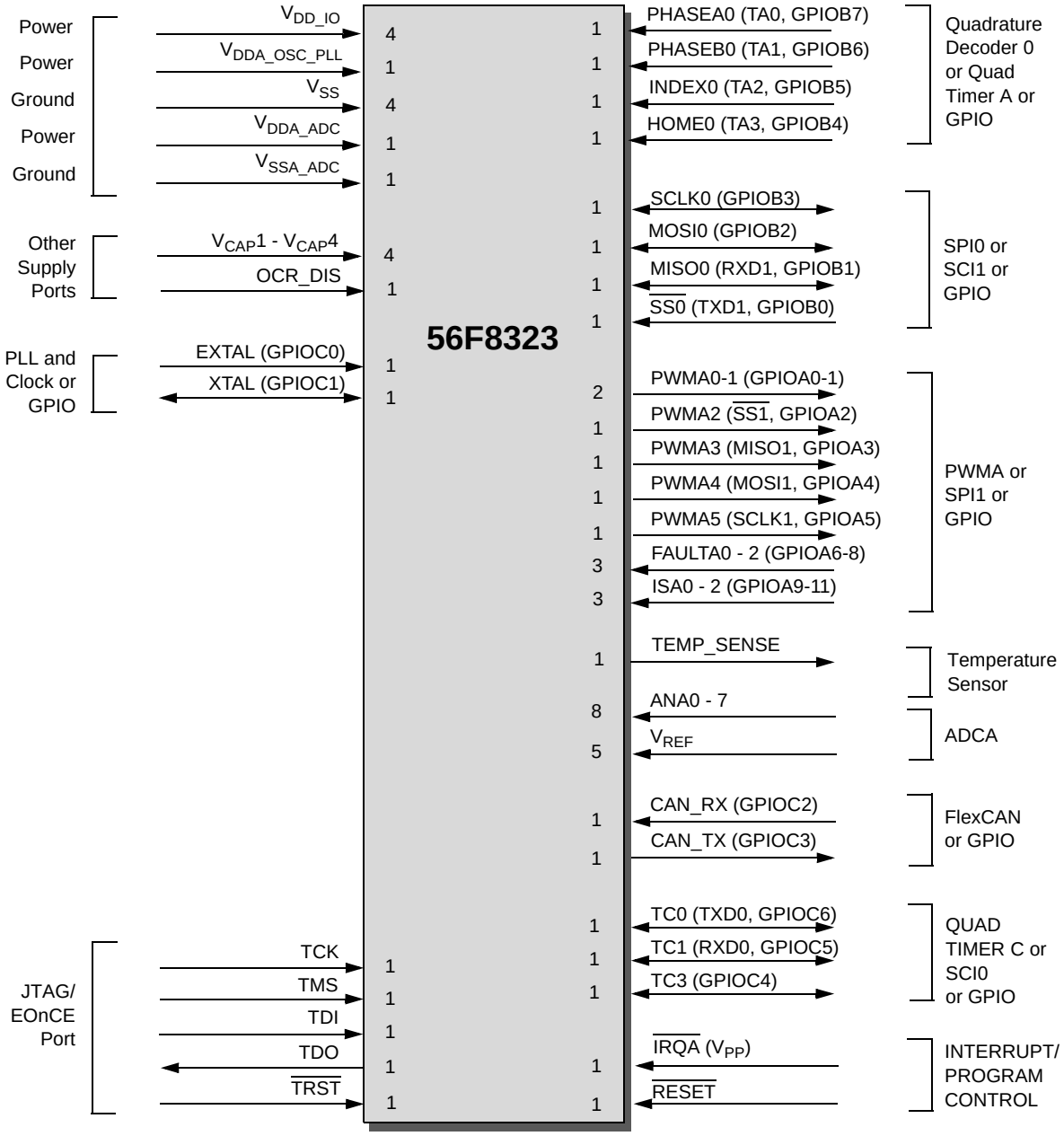


Figure 2-1 56F8323 Signals Identified by Functional Group (64-Pin LQFP)

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
HOME0	49	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 0, HOME input
(TA3)		Schmitt Input/ Output		**TA3** — Timer A, Channel 3
(GPIOB4)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(prescaler_ clock)		Output		**Clock Output** - can be used to monitor the internal prescaler_clock signal (see **Part 6.5.7** CLKO Select Register, SIM_CLKOSR). In the 56F8323, the default state after reset is HOME0. In the 56F8123, the default state is not one of the functions offered and must be reconfigured.
SCLK0	25	Schmitt Input/ Output	Input, pull-up enabled	**SPI 0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(GPIOB3)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCLK0.
MOSI0	24	Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**SPI 0 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(GPIOB2)		Schmitt Input/ Output		**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is MOSI0.

Table 2-2 Signal and Package Information for the 64-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
TC0	1	Schmitt Input/ Output	Input, pull-up enabled	**TC0** — Timer C, Channel 0
(TXD0)		Input		**Transmit Data** — SCI0 transmit data output
(GPIOC6)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TC0.
TC1	64	Schmitt Input/ Output	Input, pull-up enabled	**TC1** — Timer C, Channel 1
(RXD0)		Schmitt Input		**Receive Data** — SCI0 receive data input
(GPIOC5)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TC1.
TC3	63	Schmitt Input/ Output	Input, pull-up enabled	**TC3** — Timer C Channel 3
(GPIOC4)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TC3.
$\overline{\text{IRQA}}$	12	Schmitt Input	Input, pull-up enabled	**External Interrupt Request A** — The $\overline{\text{IRQA}}$ input is an asynchronous external interrupt request during Stop and Wait mode operation. During other operating modes, it is a synchronized external interrupt request which indicates an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered
(V_{PP})		Input		**V_{PP}** — This pin is used for Flash debugging purposes.
$\overline{\text{RESET}}$	2	Schmitt Input	Input, pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and the JTAG/EOnCE module must not be reset. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.

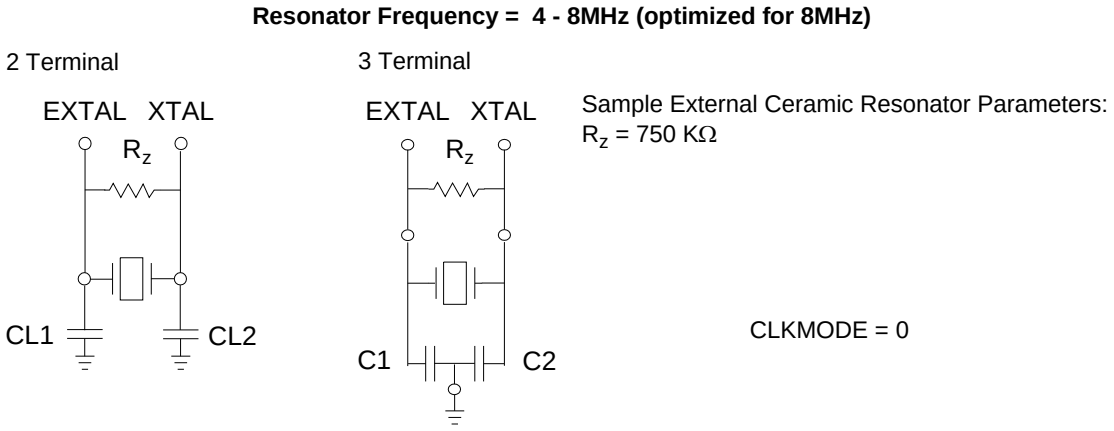


Figure 3-2 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a crystal resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.3 External Clock Source

The recommended method of connecting an external clock is illustrated in **Figure 3-3**. The external clock source is connected to XTAL and the EXTAL pin is grounded. The external clock input must be generated using a relatively low impedance driver, as the XTAL pin is actually the output pin of the oscillator (it has a very weak driver).

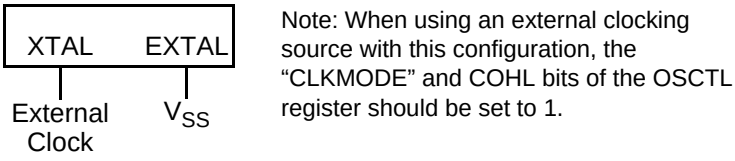


Figure 3-3 Connecting an External Clock Signal

3.3 Use of On-Chip Relaxation Oscillator

An internal relaxtion oscillator can supply the reference frequency when an external frequency source of crystal is not used. During a boot or reset sequence, the relaxation oscillator is enabled by default, and the PRECS bit in the PLLCR word is set to 0. If an external oscillator is connected, the relaxation oscillator can be deselected instead by setting the PRECS bit in the PLLCR to 1. If a changeover between internal and external oscillators is required at start up, internal device circuits compensate for any asynchronous transitions between the two clock signals so that no glitches occur in the resulting master clock to the chip. When changing clocks, the user must ensure that the clock source is not switched until the desired clock is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within ± 0.1% of 8MHz by trimming an internal capacitor. Bits 0-9 of the OSCTL (oscillator control) register allow the user to set in an additional offset (trim) to this preset value

4.4 Data Map

Note: *Data Flash is NOT available on the 56F8122 device.*

Table 4-4 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	RESERVED
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 2000	RESERVED
X:$00 1FFF X:$00 1000	*On-Chip Data Flash* 8KB
X:$00 0FFF X:$00 0000	On-Chip Data RAM 8KB[2]

1. All addresses are 16-bit Word addresses.
2. The Data RAM is organized as a 2K x 32-bit memory to allow single-cycle, long-word operations.

4.5 Flash Memory Map

Figure 4-1 illustrates the Flash Memory (FM) map on the system bus.

Flash Memory is divided into three functional blocks. The Program and boot memories reside on the Program Memory buses. They are controlled by one set of banked registers. Data Memory Flash resides on the Data Memory buses and is controlled separately by its own set of banked registers.

The top nine words of the Program Memory Flash are treated as special memory locations. The content of these words is used to control the operation of the Flash controller. Because these words are part of the Flash Memory content, their state is maintained during power-down and reset. During chip initialization, the content of these memory locations is loaded into Flash Memory control registers, detailed in the Flash Memory chapter of the **56F8300 Peripheral User Manual**. These configuration parameters are located between $00_3FF7 and $00_3FFF.

4.6 EOnCE Memory Map

Table 4-6 EOnCE Memory Map

Address	Register Acronym	Register Name
		Reserved
X:$FF FF8A	OESCR	External Signal Control Register
		Reserved
X:$FF FF8E	OBCNTR	Breakpoint Unit [0] Counter
		Reserved
X:$FF FF90	OBMSK (32 bits)	Breakpoint 1 Unit [0] Mask Register
X:$FF FF91	—	Breakpoint 1 Unit [0] Mask Register
X:$FF FF92	OBAR2 (32 bits)	Breakpoint 2 Unit [0] Address Register
X:$FF FF93	—	Breakpoint 2 Unit [0] Address Register
X:$FF FF94	OBAR1 (24 bits)	Breakpoint 1 Unit [0] Address Register
X:$FF FF95	—	Breakpoint 1 Unit [0] Address Register
X:$FF FF96	OBCR (24 bits)	Breakpoint Unit [0] Control Register
X:$FF FF97	—	Breakpoint Unit [0] Control Register
X:$FF FF98	OTB (21-24 bits/stage)	Trace Buffer Register Stages
X:$FF FF99	—	Trace Buffer Register Stages
X:$FF FF9A	OTBPR (8 bits)	Trace Buffer Pointer Register
X:$FF FF9B	OTBCR	Trace Buffer Control Register
X:$FF FF9C	OBASE (8 bits)	Peripheral Base Address Register
X:$FF FF9D	OSR	Status Register
X:$FF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:$FF FF9F	—	Instruction Step Counter
X:$FF FFA0	OCR (bits)	Control Register
		Reserved
X:$FF FFFC	OCLSR (8 bits)	Core Lock / Unlock Status Register
X:$FF FFFD	OTXRXSR (8 bits)	Transmit and Receive Status and Control Register
X:$FF FFFE	OTX / ORX (32 bits)	Transmit Register / Receive Register
X:$FF FFFF	OTX1 / ORX1	Transmit Register Upper Word Receive Register Upper Word

Table 4-8 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

Register Acronym	Address Offset	Register Description
TMRA2_CMPLD2	$29	Comparator Load Register 2
TMRA2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRA3_CMP1	$30	Compare Register 1
TMRA3_CMP2	$31	Compare Register 2
TMRA3_CAP	$32	Capture Register
TMRA3_LOAD	$33	Load Register
TMRA3_HOLD	$34	Hold Register
TMRA3_CNTR	$35	Counter Register
TMRA3_CTRL	$36	Control Register
TMRA3_SCR	$37	Status and Control Register
TMRA3_CMPLD1	$38	Comparator Load Register 1
TMRA3_CMPLD2	$39	Comparator Load Register 2
TMRA3_COMSCR	$3A	Comparator Status and Control Register

Table 4-9 Quad Timer C Registers Address Map (TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC0_CMP1	$0	Compare Register 1
TMRC0_CMP2	$1	Compare Register 2
TMRC0_CAP	$2	Capture Register
TMRC0_LOAD	$3	Load Register
TMRC0_HOLD	$4	Hold Register
TMRC0_CNTR	$5	Counter Register
TMRC0_CTRL	$6	Control Register
TMRC0_SCR	$7	Status and Control Register
TMRC0_CMPLD1	$8	Comparator Load Register 1
TMRC0_CMPLD2	$9	Comparator Load Register 2
TMRC0_COMSCR	$A	Comparator Status and Control Register
		Reserved
TMRC1_CMP1	$10	Compare Register 1
TMRC1_CMP2	$11	Compare Register 2
TMRC1_CAP	$12	Capture Register
TMRC1_LOAD	$13	Load Register

Table 4-27 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8123 device

Register Acronym	Address Offset	Register Description
FCMB1_DATA	$4B	Message Buffer 1 Data Register
FCMB1_DATA	$4C	Message Buffer 1 Data Register
FCMB1_DATA	$4D	Message Buffer 1 Data Register
FCMB1_DATA	$4E	Message Buffer 1 Data Register
		Reserved
FCMB2_CONTROL	$50	Message Buffer 2 Control / Status Register
FCMB2_ID_HIGH	$51	Message Buffer 2 ID High Register
FCMB2_ID_LOW	$52	Message Buffer 2 ID Low Register
FCMB2_DATA	$53	Message Buffer 2 Data Register
FCMB2_DATA	$54	Message Buffer 2 Data Register
FCMB2_DATA	$55	Message Buffer 2 Data Register
FCMB2_DATA	$56	Message Buffer 2 Data Register
		Reserved
FCMB3_CONTROL	$58	Message Buffer 3 Control / Status Register
FCMB3_ID_HIGH	$59	Message Buffer 3 ID High Register
FCMB3_ID_LOW	$5A	Message Buffer 3 ID Low Register
FCMB3_DATA	$5B	Message Buffer 3 Data Register
FCMB3_DATA	$5C	Message Buffer 3 Data Register
FCMB3_DATA	$5D	Message Buffer 3 Data Register
FCMB3_DATA	$5E	Message Buffer 3 Data Register
		Reserved
FCMB4_CONTROL	$60	Message Buffer 4 Control / Status Register
FCMB4_ID_HIGH	$61	Message Buffer 4 ID High Register
FCMB4_ID_LOW	$62	Message Buffer 4 ID Low Register
FCMB4_DATA	$63	Message Buffer 4 Data Register
FCMB4_DATA	$64	Message Buffer 4 Data Register
FCMB4_DATA	$65	Message Buffer 4 Data Register
FCMB4_DATA	$66	Message Buffer 4 Data Register
		Reserved
FCMB5_CONTROL	$68	Message Buffer 5 Control / Status Register
FCMB5_ID_HIGH	$69	Message Buffer 5 ID High Register
FCMB5_ID_LOW	$6A	Message Buffer 5 ID Low Register
FCMB5_DATA	$6B	Message Buffer 5 Data Register

5.6.4.3 FlexCAN Wake Up Interrupt Priority Level (FCWKUP IPL)— Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.4 FlexCAN Error Interrupt Priority Level (FCERR IPL)— Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.5 FlexCAN Bus Off Interrupt Priority Level (FCBOFF IPL)— Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.5 Interrupt Priority Register 4 (IPR4)

Base + $4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-7 Interrupt Priority Register 4 (IPR4)

5.6.5.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR5)

5.6.6.1 Reserved—Bits 15–12

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.6.2 SCI1 Receiver Full Interrupt Priority Level (SCI1_RCV IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.4 Reserved—Bits 9–8

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.5 ADC A Zero Crossing or Limit Error Interrupt Priority Level (ADCA_ZC IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.10.7 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.10.8 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.11 Vector Base Address Register (VBA)

Base + $A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	VECTOR BASE ADDRESS												
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-13 Vector Base Address Register (VBA)

5.6.11.1 Reserved—Bits 15–13

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14 Fast Interrupt 0 Vector Address High Register (FIVAH0)

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-16 Fast Interrupt 0 Vector Address High Register (FIVAH0)

5.6.14.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.14.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

5.6.15 Fast Interrupt 1 Match Register (FIM1)

Base + $E	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-17 Fast Interrupt 1 Match Register (FIM1)

5.6.15.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0, but cannot be modified by writing.

5.6.15.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 6–0

This value determines which IRQ will be a Fast Interrupt 1. Fast interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first; for details, see **Part 5.3.3**. IRQs used as fast interrupts *must* be set to priority level 2. Unexpected results will occur if a fast interrupt vector is set to any other priority. Fast interrupts automatically become the highest-priority level 2 interrupt, regardless of their location in the interrupt table, prior to being declared as fast interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to **Table 4-3**.

6.5 Register Descriptions

Table 6-1 SIM Registers (SIM_BASE = $00F350)

Address Offset	Address Acronym	Register Name	Section Location
Base + $0	SIM_CONTROL	Control Register	6.5.1
Base + $1	SIM_RSTSTS	Reset Status Register	6.5.2
Base + $2	SIM_SCR0	Software Control Register 0	6.5.3
Base + $3	SIM_SCR1	Software Control Register 1	6.5.3
Base + $4	SIM_SCR2	Software Control Register 2	6.5.3
Base + $5	SIM_SCR3	Software Control Register 3	6.5.3
Base + $6	SIM_MSH_ID	Most Significant Half of JTAG ID	6.5.4
Base + $7	SIM_LSH_ID	Least Significant Half of JTAG ID	6.5.5
Base + $8	SIM_PUDR	Pull-up Disable Register	6.5.6
		Reserved	
Base + $A	SIM_CLKOSR	CLKO Select Register	6.5.7
Base + $B	SIM_GPS	GPIO Peripheral Select Register	6.5.7
Base + $C	SIM_PCE	Peripheral Clock Enable Register	6.5.8
Base + $D	SIM_ISALH	I/O Short Address Location High Register	6.5.9
Base + $E	SIM_ISALL	I/O Short Address Location Low Register	6.5.10

Part 7 Security Features

The 56F8323/56F8123 offer security features intended to prevent unauthorized users from reading the contents of the Flash memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable the EOnCE interface, preventing access to internal code. Normal program execurtion is otherwise unaffected.

7.2 Flash Access Blocking Mechanisms

The 56F8323/56F8123 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Unsecured Mode
- Secure Mode (EOnCE disabled)

When Flash security is enabled as described in the Flash Memory module specification, the device will disable the EOnCE debug interface.

7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The $\overline{\text{TRST}}$, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

EXAMPLE 1: If the system clock is the 8MHz crystal frequency because the PLL has not been set up, the input clock will be below 12.8MHz, so PRDIV8=FM_CLKDIV[6]=0. Using the following equation yields a DIV value of 19 for a clock of 200kHz, and a DIV value of 20 for a clock of 190kHz. This translates into an FM_CLKDIV[6:0] value of $13 or $14, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

EXAMPLE 2: In this example, the system clock has been set up with a value of 32MHz, making the FM input clock 16MHz. Because that is greater than 12.8MHz, PRDIV8=FM_CLKDIV[6]=1. Using the following equation yields a DIV value of 9 for a clock of 200kHz, and a DIV value of 10 for a clock of 181kHz. This translates to an FM_CLKDIV[6:0] value of $49 or $4A, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)(8)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence has completed. For details, see the JTAG Section in the **56F8300 Peripheral User Manual**.

Note: Once the lockout recovery sequence has completed, the user must reset both the JTAG TAP controller (by asserting $\overline{\text{TRST}}$) and the device (by asserting external chip reset) to return to normal unsecured operation.

7.2.4 Product Analysis

The recommended method of unsecuring a programmed device for product analysis of field failures is via the backdoor key access. The customer would need to supply Technical Support with the backdoor key and the protocol to access the backdoor routine in the Flash. Additionally, the KEYEN bit that allows backdoor key access must be set.

An alternative method for performing analysis on a secured microcontroller would be to mass-erase and reprogram the Flash with the original code, but to modify the security bytes.

To insure that a customer does not inadvertently lock himself out of the device during programming, it is recommended that he program the backdoor access key first, his application code second and the security bytes within the FM configuration field last.

Table 10-8 Current Consumption per Power Supply Pin (Typical)
On-Chip Regulator Disabled (OCR_DIS = High)

Mode	I_{DD_Core}	I_{DD_IO}[1]	I_{DD_ADC}	$I_{DD\_OSC\_PLL}$	Test Conditions
RUN1_MAC	110mA	13µA	25mA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • Continuous MAC instructions with fetches from Data RAM • ADC powered on and clocked
Wait3	55mA	13µA	35µA	2.5mA	• 60MHz Device Clock • All peripheral clocks are enabled • ADC powered off
Stop1	700µA	13µA	0µA	360µA	• 4MHz Device Clock • All peripheral clocks are off • Relaxation oscillator is on • ADC powered off • PLL powered off
Stop2	100µA	13µA	0µA	145µA	• Relaxation oscillator is off • All peripheral clocks are off • ADC powered off • PLL powered off

1. No Output Switching (Output switching current can be estimated from I = CVf for each output)

10.2.1 Voltage Regulator Specifications

The 56F8323/56F8123 have two on-chip regulators. One supplies the PLL and has no external pins; therefore, it has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.6V to the device's core logic. This regulator requires two external 2.2µF, or greater, capacitors for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pins. The specifications for this regulator are shown in **Table 10-9**.

Table 10-9. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Unloaded Output Voltage (0mA Load)	V_{RNL}	2.25	—	2.75	V
Loaded Output Voltage (200mA load)	V_{RL}	2.25	—	2.75	V
Line Regulation @ 250mA load (V_{DD}33 ranges from 3.0V to 3.6V)	V_R	2.25	—	2.75	V

11.2 56F8123 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8123. This device comes in a 64-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline for the 64-pin LQFP, **Figure 11-3** shows the mechanical parameters for this package, and **Table 11-1** lists the pin-out for the 64-pin LQFP case.

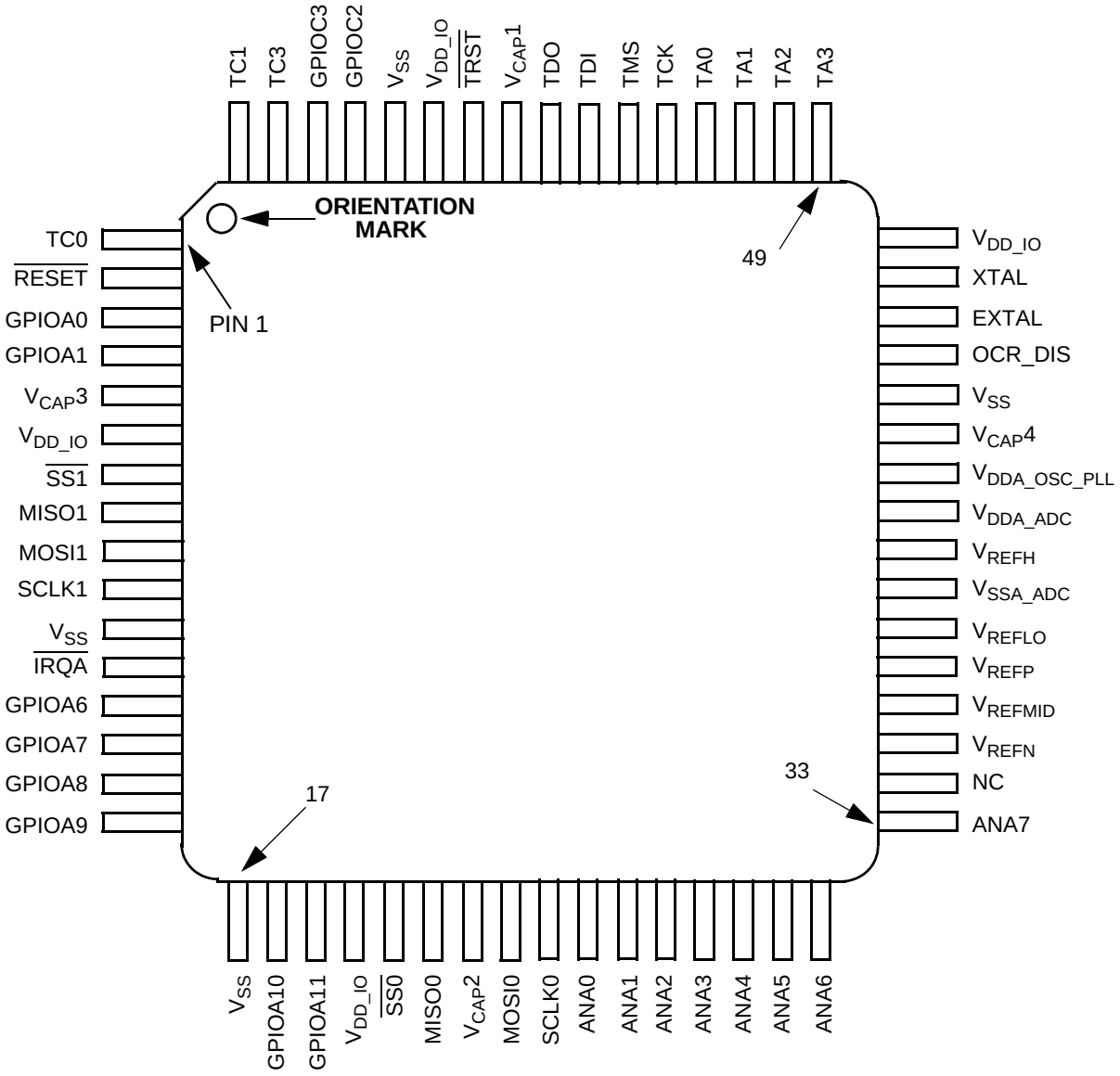


Figure 11-2 Top View, 56F8123 64-Pin LQFP Package

Table 11-2 56F8123 64-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	TC0	17	V_{SS}	33	ANA7	49	TA3
2	$\overline{\text{RESET}}$	18	GPIOA10	34	NC	50	TA2
3	GPIOA0	19	GPIOA11	35	V_{REFN}	51	TA1
4	GPIOA1	20	V_{DD_IO}	36	V_{REFMID}	52	TA0
5	$V_{CAP}3$	21	$\overline{\text{SS0}}$	37	V_{REFP}	53	TCK
6	V_{DD_IO}	22	MISO0	38	V_{REFLO}	54	TMS
7	$\overline{\text{SS1}}$	23	$V_{CAP}2$	39	V_{SSA_ADC}	55	TDI
8	MISO1	24	MOSI0	40	V_{REFH}	56	TDO
9	MOSI1	25	SCLK0	41	V_{DDA_ADC}	57	$V_{CAP}1$
10	SCLK1	26	ANA0	42	$V_{DDA\_OSC\_PLL}$	58	$\overline{\text{TRST}}$
11	V_{SS}	27	ANA1	43	$V_{CAP}4$	59	V_{DD_IO}
12	$\overline{\text{IRQA}}$	28	ANA2	44	V_{SS}	60	V_{SS}
13	GPIOA6	29	ANA3	45	OCR_DIS	61	GPIOC2
14	GPIOA7	30	ANA4	46	EXTAL	62	GPIOC3
15	GPIOA8	31	ANA5	47	XTAL	63	TC3
16	GPIOA9	32	ANA6	48	V_{DD_IO}	64	TC1

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8323/56F8123:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor