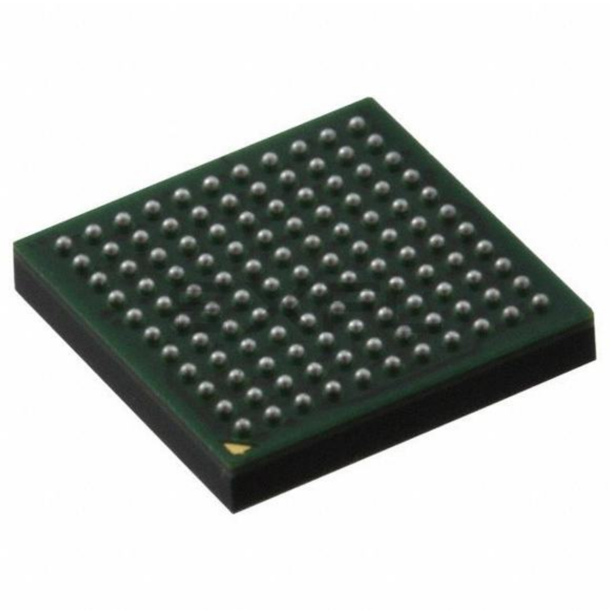

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22dx128vmc5

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK22 and MK22 .

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K22
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory

Table continues on the next page...

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
##	Kinetis family	• 1# = K11/K12 • 2# = K21/K22
C	Speed	• G = 50 MHz
F	Flash memory configuration	• G = 128 KB + Flex • H = 256 KB + Flex • 9 = 512 KB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• MC = 121 MAPBGA

This tables lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK22DX256VLK5	M22GHVLF
MK22DX128VMC5	M22GGVLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				1
	• @ full temperature range	—	1.0	μA	
	• @ 25 °C	—	0.1	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • 1.71 V/(V_{DD} slew rate) ≤ 300 μs • 1.71 V/(V_{DD} slew rate) > 300 μs	 — —	 300 1.7 V / (V_{DD} slew rate)	μs	1
	• VLLS0 → RUN	—	135	μs	
	• VLLS1 → RUN	—	135	μs	
	• VLLS2 → RUN	—	85	μs	
	• VLLS3 → RUN	—	85	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8 V • @ 3.0 V	 — —	 12.98 12.93	 14 13.8	 mA mA	2

Table continues on the next page...

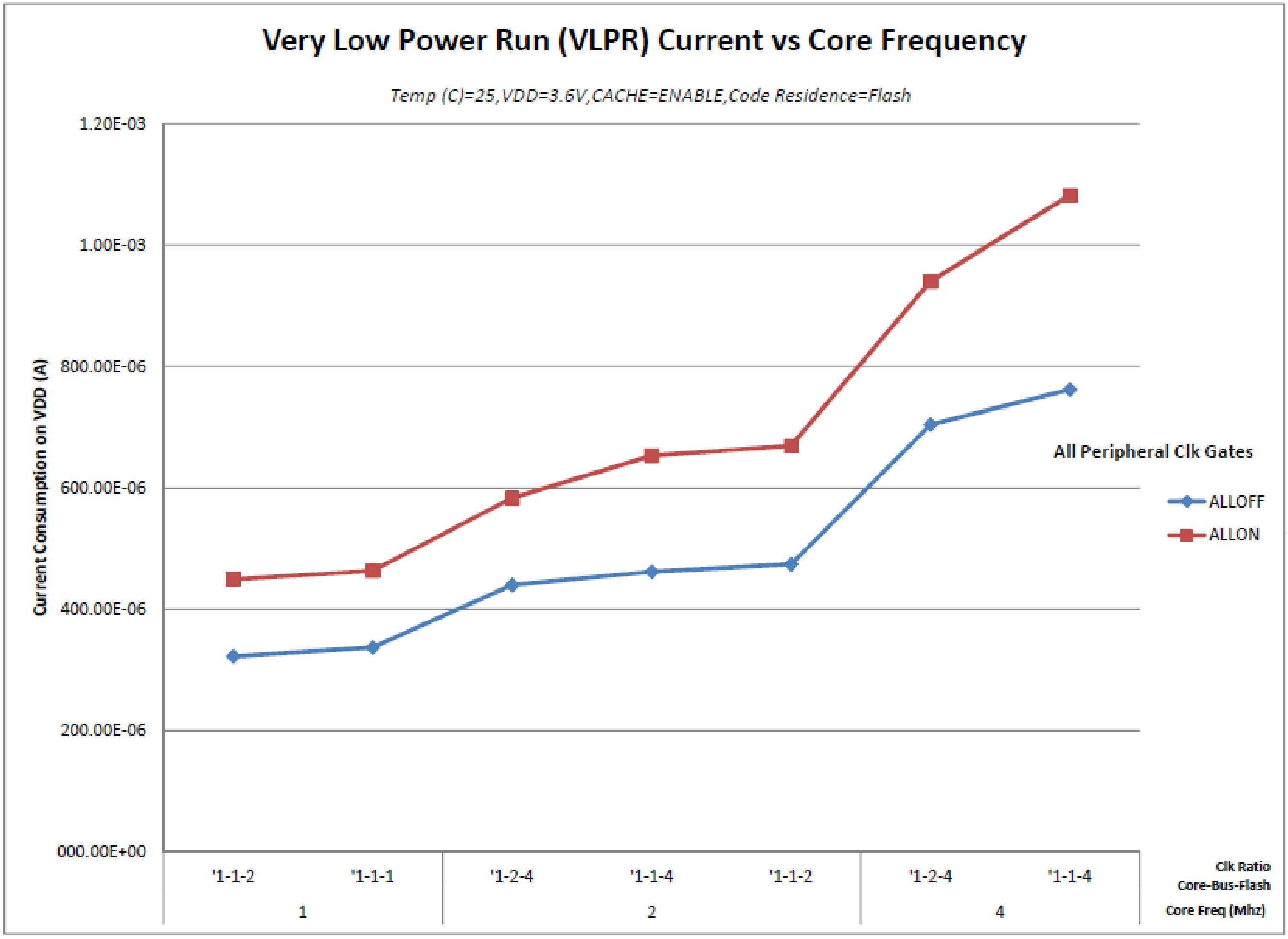

Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors 1

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBμV	2, 3
V_{RE2}	Radiated emissions voltage, band 2	50–150	21	dBμV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	19	dBμV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBμV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

3. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 48MHz
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	

Table continues on the next page...

3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	79	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	67	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	42	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	29	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	°C/W	5

Table continues on the next page...

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.
3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications

Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	
	Program Partition for EEPROM execution time					
$t_{pgmpart64k}$	• 64 KB FlexNVM	—	138	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	μs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup		475	2000	μs	
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1800	μs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2050	μs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 24 and Table 25 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 24. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

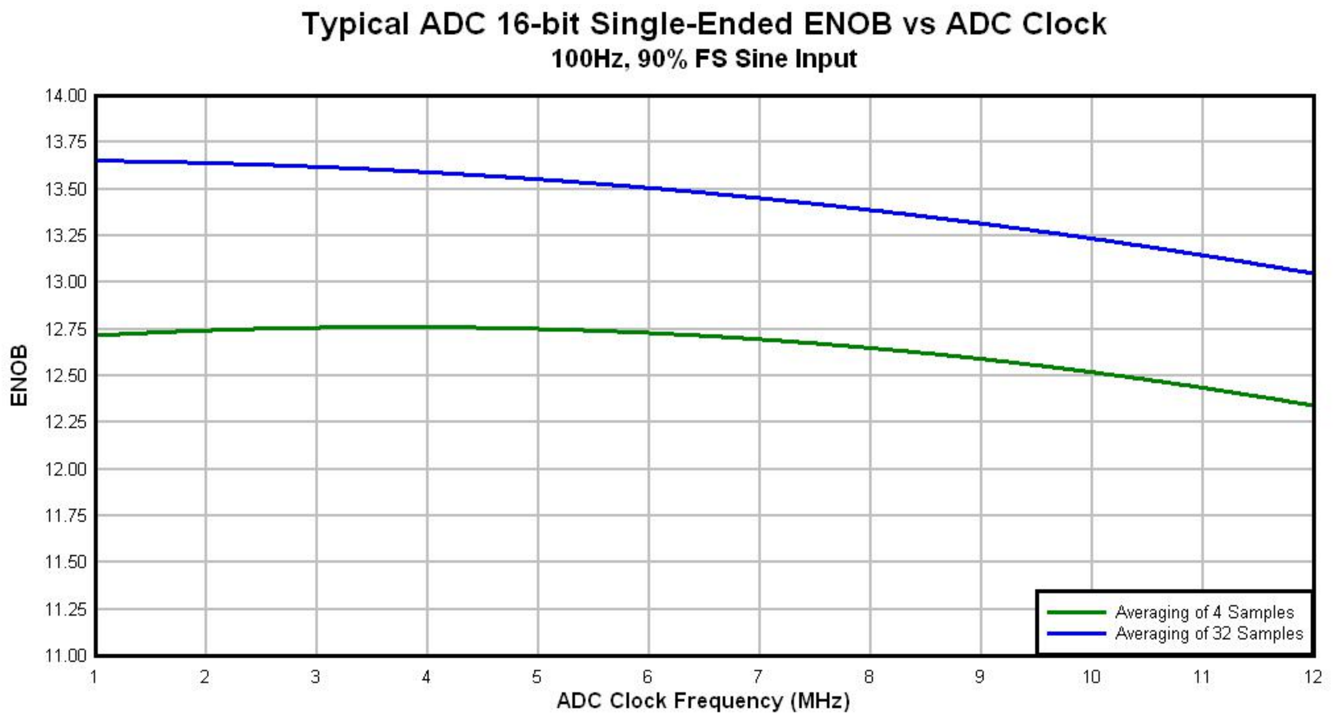

Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs

Table continues on the next page...

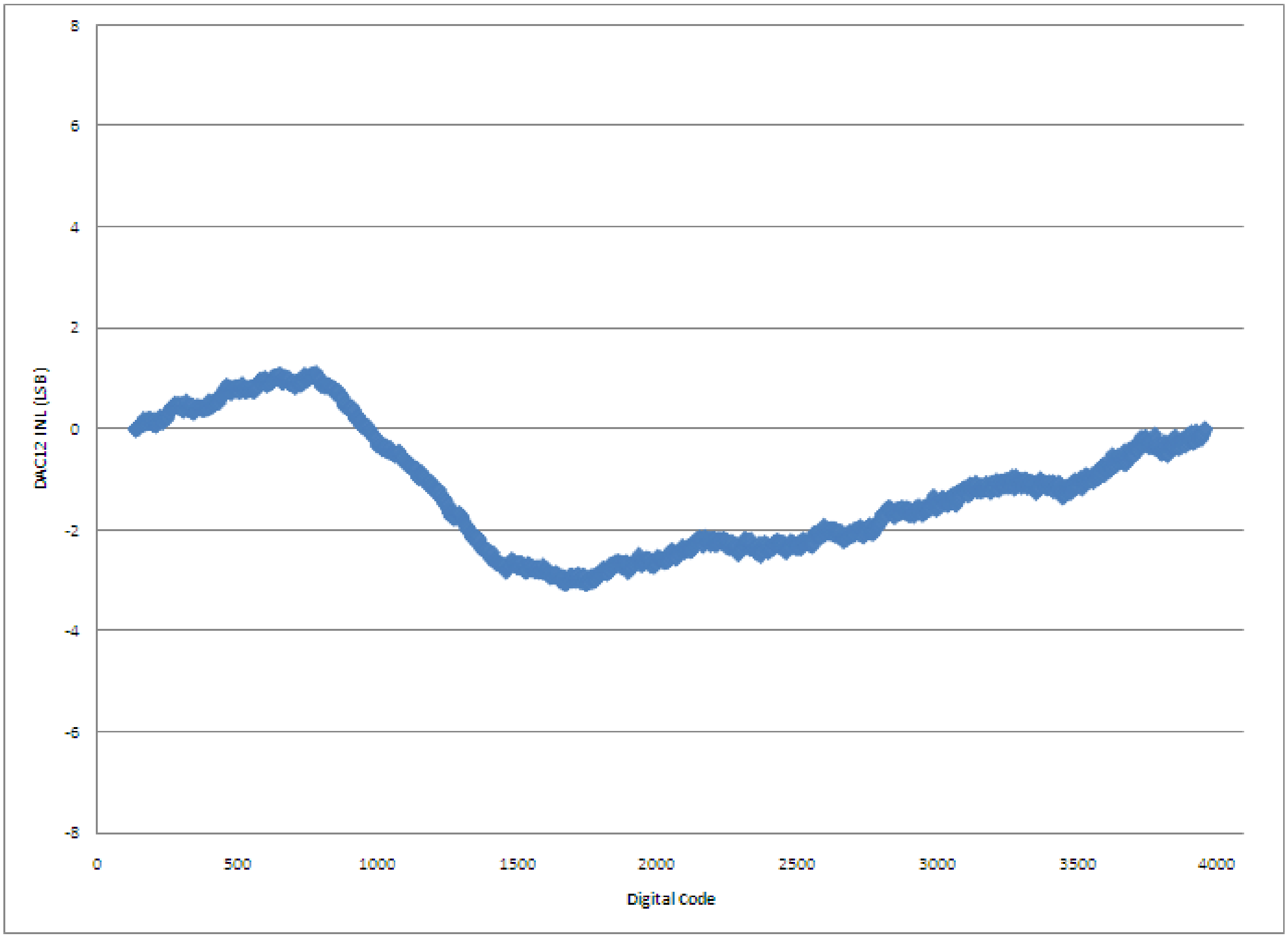

Figure 14. Typical INL error vs. digital code

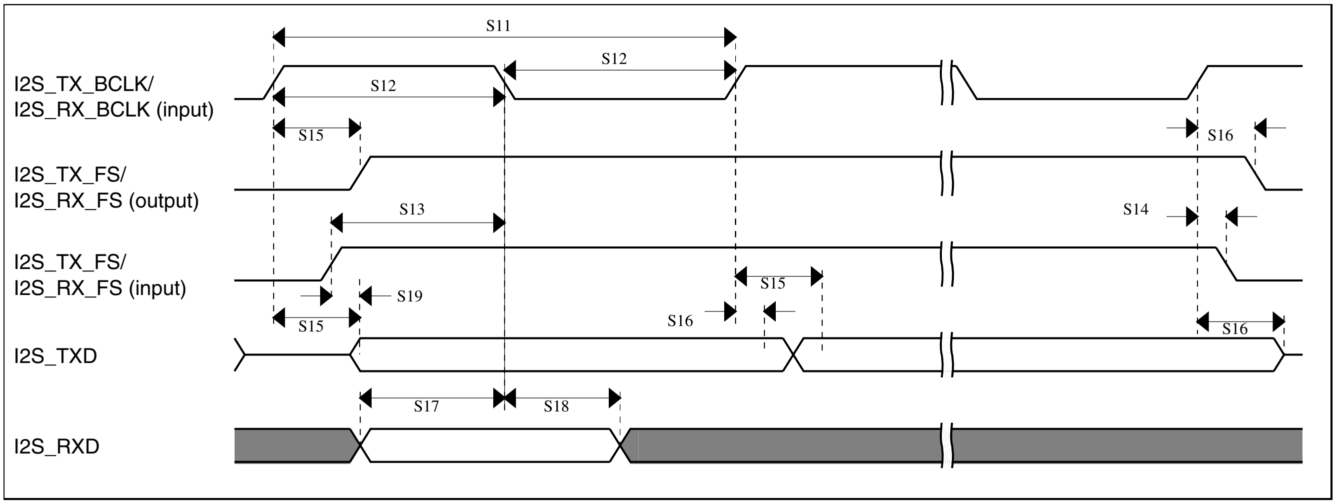

Figure 21. I2S/SAI timing — slave modes

6.8.9 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

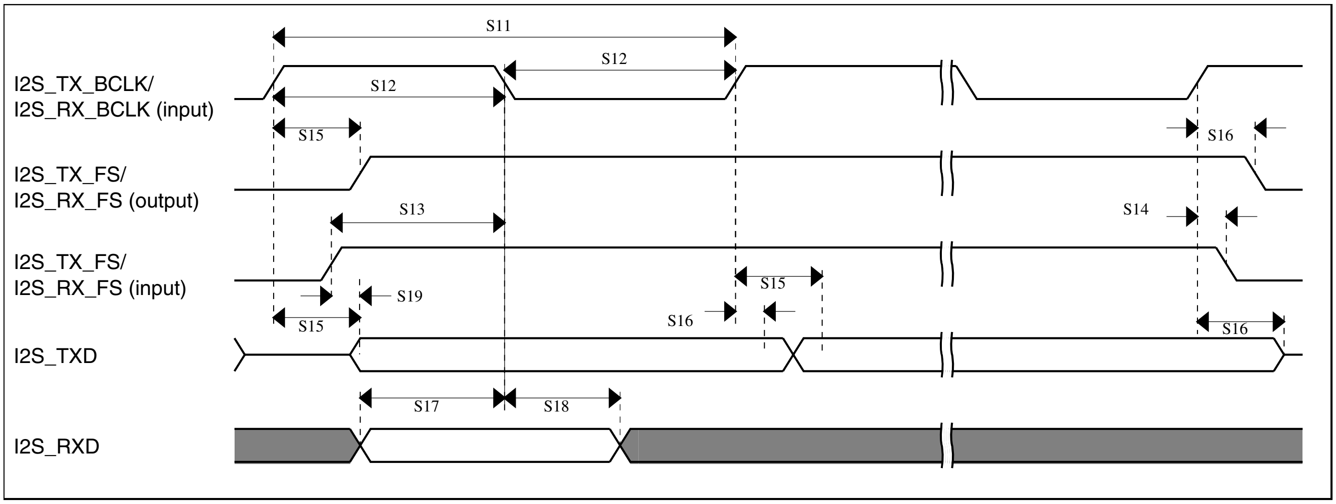

Figure 23. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
81-pin MAPBGA	98ASA00344D
121-pin MAPBGA	98ASA00344D

8 Pinout

8.1 K22 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
E3	ADC0_SE11	ADC0_SE11	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	I2C1_SCL	SPI1_SIN	
E2	ADC0_DP1	ADC0_DP1	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
F4	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	
H7	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX		TRACE_D0			
G4	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
E6	VDD	VDD								
G7	VSS	VSS								
L6	VSS	VSS								
F1	USB0_DP	USB0_DP								
F2	USB0_DM	USB0_DM								
G1	VOUT33	VOUT33								
G2	VREGIN	VREGIN								
K1	ADC0_DP0	ADC0_DP0								
K2	ADC0_DM0	ADC0_DM0								

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G10	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
G9	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
G8	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0		
D10	DISABLED		PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1		
C10	DISABLED		PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		
B11	DISABLED		PTB12	UART3_RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_PHA		
C11	DISABLED		PTB13	UART3_CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_PHB		
B10	DISABLED		PTB16	SPI1_SOUT	UART0_RX			EWM_IN	FTM_CLKIN0	
E9	DISABLED		PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	FTM_CLKIN1	
D9	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK				
C9	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS				
B9	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1		
D8	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
C8	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
B8	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
G3	VSS	VSS								
E5	VDD	VDD								
A8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
D7	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	FTM0_CH2	
C7	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
B7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS				
A7	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
D6	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_BCLK		FTM2_FLT0		
C6	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS				
C5	DISABLED		PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1				
B6	DISABLED		PTC12							
A6	DISABLED		PTC13							
D5	DISABLED		PTC16		UART3_RX					
C4	DISABLED		PTC17		UART3_TX					
D4	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b					
D3	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
C3	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	I2C0_SCL				
B3	DISABLED		PTD3	SPI0_SIN	UART2_TX	I2C0_SDA				

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A3	ADC0_SE21	ADC0_SE21	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
A2	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b		
B2	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
A1	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
A11	NC	NC								
K3	NC	NC								
H4	NC	NC								
F3	NC	NC								
H1	NC	NC								
H2	NC	NC								
J1	NC	NC								
J2	NC	NC								
J3	NC	NC								
H3	NC	NC								
K4	NC	NC								
H5	NC	NC								
J5	NC	NC								
H6	NC	NC								
J9	NC	NC								
J4	NC	NC								
H11	NC	NC								
F11	NC	NC								
E11	NC	NC								
D11	NC	NC								
E10	NC	NC								
F10	NC	NC								
F9	NC	NC								
F8	NC	NC								
E8	NC	NC								
E7	NC	NC								
F7	NC	NC								
A5	NC	NC								
B5	NC	NC								
B4	NC	NC								
A4	NC	NC								
A10	NC	NC								
A9	NC	NC								
B1	NC	NC								

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C2	NC	NC								
C1	NC	NC								
D2	NC	NC								
D1	NC	NC								
E1	NC	NC								

8.2 K22 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.