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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	108
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2917fbd144-551

2.2 ARM968E-S processor

The ARM968E-S is a general purpose 32-bit RISC processor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective controller core.

Amongst the most compelling features of the ARM968E-S are:

- Separate directly connected instruction and data Tightly Coupled Memory (TCM) interfaces
- Write buffers for the AHB and TCM buses
- Enhanced 16 × 32 multiplier capable of single-cycle MAC operations and 16-bit fixed-point DSP instructions to accelerate signal-processing algorithms and applications.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. The ARM968E-S is based on the ARMv5TE five-stage pipeline architecture. Typically, in a three-stage pipeline architecture, while one instruction is being executed its successor is being decoded and a third instruction is being fetched from memory. In the five-stage pipeline additional stages are added for memory access and write-back cycles.

The ARM968E-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions or to applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM968E-S processor has two instruction sets:

- Standard 32-bit ARMv5TE set
- 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit controller using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code can provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM controller connected to a 16-bit memory system.

The ARM968E-S processor is described in detail in the ARM968E-S data sheet Ref. 2.

2.3 On-chip flash memory system

The LPC2917/19 includes a 512 kB or 768 kB flash memory system. This memory can be used for both code and data storage. Programming of the flash memory can be accomplished in several ways. It may be programmed in-system via a serial port (e.g., CAN).

- Allows minimization of system operating power consumption in any configuration.
- Standard ARM test and debug interface with real-time in-circuit emulator.
- Boundary-scan test supported.
- Dual power supply:
  - CPU operating voltage: 1.8 V ± 5 %.
  - I/O operating voltage: 2.7 V to 3.6 V; inputs tolerant up to 5.5 V.
- 144-pin LQFP package.
- –40 °C to 85 °C ambient operating temperature range.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2917FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2919FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Part options

Type number	Flash memory	RAM	SMC	LIN 2.0	Package
LPC2917FBD144	512 kB	80 kB (including TCMs)	32-bit	2	LQFP144
LPC2919FBD144	768 kB	80 kB (including TCMs)	32-bit	2	LQFP144

found in the specific subsystem description. Some branch clocks have special protection since they clock vital system parts of the device and should (for example) not be switched off. See Section 8.8.6 for more details of how to control the individual branch clocks.

Table 7. Base clock and branch clock overview

Base clock	Branch clock name	Parts of the device clocked by this branch clock	Remark
BASE_SAFE_CLK	CLK_SAFE	watchdog timer	[1]
BASE_SYS_CLK	CLK_SYS_CPU	ARM968E-S and TCMs	
	CLK_SYS_SYS	AHB bus infrastructure	
	CLK_SYS_PCRSS	AHB side of bridge in PCRSS	
	CLK_SYS_FMC	Flash Memory Controller	
	CLK_SYS_RAM0	Embedded SRAM Controller 0 (32 kB)	
	CLK_SYS_RAM1	Embedded SRAM Controller 1 (16 kB)	
	CLK_SYS_SMC	External Static Memory Controller	
	CLK_SYS_GESS	General Subsystem	
	CLK_SYS_VIC	Vectored Interrupt Controller	
	CLK_SYS_PESS	Peripheral Subsystem	[2] [4]
	CLK_SYS_GPIO0	GPIO bank 0	
	CLK_SYS_GPIO1	GPIO bank 1	
	CLK_SYS_GPIO2	GPIO bank 2	
	CLK_SYS_GPIO3	GPIO bank 3	
	CLK_SYS_IVNSS_A	AHB side of bridge of IVNSS	
BASE_PCR_CLK	CLK_PCR_SLOW	PCRSS, CGU, RGU and PMU logic clock	[1], [3]
BASE_IVNSS_CLK	CLK_IVNSS_APB	APB side of the IVNSS	
	CLK_IVNSS_CANCA	CAN controller Acceptance Filter	
	CLK_IVNSS_CANC0	CAN channel 0	
	CLK_IVNSS_CANC1	CAN channel 1	
	CLK_IVNSS_LIN0	LIN channel 0	
	CLK_IVNSS_LIN1	LIN channel 1	
BASE_MSCSS_CLK	CLK_MSCSS_APB	APB side of the MSCSS	
	CLK_MSCSS_MTMR0	Timer 0 in the MSCSS	
	CLK_MSCSS_MTMR1	Timer 1 in the MSCSS	
	CLK_MSCSS_PWM0	PWM 0	
	CLK_MSCSS_PWM1	PWM 0	
	CLK_MSCSS_PWM2	PWM 0	
	CLK_MSCSS_PWM3	PWM 0	
	CLK_MSCSS_ADC1_APB	APB side of ADC 1	
	CLK_MSCSS_ADC2_APB	APB side of ADC 2	

8.1.2 Description

After reset flash initialization is started, which takes t_{init} time, see Section 12. During this initialization flash access is not possible and AHB transfers to flash are stalled, blocking the AHB bus.

During flash initialization the index sector is read to identify the status of the JTAG access protection and sector security. If JTAG access protection is active the flash is not accessible via JTAG. ARM debug facilities are disabled to protect the flash memory contents against unwanted reading out externally. If sector security is active only the concerned sections are read.

Flash can be read synchronously or asynchronously to the system clock. In synchronous operation the flash goes into standby after returning the read data. Started reads cannot be stopped, and speculative reading and dual buffering are therefore not supported.

With asynchronous reading, transfer of the address to the flash and of read data from the flash is done asynchronously, giving the fastest possible response time. Started reads can be stopped, so speculative reading and dual buffering are supported.

Buffering is offered because the flash has a 128-bit wide data interface while the AHB interface has only 32 bits. With buffering a buffer line holds the complete 128-bit flash word, from which four words can be read. Without buffering every AHB data port read starts a flash read. A flash read is a slow process compared to the minimum AHB cycle time, so with buffering the average read time is reduced. This can improve system performance.

With single buffering the most recently read flash word remains available until the next flash read. When an AHB data-port read transfer requires data from the same flash word as the previous read transfer, no new flash read is done and the read data is given without wait cycles.

When an AHB data-port read transfer requires data from a different flash word to that involved in the previous read transfer, a new flash read is done and wait states are given until the new read data is available.

With dual buffering a secondary buffer line is used, the output of the flash being considered as the primary buffer. On a primary buffer hit data can be copied to the secondary buffer line, which allows the flash to start a speculative read of the next flash word.

Both buffer lines are invalidated after:

- Initialization
- Configuration-register access
- Data-latch reading
- Index-sector reading

The modes of operation are listed in Table 8.

Table 9. Flash sector overview …continued

Sector number	Sector size (kB)	Sector base address
11	64	0004 0000h
12	64	0005 0000h
13	64	0006 0000h
14	64	0007 0000h
15[1]	64	0008 0000h
16[1]	64	0009 0000h
17[1]	64	000A 0000h
18[1]	64	000B 0000h

[1] Availability of sector 15 to sector 18 depends on device type, see Section 4 “Ordering information”.

The index sector is a special sector in which the JTAG access protection and sector security are located. The address space becomes visible by setting the FS_ISS bit and overlaps the regular flash sector’s address space.

Note that the index sector cannot be erased, and that access to it has to be performed via code outside the flash.

8.1.6 Flash bridge wait-states

To eliminate the delay associated with synchronizing flash read data, a predefined number of wait-states must be programmed. These depend on flash memory response time and system clock period. The minimum wait-states value can be calculated with the following formulas:

Synchronous reading:

$$WST > \frac{t_{acc(clk)}}{t_{t_{tclk(sys)}}} - 1 \quad (1)$$

Asynchronous reading:

$$WST > \frac{t_{acc(addr)}}{t_{tclk(sys)}} - 1 \quad (2)$$

Remark: If the programmed number of wait-states is more than three, flash data reading cannot be performed at full speed (i.e., with zero wait-states at the AHB bus) if speculative reading is active.

8.2 External static memory controller

8.2.1 Overview

The LPC2917/19 contains an external Static Memory Controller (SMC) which provides an interface for external (off-chip) memory devices.

Key features are:

- Supports static memory-mapped devices including RAM, ROM, flash, burst ROM and external I/O devices

8.2.3 External static-memory controller pin description

The external static-memory controller module in the LPC2917/19 has the following pins, which are combined with other functions on the port pins of the LPC2917/19. Table 12 shows the external memory controller pins.

Table 12. External memory controller pins

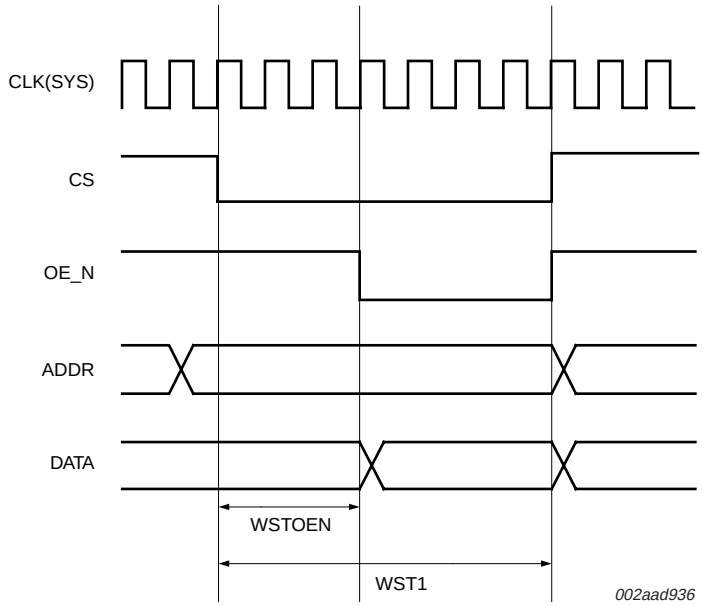
Symbol	Direction	Description
EXTBUS CSx	OUT	memory-bank x select, x runs from 0 to 7
EXTBUS BLSy	OUT	byte-lane select input y, y runs from 0 to 3
EXTBUS WE_N	OUT	write enable (active LOW)
EXTBUS OE_N	OUT	output enable (active LOW)
EXTBUS A[23:0]	OUT	address bus
EXTBUS D[31:0]	IN/OUT	data bus

8.2.4 External static-memory controller clock description

The External Static-Memory Controller is clocked by CLK_SYS_SMC, see Section 7.2.2.

8.2.5 External memory timing diagrams

A timing diagram for reading from external memory is shown in Figure 4. The relationship between the wait-state settings is indicated with arrows.



WSTOEN = 3, WST1 = 7

Fig 4. Reading from external memory

A timing diagram for writing to external memory is shown In Figure 5. The relationship between wait-state settings is indicated with arrows.

8.4.3 Timer

8.4.3.1 Overview

The LPC2917/19 contains six identical timers: four in the peripheral subsystem and two in the Modulation and Sampling Control SubSystem (MSCSS) located at different peripheral base addresses. This section describes the four timers in the peripheral subsystem. Each timer has four capture inputs and/or match outputs. Connection to device pins depends on the configuration programmed into the port function-select registers. The two timers located in the MSCSS have no external capture or match pins, but the memory map is identical, see Section 8.7.7. One of these timers has an external input for a pause function.

The key features are:

- 32-bit timer/counter with programmable 32-bit prescaler
- Up to four 32-bit capture channels per timer. These take a snapshot of the timer value when an external signal connected to the TIMERx CAPn input changes state. A capture event may also optionally generate an interrupt
- Four 32-bit match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Pause input pin (MSCSS timers only)

8.4.3.2 Description

The timers are designed to count cycles of the clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. They also include capture inputs to trap the timer value when an input signal changes state, optionally generating an interrupt. The core function of the timers consists of a 32 bit ‘prescale counter’ triggering the 32 bit ‘timer counter’. Both counters run on clock CLK_TMRx (x runs from 0 to 3) and all time references are related to the period of this clock. Note that each timer has its individual clock source within the Peripheral SubSystem. In the Modulation and Sampling SubSystem each timer also has its own individual clock source. See section Section 8.8.6 for information on generation of these clocks.

8.4.3.3 Pin description

The four timers in the peripheral subsystem of the LPC2917/19 have the pins described below. The two timers in the modulation and sampling subsystem have no external pins except for the pause pin on MSCSS timer 1. See Section 8.7.7 for a description of these

timers and their associated pins. The timer pins are combined with other functions on the port pins of the LPC2917/19, see Section 8.3.3. Table Table 14 shows the timer pins (x runs from 0 to 3).

Table 14. Timer pins

Symbol	Direction	Description
TIMERx CAP[0]	IN	TIMER x capture input 0
TIMERx CAP[1]	IN	TIMER x capture input 1
TIMERx CAP[2]	IN	TIMER x capture input 2
TIMERx CAP[3]	IN	TIMER x capture input 3
TIMERx MAT[0]	OUT	TIMER x match output 0
TIMERx MAT[1]	OUT	TIMER x match output 1
TIMERx MAT[2]	OUT	TIMER x match output 2
TIMERx MAT[3]	OUT	TIMER x match output 3

8.4.3.4 Timer clock description

The timer modules are clocked by two different clocks; CLK_SYS_PESS and CLK_TMRx (x = 0-3), see Section 7.2.2. Note that each timer has its own CLK_TMRx branch clock for power management. The frequency of all these clocks is identical as they are derived from the same base clock BASE_CLK_TMR. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_TMRx.

8.4.4 UARTs

8.4.4.1 Overview

The LPC2917/19 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs
- Register locations conform to 550 industry standard
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes
- Built-in baud rate generator

8.4.4.2 Description

The UART is commonly used to implement a serial interface such as RS232. The LPC2917/19 contains two industry-standard 550 UARTs with 16-byte transmit and receive FIFOs, but they can also be put into 450 mode without FIFOs.

8.4.4.3 UART pin description

The two UARTs in the LPC2917/19 have the following pins. The UART pins are combined with other functions on the port pins of the LPC2917/19. Table 15 shows the UART pins (x runs from 0 to 1).

Table 15. UART pins

Symbol	Direction	Description
UARTx TXD	OUT	UART channel x transmit data output
UARTx RXD	IN	UART channel x receive data input

Depending on the operating mode selected, the SPI_CS_OUT outputs operate as an active-HIGH frame synchronization output for Texas Instruments synchronous serial frame format or an active-LOW chip select for SPI.

Each data frame is between four and 16 bits long, depending on the size of words programmed, and is transmitted starting with the MSB.

There are two basic frame types that can be selected:

- Texas Instruments synchronous serial
- Motorola Serial Peripheral Interface

8.4.5.3 Modes of operation

The SPI module can operate in:

- Master mode:
  - Normal transmission mode
  - Sequential slave mode
- Slave mode

8.4.5.4 SPI pin description

The three SPI modules in the LPC2917/19 have the pins listed below. The pins are combined with other functions on the port pins of the LPC2917/19, see Section 8.3.3. Table 16 shows the SPI pins (x runs from 0 to 2; y runs from 0 to 3).

Table 16. SPI pins

Symbol	Direction	Description
SPIx SCSy	IN/OUT	SPIx chip select[1][2]
SPIx SCK	IN/OUT	SPIx clock[1]
SPIx SDI	IN	SPIx data input
SPIx SDO	OUT	SPIx data output

[1] Direction of SPIx SCS and SPIx SCK pins depends on master or slave mode. These pins are output in master mode, input in slave mode.

[2] In slave mode there is only one chip select input pin, SPIx SCS0. The other chip selects have no function in slave mode.

8.4.5.5 SPI clock description

The SPI modules are clocked by two different clocks; CLK_SYS_PESS and CLK_SPIx (x = 0-2), see Section 7.2.2. Note that each SPI has its own CLK_SPIx branch clock for power management. The frequency of all clocks CLK_SPIx is identical as they are derived from the same base clock BASE_CLK_SPI. The register interface towards the system bus is clocked by CLK_SYS_PESS. The serial-clock rate divisor is clocked by CLK_SPIx.

The SPI clock frequency can be controlled by the CGU. In master mode the SPI clock frequency (CLK_SPIx) must be set to at least twice the SPI serial clock rate on the interface. In slave mode CLK_SPIx must be set to four times the SPI serial clock rate on the interface.

control. Several other trigger possibilities are provided for the ADCs (external, cascaded or following a PWM). The capture inputs of both timers can also be used to capture the start pulse of the ADCs.

The PWMs can be used to generate waveforms in which the frequency, duty cycle and rising and falling edges can be controlled very precisely. Capture inputs are provided to measure event phases compared to the main counter. Depending on the applications, these inputs can be connected to digital sensor motor outputs or digital external signals. Interrupt signals are generated on several events to closely interact with the CPU.

The ADCs can be used for any application needing accurate digitized data from analog sources. To support applications like motor control, a mechanism to synchronize several PWMs and ADCs is available (sync_in and sync_out).

Note that the PWMs run on the PWM clock and the ADCs on the ADC clock, see Section 8.8.4.

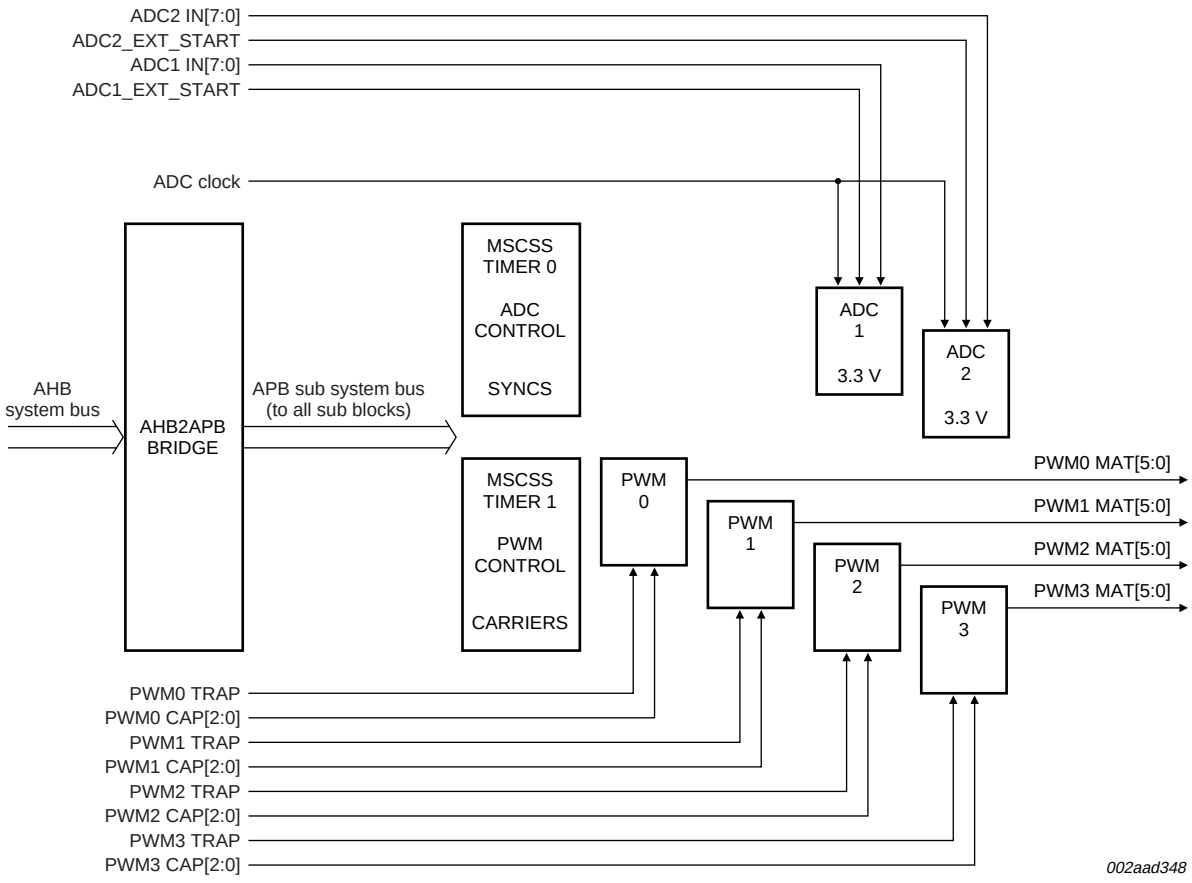


Fig 7. Modulation and sampling control subsystem block diagram

8.7.2.1 Synchronization and trigger features of the MSCSS

The MSCSS contains two internal timers to generate synchronization and carrier pulses for the ADCs and PWMs. Figure 8 shows how the timers are connected to the ADC and PWM modules.

- CLK_SYS_MSCSS_A clocks the AHB side of the AHB-to-APB bus bridge
- CLK_MSCSS_APB clocks the subsystem APB bus
- CLK_MSCSS_MTMR0/1 clocks the timers
- CLK_MSCSS_PWM0..3 clocks the PWMs.

Each ADC has two clock areas; a APB part clocked by CLK_MSCSS_ADCx_APB (x = 1 or 2) and a control part for the analog section clocked by CLK_ADCx = 1 or 2), see Section 7.2.2.

All clocks are derived from the BASE_MSCSS_CLK, except for CLK_SYS_MSCSS_A which is derived form BASE_SYS_CLK, and the CLK_ADCx clocks which are derived from BASE_CLK_ADC. If specific PWM or ADC modules are not used their corresponding clocks can be switched off.

8.7.5 Analog-to-digital converter

8.7.5.1 Overview

The MSCSS in the LPC2917/19 includes two 10-bit successive-approximation analog-to-digital converters.

The key features of the ADC interface module are:

- ADC1 and ADC2: Eight analog inputs; time-multiplexed; measurement range up to 3.3 V
- External reference-level inputs
- 400 ksample/s at 10-bit resolution up to 1500 ksample/s at 2-bit resolution
- Programmable resolution from 2-bit to 10-bit
- Single analog-to-digital conversion scan mode and continuous analog-to-digital conversion scan mode
- Optional conversion on transition on external start input, timer capture/match signal, PWM_sync or ‘previous’ ADC
- Converted digital values are stored in a register for each channel
- Optional compare condition to generate a ‘less than’ or an ‘equal to or greater than’ compare-value indication for each channel
- Power-down mode

8.7.5.2 Description

The ADC block diagram, Figure 9, shows the basic architecture of each ADC. The ADC functionality is divided into two major parts; one part running on the MSCSS Subsystem clock, the other on the ADC clock. This split into two clock domains affects the behavior from a system-level perspective. The actual analog-to-digital conversions take place in the ADC clock domain, but system control takes place in the system clock domain.

A mechanism is provided to modify configuration of the ADC and control the moment at which the updated configuration is transferred to the ADC domain.

The ADC clock is limited to 4.5 MHz maximum frequency and should always be lower than or equal to the system clock frequency. To meet this constraint or to select the desired lower sampling frequency the clock generation unit provides a programmable fractional

system-clock divider dedicated to the ADC clock. Conversion rate is determined by the ADC clock frequency divided by the number of resolution bits plus one. Accessing ADC registers requires an enabled ADC clock, which is controllable via the clock generation unit, see Section 8.8.4.

Each ADC has four start inputs. Note that start 0 and start 2 are captured in the system clock domain while start 1 and start 3 are captured in the ADC domain. The start inputs are connected at MSCSS level, see Section 8.7.2.1 for details.

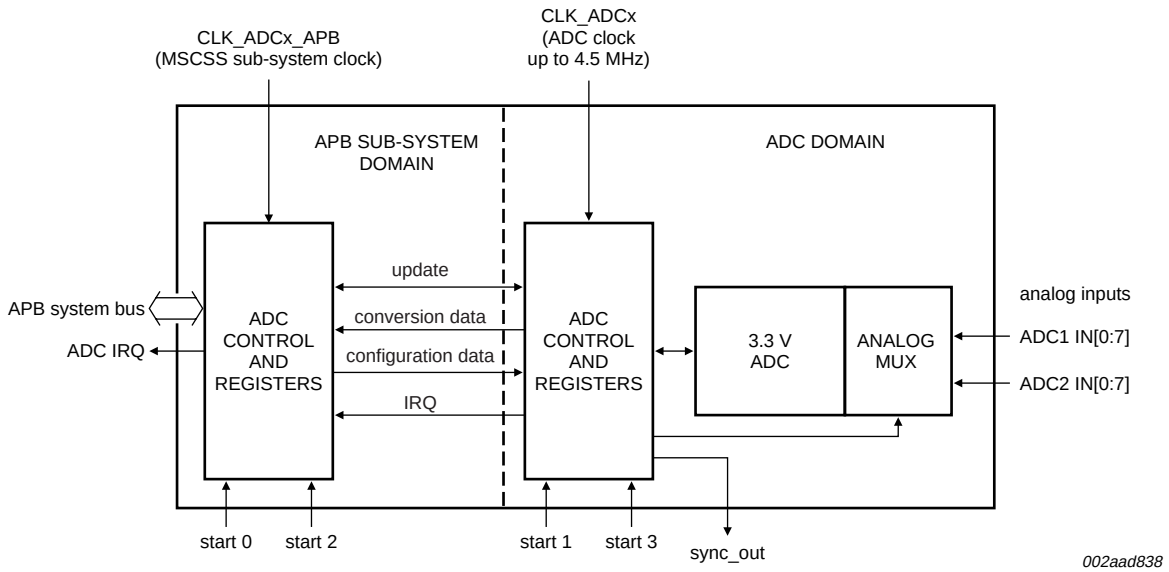


Fig 9. ADC block diagram

8.7.5.3 ADC pin description

The two ADC modules in the MSCSS have the pins described below. The ADCx input pins are combined with other functions on the port pins of the LPC2917/19. The VREFN and VREFP pins are common for both ADCs. Table 20 shows the ADC pins.

Table 20. Analog to digital converter pins

Symbol	Direction	Description
ADCn IN[7:0]	IN	analog input for ADCn, channel 7 to channel 0 (n is 1 or 2)
ADCn_EXT_START	IN	ADC external start-trigger input (n is 1 or 2)
VREFN	IN	ADC LOW reference level
VREFP	IN	ADC HIGH reference level

8.7.5.4 ADC clock description

The ADC modules are clocked from two different sources; CLK_MSCSS_ADCx_APB and CLK_ADCx (x = 1 or 2), see Section 7.2.2. Note that each ADC has its own CLK_ADCx and CLK_MSCSS_ADCx_APB branch clocks for power management. If an ADC is unused both its CLK_MSCSS_ADCx_APB and CLK_ADCx can be switched off.

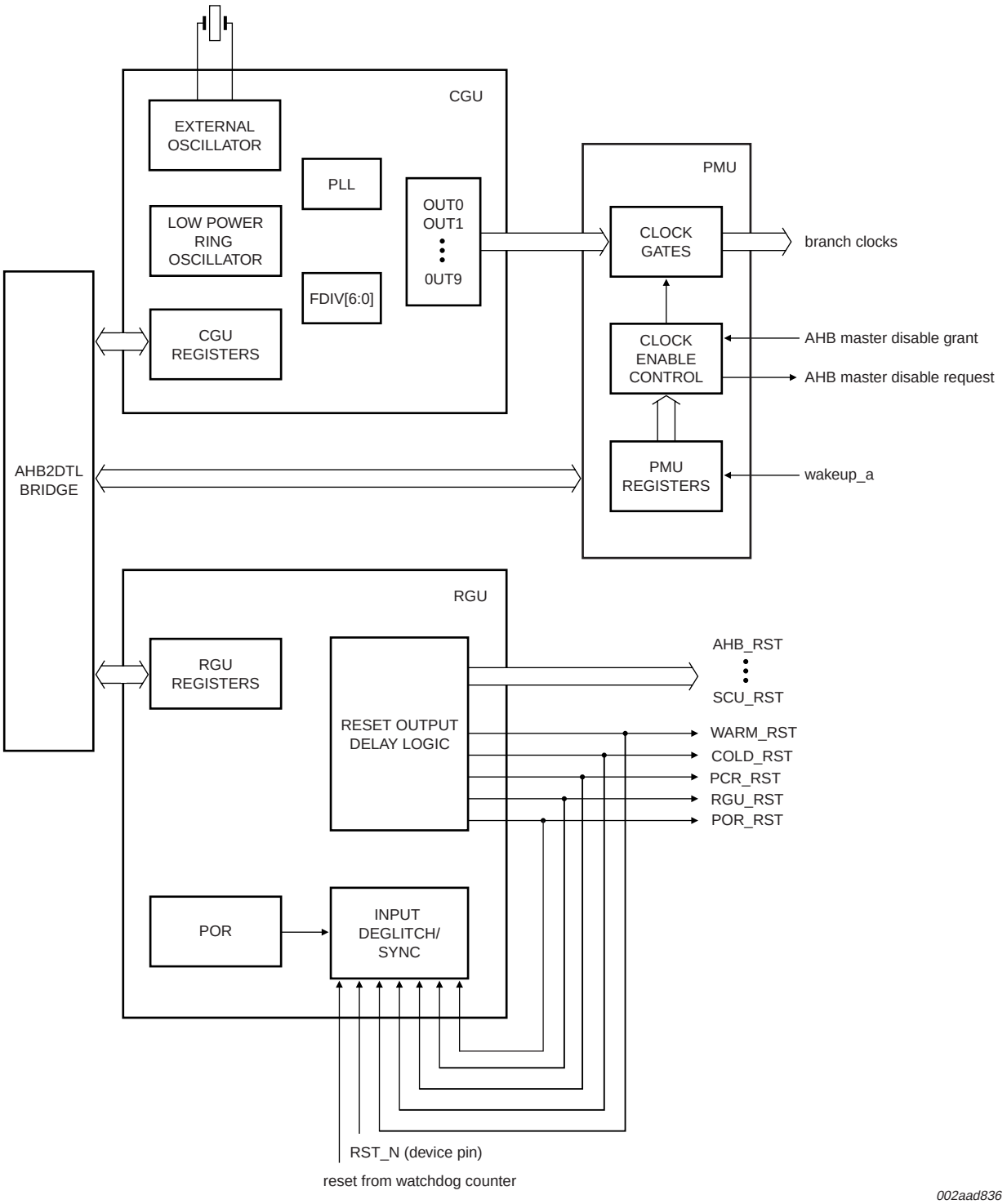


Fig 11. PCRSS block diagram

For generation of these base clocks, the CGU consists of primary and secondary clock generators and one output generator for each base clock.

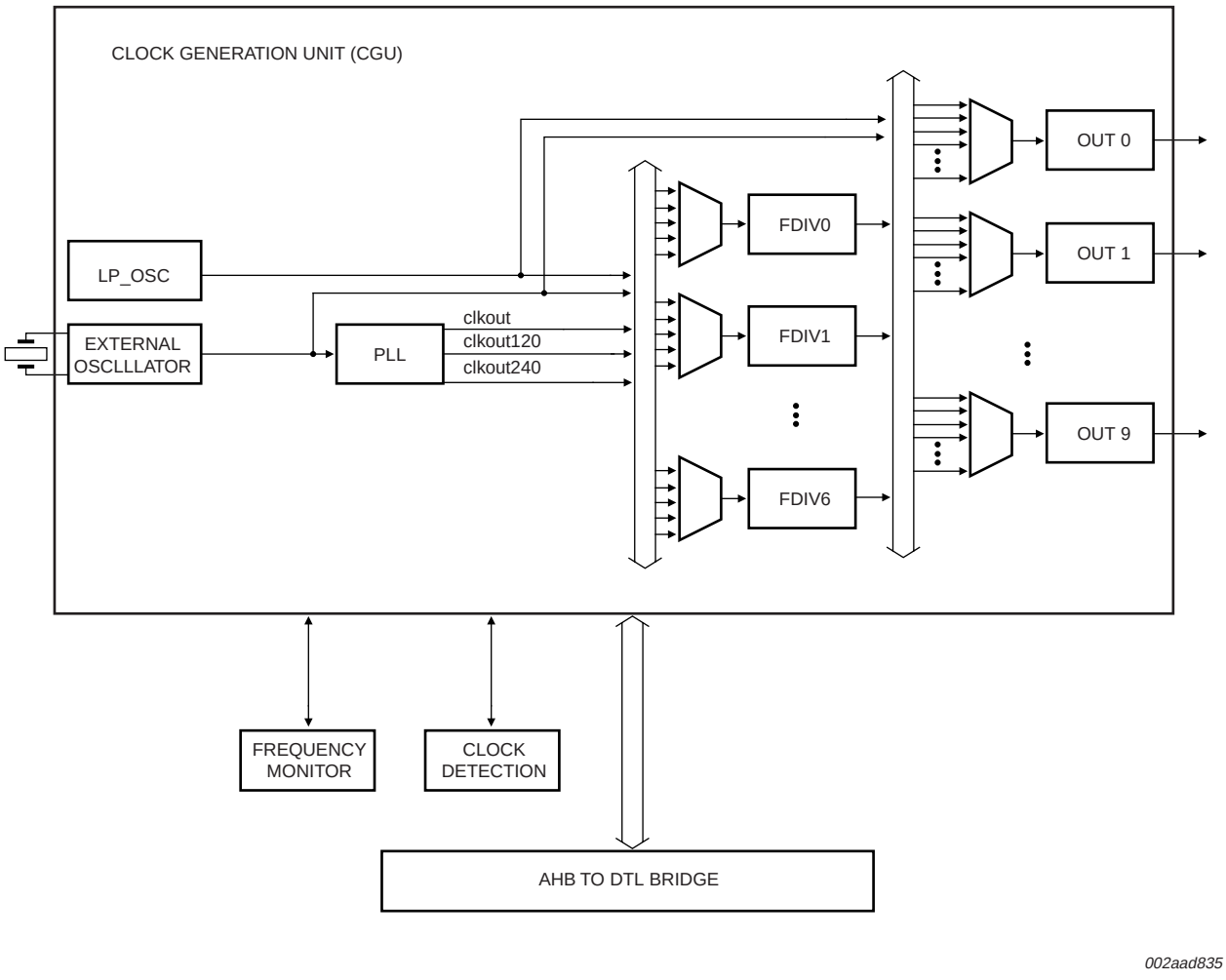


Fig 12. Block diagram of the CGU

There are two primary clock generators: a low-power ring oscillator (LP_OSC) and a crystal oscillator. See Figure 12.

LP_OSC is the source for the BASE_PCR_CLK that clocks the CGU itself and for BASE_SAFE_CLK that clocks a minimum of other logic in the device (like the watchdog timer). To prevent the device from losing its clock source LP_OSC cannot be put into power-down. The crystal oscillator can be used as source for high-frequency clocks or as an external clock input if a crystal is not connected.

Secondary clock generators are a PLL and seven fractional dividers (FDIV0..6). The PLL has three clock outputs: normal, 120° phase-shifted and 240° phase-shifted.

Configuration of the CGU: For every output generator - generating the base clocks - a choice can be made from the primary and secondary clock generators according to Figure 13.

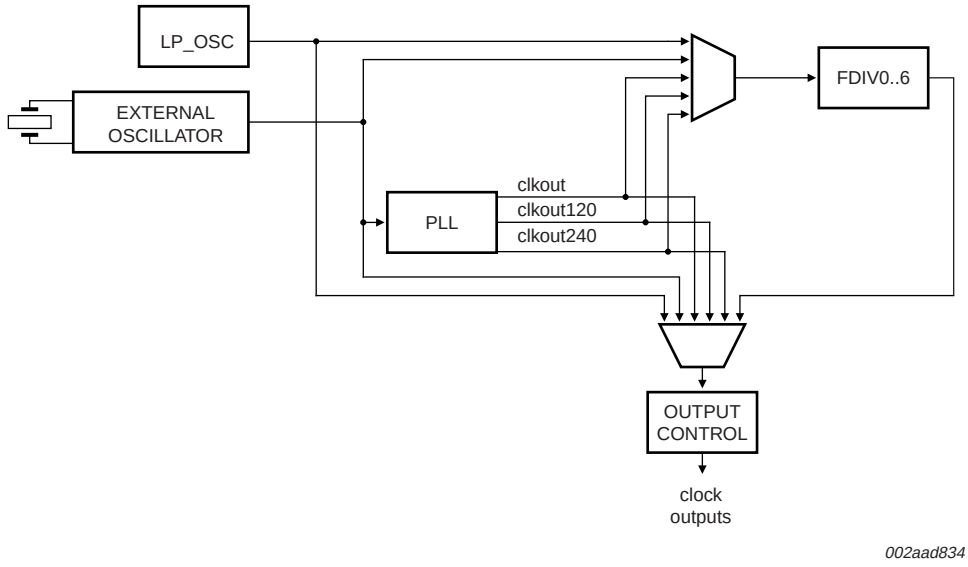


Fig 13. Structure of the clock generation scheme

Any output generator (except for BASE_SAFE_CLK and BASE_PCR_CLK) can be connected to either a fractional divider (FDIV0..6) or to one of the outputs of the PLL or to LP_OSC/crystal oscillator directly. BASE_SAFE_CLK and BASE_PCR_CLK can use only LP_OSC as source.

The fractional dividers can be connected to one of the outputs of the PLL or directly to LP_OSC/crystal Oscillator.

The PLL can be connected to the crystal oscillator.

In this way every output generating the base clocks can be configured to get the required clock. Multiple output generators can be connected to the same primary or secondary clock source, and multiple secondary clock sources can be connected to the same PLL output or primary clock source.

Invalid selections/programming - connecting the PLL to an FDIV or to one of the PLL outputs itself for example - will be blocked by hardware. The control register will not be written, the previous value will be kept, although all other fields will be written with new data. This prevents clocks being blocked by incorrect programming.

Default Clock Sources: Every secondary clock generator or output generator is connected to LP_OSC at reset. In this way the device runs at a low frequency after reset. It is recommended to switch BASE_SYS_CLK to a high-frequency clock generator as (one of) the first step(s) in the boot code after verifying that the high-frequency clock generator is running.

Clock Activity Detection: Clocks that are inactive are automatically regarded as invalid, and values of ‘CLK_SEL’ that would select those clocks are masked and not written to the control registers. This is accomplished by adding a clock detector to every clock generator. The RDET register keeps track of which clocks are active and inactive, and the

Triple output phases: For applications that require multiple clock phases two additional clock outputs can be enabled by setting register P23EN to logic 1, thus giving three clocks with a 120° phase difference. In this mode all three clocks generated by the analog section are sent to the output dividers. When the PLL has not yet achieved lock the second and third phase output dividers run unsynchronized, which means that the phase relation of the output clocks is unknown. When the PLL LOCK register is set the second and third phase of the output dividers are synchronized to the main output clock CLKOUT PLL, thus giving three clocks with a 120° phase difference.

Direct output mode: In normal operating mode (with DIRECT set to logic 0) the CCO clock is divided by 2, 4, 8 or 16 depending on the value on the PSEL[1:0] input, giving an output clock with a 50 % duty cycle. If a higher output frequency is needed the CCO clock can be sent directly to the output by setting DIRECT to logic 1. Since the CCO does not directly generate a 50 % duty cycle clock, the output clock duty cycle in this mode can deviate from 50 %.

Power-down control: A Power-down mode has been incorporated to reduce power consumption when the PLL clock is not needed. This is enabled by setting the PD control register bit. In this mode the analog section of the PLL is turned off, the oscillator and the phase-frequency detector are stopped and the dividers enter a reset state. While in Power-down mode the LOCK output is low, indicating that the PLL is not in lock. When Power-down mode is terminated by clearing the PD control-register bit the PLL resumes normal operation, and makes the LOCK signal high once it has regained lock on the input clock.

8.8.4.4 CGU pin description

The CGU module in the LPC2917/19 has the pins listed in Table 24 below.

Table 24. CGU pins

Symbol	Direction	Description
XOUT_OSC	OUT	oscillator crystal output
XIN_OSC	IN	oscillator crystal input or external clock input

8.8.5 Reset Generation Unit (RGU)

8.8.5.1 Overview

The key features of the Reset Generation Unit (RGU) are:

- Reset controlled individually per subsystem
- Automatic reset stretching and release
- Monitor function to trace resets back to source
- Register write-protection mechanism to prevent unintentional resets

8.8.5.2 Description

The RGU controls all internal resets.

Each reset output is defined as a (combination of) reset input sources including the external reset input pins and internal power-on reset, see Table 25. The first five resets listed in this table form a sort of cascade to provide the multiple levels of impact that a reset may have. The combined input sources are logically OR-ed together so that activating any of the listed reset sources causes the output to go active.

Table 28. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
ESD						
V_{esd}	electrostatic discharge voltage	on all pins				
		human body model	[7]	–2000	+2000	V
		machine model	[8]	–200	+200	V
		charged device model		–500	+500	V
		on corner pins				
		charged device model		–750	+750	V

[1] Based on package heat transfer, not device power consumption.

[2] Peak current must be limited at 25 times average current.

[3] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[4] Only when $V_{DD(IO)}$ is present.

[5] Note that pull-up should be off. With pull-up do not exceed 3.6 V.

[6] In accordance with IEC 60747-1. An alternative definition of the virtual junction temperature is: $T_{vj} = T_{amb} + P_{tot} \times R_{th(j-a)}$ where $R_{th(j-a)}$ is a fixed value; see Section 10. The rating for T_{vj} limits the allowable combinations of power dissipation and ambient temperature.

[7] Human-body model: discharging a 100 pF capacitor via a 10 kΩ series resistor.

[8] Machine model: discharging a 200 pF capacitor via a 0.75 μH series inductance and 10 Ω resistor.

[9] 112 mA per $V_{DD(IO)}$ or $V_{SS(IO)}$ should not be exceeded.

10. Thermal characteristics

Table 29. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		package;		
		LQFP144	62	K/W

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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