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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM968E-S
Core Size	32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	108
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	88K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 1.89V
Data Converters	A/D 16x10b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2919fbd144-01

- Allows minimization of system operating power consumption in any configuration.
- Standard ARM test and debug interface with real-time in-circuit emulator.
- Boundary-scan test supported.
- Dual power supply:
  - CPU operating voltage: 1.8 V ± 5 %.
  - I/O operating voltage: 2.7 V to 3.6 V; inputs tolerant up to 5.5 V.
- 144-pin LQFP package.
- –40 °C to 85 °C ambient operating temperature range.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2917FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2919FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Part options

Type number	Flash memory	RAM	SMC	LIN 2.0	Package
LPC2917FBD144	512 kB	80 kB (including TCMs)	32-bit	2	LQFP144
LPC2919FBD144	768 kB	80 kB (including TCMs)	32-bit	2	LQFP144

Table 3. LQFP144 pin assignment *...continued*

Pin name	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P1[13]/EI3/WE_N	51	GPIO 1, pin 13	EXTINT3	-	EXTBUS WE_N
P1[12]/EI2/OE_N	52	GPIO 1, pin 12	EXTINT2	-	EXTBUS OE_N
$V_{DD(IO)}$	53	3.3 V power supply for I/O			
P2[2]/MAT2[2]/TRAP1/D10	54	GPIO 2, pin 2	TIMER2 MAT2	PWM TRAP1	EXTBUS D10
P2[3]/MAT2[3]/TRAP0/D11	55	GPIO 2, pin 3	TIMER2 MAT3	PWM TRAP0	EXTBUS D11
P1[11]/SCK1/CS3	56	GPIO 1, pin 11	SPI1 SCK	-	EXTBUS CS3
P1[10]/SDI1/CS2	57	GPIO 1, pin 10	SPI1 SDI	-	EXTBUS CS2
P3[12]/SCS1[0]/EI4	58	GPIO 3, pin 12	SPI1 SCS0	EXTINT4	-
$V_{SS(CORE)}$	59	ground for digital core			
$V_{DD(CORE)}$	60	1.8 V power supply for digital core			
P3[13]/SDO1/EI5	61	GPIO 3, pin 13	SPI1 SDO	EXTINT5	-
P2[4]/MAT1[0]/EI0/D12	62	GPIO 2, pin 4	TIMER1 MAT0	EXTINT0	EXTBUS D12
P2[5]/MAT1[1]/EI1/D13	63	GPIO 2, pin 5	TIMER1 MAT1	EXTINT1	EXTBUS D13
P1[9]/SDO1/RXDL1/CS1	64	GPIO 1, pin 9	SPI1 SDO	LIN1 RXDL	EXTBUS CS1
$V_{SS(IO)}$	65	ground for I/O			
P1[8]/SCS1[0]/TXDL1/CS0	66	GPIO 1, pin 8	SPI1 SCS0	LIN1 TXDL	EXTBUS CS0
P1[7]/SCS1[3]/RXD1/A7	67	GPIO 1, pin 7	SPI1 SCS3	UART1 RXD	EXTBUS A7
P1[6]/SCS1[2]/TXD1/A6	68	GPIO 1, pin 6	SPI1 SCS2	UART1 TXD	EXTBUS A6
P2[6]/MAT1[2]/EI2/D14	69	GPIO 2, pin 6	TIMER1 MAT2	EXTINT2	EXTBUS D14
P1[5]/SCS1[1]/PMAT3[5]/A5	70	GPIO 1, pin 5	SPI1 SCS1	PWM3 MAT5	EXTBUS A5
P1[4]/SCS2[2]/PMAT3[4]/A4	71	GPIO 1, pin 4	SPI2 SCS2	PWM3 MAT4	EXTBUS A4
TRST_N	72	IEEE 1149.1 test reset NOT; active LOW; pulled up internally			
RST_N	73	asynchronous device reset; active LOW; pulled up internally			
$V_{SS(OSC)}$	74	ground for oscillator			
XOUT_OSC	75	crystal out for oscillator			
XIN_OSC	76	crystal in for oscillator			
$V_{DD(OSC)}$	77	1.8 V supply for oscillator			
$V_{SS(PLL)}$	78	ground for PLL			
P2[7]/MAT1[3]/EI3/D15	79	GPIO 2, pin 7	TIMER1 MAT3	EXTINT3	EXTBUS D15
P3[14]/SDI1/EI6/TXDC0	80	GPIO 3, pin 14	SPI1 SDI	EXTINT6	CAN0 TXDC
P3[15]/SCK1/EI7/RXDC0	81	GPIO 3, pin 15	SPI1 SCK	EXTINT7	CAN0 RXDC
$V_{DD(IO)}$	82	3.3 V power supply for I/O			
P2[8]/PMAT0[0]/SCS0[2]	83	GPIO 2, pin 8	-	PWM0 MAT0	SPI0 SCS2
P2[9]/PMAT0[1]/SCS0[1]	84	GPIO 2, pin 9	-	PWM0 MAT1	SPI0 SCS1
P1[3]/SCS2[1]/PMAT3[3]/A3	85	GPIO 1, pin 3	SPI2 SCS1	PWM3 MAT3	EXTBUS A3
P1[2]/SCS2[3]/PMAT3[2]/A2	86	GPIO 1, pin 2	SPI2 SCS3	PWM3 MAT2	EXTBUS A2
P1[1]/EI1/PMAT3[1]/A1	87	GPIO 1, pin 1	EXTINT1	PWM3 MAT1	EXTBUS A1
$V_{SS(CORE)}$	88	ground for digital core			
$V_{DD(CORE)}$	89	1.8 V power supply for digital core			
P1[0]/EI0/PMAT3[0]/A0	90	GPIO 1, pin 0	EXTINT0	PWM3 MAT0	EXTBUS A0

7.1.3 IEEE 1149.1 interface pins (JTAG boundary-scan test)

The LPC2917/19 contains boundary-scan test logic according to IEEE 1149.1, also referred to in this document as JTAG. The boundary-scan test pins can be used to connect a debugger probe for the embedded ARM processor. Pin JTAGSEL selects between boundary-scan mode and debug mode. Table 5 shows the boundary- scan test pins.

Table 5. IEEE 1149.1 boundary-scan test and debug interface

Symbol	Description
JTAGSEL	TAP controller select input. LOW-level selects ARM debug mode and HIGH-level selects boundary scan and flash programming; pulled up internally
TRST_N	test reset input; pulled up internally (active LOW)
TMS	test mode select input; pulled up internally
TDI	test data input, pulled up internally
TDO	test data output
TCK	test clock input

7.1.4 Power supply pins description

Table 6 shows the power supply pins.

Table 6. Power supplies

Symbol	Description
$V_{DD(CORE)}$	digital core supply 1.8 V
$V_{SS(CORE)}$	digital core ground (digital core, ADC1/2)
$V_{DD(IO)}$	I/O pins supply 3.3 V
$V_{SS(IO)}$	I/O pins ground
$V_{DD(OSC)}$	oscillator and PLL supply
$V_{SS(OSC)}$	oscillator ground
$V_{DDA(ADC3V3)}$	ADC1/2 3.3 V supply
$V_{SS(PLL)}$	PLL ground

7.2 Clocking strategy

7.2.1 Clock architecture

The LPC2917/19 contains several different internal clock areas. Peripherals like Timers, SPI, UART, CAN and LIN have their own individual clock sources called Base Clocks. All base clocks are generated by the Clock Generation Unit (CGU). They may be unrelated in frequency and phase and can have different clock sources within the CGU.

The system clock for the CPU and AHB Bus infrastructure has its own base clock. This means most peripherals are clocked independently from the system clock. See Figure 3 for an overview of the clock areas within the device.

Within each clock area there may be multiple branch clocks, which offers very flexible control for power-management purposes. All branch clocks are outputs of the Power Management Unit (PMU) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase. See Section 8.8 for more details of clock and power control within the device.

8.1.2 Description

After reset flash initialization is started, which takes t_{init} time, see Section 12. During this initialization flash access is not possible and AHB transfers to flash are stalled, blocking the AHB bus.

During flash initialization the index sector is read to identify the status of the JTAG access protection and sector security. If JTAG access protection is active the flash is not accessible via JTAG. ARM debug facilities are disabled to protect the flash memory contents against unwanted reading out externally. If sector security is active only the concerned sections are read.

Flash can be read synchronously or asynchronously to the system clock. In synchronous operation the flash goes into standby after returning the read data. Started reads cannot be stopped, and speculative reading and dual buffering are therefore not supported.

With asynchronous reading, transfer of the address to the flash and of read data from the flash is done asynchronously, giving the fastest possible response time. Started reads can be stopped, so speculative reading and dual buffering are supported.

Buffering is offered because the flash has a 128-bit wide data interface while the AHB interface has only 32 bits. With buffering a buffer line holds the complete 128-bit flash word, from which four words can be read. Without buffering every AHB data port read starts a flash read. A flash read is a slow process compared to the minimum AHB cycle time, so with buffering the average read time is reduced. This can improve system performance.

With single buffering the most recently read flash word remains available until the next flash read. When an AHB data-port read transfer requires data from the same flash word as the previous read transfer, no new flash read is done and the read data is given without wait cycles.

When an AHB data-port read transfer requires data from a different flash word to that involved in the previous read transfer, a new flash read is done and wait states are given until the new read data is available.

With dual buffering a secondary buffer line is used, the output of the flash being considered as the primary buffer. On a primary buffer hit data can be copied to the secondary buffer line, which allows the flash to start a speculative read of the next flash word.

Both buffer lines are invalidated after:

- Initialization
- Configuration-register access
- Data-latch reading
- Index-sector reading

The modes of operation are listed in Table 8.

Table 9. Flash sector overview …continued

Sector number	Sector size (kB)	Sector base address
11	64	0004 0000h
12	64	0005 0000h
13	64	0006 0000h
14	64	0007 0000h
15[1]	64	0008 0000h
16[1]	64	0009 0000h
17[1]	64	000A 0000h
18[1]	64	000B 0000h

[1] Availability of sector 15 to sector 18 depends on device type, see Section 4 “Ordering information”.

The index sector is a special sector in which the JTAG access protection and sector security are located. The address space becomes visible by setting the FS_ISS bit and overlaps the regular flash sector’s address space.

Note that the index sector cannot be erased, and that access to it has to be performed via code outside the flash.

8.1.6 Flash bridge wait-states

To eliminate the delay associated with synchronizing flash read data, a predefined number of wait-states must be programmed. These depend on flash memory response time and system clock period. The minimum wait-states value can be calculated with the following formulas:

Synchronous reading:

$$WST > \frac{t_{acc(clk)}}{t_{t_{tclk(sys)}}} - 1 \quad (1)$$

Asynchronous reading:

$$WST > \frac{t_{acc(addr)}}{t_{tclk(sys)}} - 1 \quad (2)$$

Remark: If the programmed number of wait-states is more than three, flash data reading cannot be performed at full speed (i.e., with zero wait-states at the AHB bus) if speculative reading is active.

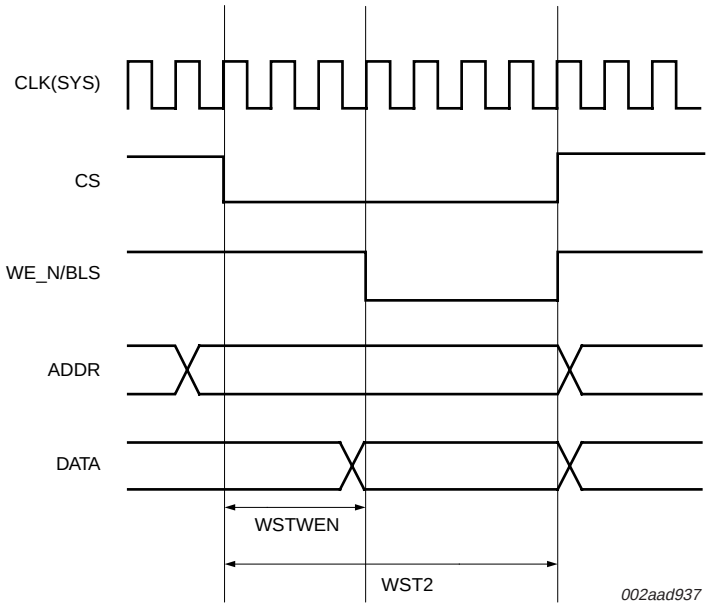
8.2 External static memory controller

8.2.1 Overview

The LPC2917/19 contains an external Static Memory Controller (SMC) which provides an interface for external (off-chip) memory devices.

Key features are:

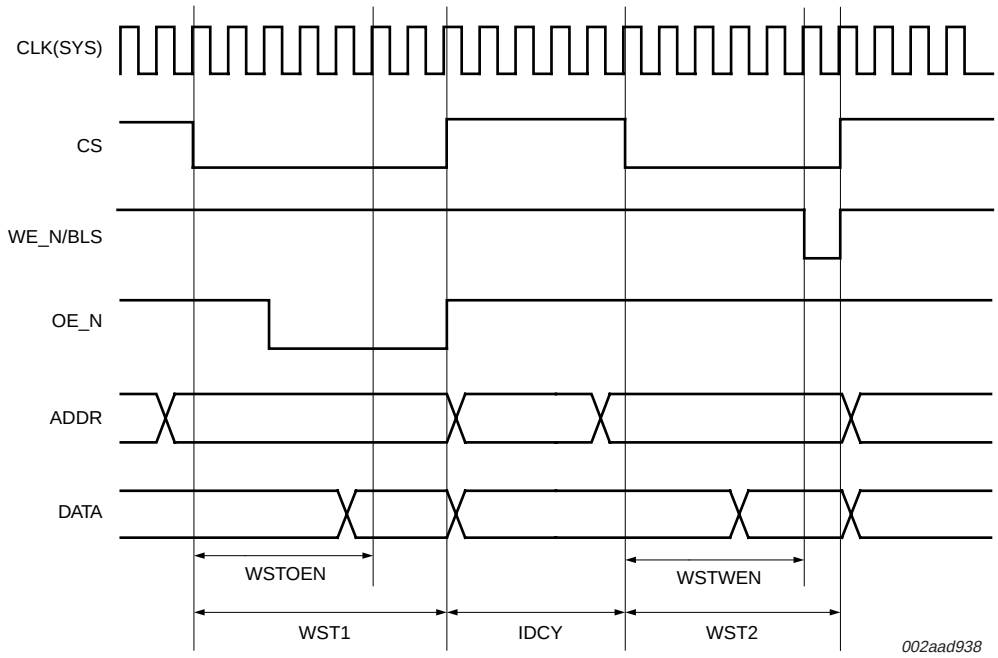
- Supports static memory-mapped devices including RAM, ROM, flash, burst ROM and external I/O devices



WSTWEN = 3, WST2 = 7

Fig 5. Writing to external memory

Usage of the idle/turn-around time (IDCY) is demonstrated In Figure 6. Extra wait states are added between a read and a write cycle in the same external memory device.



WSTOEN = 5, WSTWEN = 5, WST1 = 7, WST2 = 6, IDCY = 5

Fig 6. Reading/writing external memory

Depending on the operating mode selected, the SPI_CS_OUT outputs operate as an active-HIGH frame synchronization output for Texas Instruments synchronous serial frame format or an active-LOW chip select for SPI.

Each data frame is between four and 16 bits long, depending on the size of words programmed, and is transmitted starting with the MSB.

There are two basic frame types that can be selected:

- Texas Instruments synchronous serial
- Motorola Serial Peripheral Interface

8.4.5.3 Modes of operation

The SPI module can operate in:

- Master mode:
  - Normal transmission mode
  - Sequential slave mode
- Slave mode

8.4.5.4 SPI pin description

The three SPI modules in the LPC2917/19 have the pins listed below. The pins are combined with other functions on the port pins of the LPC2917/19, see Section 8.3.3. Table 16 shows the SPI pins (x runs from 0 to 2; y runs from 0 to 3).

Table 16. SPI pins

Symbol	Direction	Description
SPIx SCSy	IN/OUT	SPIx chip select[1][2]
SPIx SCK	IN/OUT	SPIx clock[1]
SPIx SDI	IN	SPIx data input
SPIx SDO	OUT	SPIx data output

[1] Direction of SPIx SCS and SPIx SCK pins depends on master or slave mode. These pins are output in master mode, input in slave mode.

[2] In slave mode there is only one chip select input pin, SPIx SCS0. The other chip selects have no function in slave mode.

8.4.5.5 SPI clock description

The SPI modules are clocked by two different clocks; CLK_SYS_PESS and CLK_SPIx (x = 0-2), see Section 7.2.2. Note that each SPI has its own CLK_SPIx branch clock for power management. The frequency of all clocks CLK_SPIx is identical as they are derived from the same base clock BASE_CLK_SPI. The register interface towards the system bus is clocked by CLK_SYS_PESS. The serial-clock rate divisor is clocked by CLK_SPIx.

The SPI clock frequency can be controlled by the CGU. In master mode the SPI clock frequency (CLK_SPIx) must be set to at least twice the SPI serial clock rate on the interface. In slave mode CLK_SPIx must be set to four times the SPI serial clock rate on the interface.

8.4.6 General-purpose I/O

8.4.6.1 Overview

The LPC2917/19 contains four general-purpose I/O ports located at different peripheral base addresses. In the 144-pin package all four ports are available. All I/O pins are bidirectional, and the direction can be programmed individually. The I/O pad behavior depends on the configuration programmed in the port function-select registers.

The key features are:

- General-purpose parallel inputs and outputs
- Direction control of individual bits
- Synchronized input sampling for stable input-data values
- All I/O defaults to input at reset to avoid any possible bus conflicts

8.4.6.2 Description

The general-purpose I/O provides individual control over each bidirectional port pin. There are two registers to control I/O direction and output level. The inputs are synchronized to achieve stable read-levels.

To generate an open-drain output, set the bit in the output register to the desired value. Use the direction register to control the signal. When set to output, the output driver actively drives the value on the output: when set to input the signal floats and can be pulled up internally or externally.

8.4.6.3 GPIO pin description

The five GPIO ports in the LPC2917/19 have the pins listed below. The GPIO pins are combined with other functions on the port pins of the LPC2917/19. Table 17 shows the GPIO pins.

Table 17. GPIO pins

Symbol	Direction	Description
GPIO0 pin[31:0]	IN/OUT	GPIO port x pins 31 to 0
GPIO1 pin[31:0]	IN/OUT	GPIO port x pins 31 to 0
GPIO2 pin[27:0]	IN/OUT	GPIO port x pins 27 to 0
GPIO3 pin[15:0]	IN/OUT	GPIO port x pins 15 to 0

8.4.6.4 GPIO clock description

The GPIO modules are clocked by several clocks, all of which are derived from BASE_SYS_CLK; CLK_SYS_PESS and CLK_SYS_GPIOx (x = 0-3), see Section 7.2.2. Note that each GPIO has its own CLK__SYS_GPIOx branch clock for power management. The frequency of all clocks CLK_SYS_GPIOx is identical to CLK_SYS_PESS since they are derived from the same base clock BASE_SYS_CLK.

8.5 CAN gateway

8.5.1 Overview

Controller Area Network (CAN) is the definition of a high-performance communication protocol for serial data communication. The two CAN controllers in the LPC2917/19 provide a full implementation of the CAN protocol according to the *CAN specification version 2.0B*. The gateway concept is fully scalable with the number of CAN controllers, and always operates together with a separate powerful and flexible hardware acceptance filter.

The key features are:

- Supports 11-bit as well as 29-bit identifiers
- Double receive buffer and triple transmit buffer
- Programmable error-warning limit and error counters with read/write access
- Arbitration-lost capture and error-code capture with detailed bit position
- Single-shot transmission (i.e., no re-transmission)
- Listen-only mode (no acknowledge; no active error flags)
- Reception of ‘own’ messages (self-reception request)
- Full CAN mode for message reception

8.5.2 Global acceptance filter

The global acceptance filter provides look-up of received identifiers - called acceptance filtering in CAN terminology - for all the CAN controllers. It includes a CAN ID look-up table memory, in which software maintains one to five sections of identifiers. The CAN ID look-up table memory is 2 kB large (512 words, each of 32 bits). It can contain up to 1024 standard frame identifiers or 512 extended frame identifiers or a mixture of both types. It is also possible to define identifier groups for standard and extended message formats.

8.5.3 CAN pin description

The two CAN controllers in the LPC2917/19 have the pins listed below. The CAN pins are combined with other functions on the port pins of the LPC2917/19. Table 18 shows the CAN pins (x runs from 0 to 1).

Table 18. CAN pins

Symbol	Direction	Description
CANx TXDC	OUT	CAN channel x transmit data output
CANx RXDC	IN	CAN channel x receive data input

8.6 LIN

8.6.1 Overview

The LPC2917/19 contain two LIN 2.0 master controllers. These can be used as dedicated LIN 2.0 master controllers with additional support for sync break generation and with hardware implementation of the LIN protocol according to spec 2.0.

The key features are:

system-clock divider dedicated to the ADC clock. Conversion rate is determined by the ADC clock frequency divided by the number of resolution bits plus one. Accessing ADC registers requires an enabled ADC clock, which is controllable via the clock generation unit, see Section 8.8.4.

Each ADC has four start inputs. Note that start 0 and start 2 are captured in the system clock domain while start 1 and start 3 are captured in the ADC domain. The start inputs are connected at MSCSS level, see Section 8.7.2.1 for details.

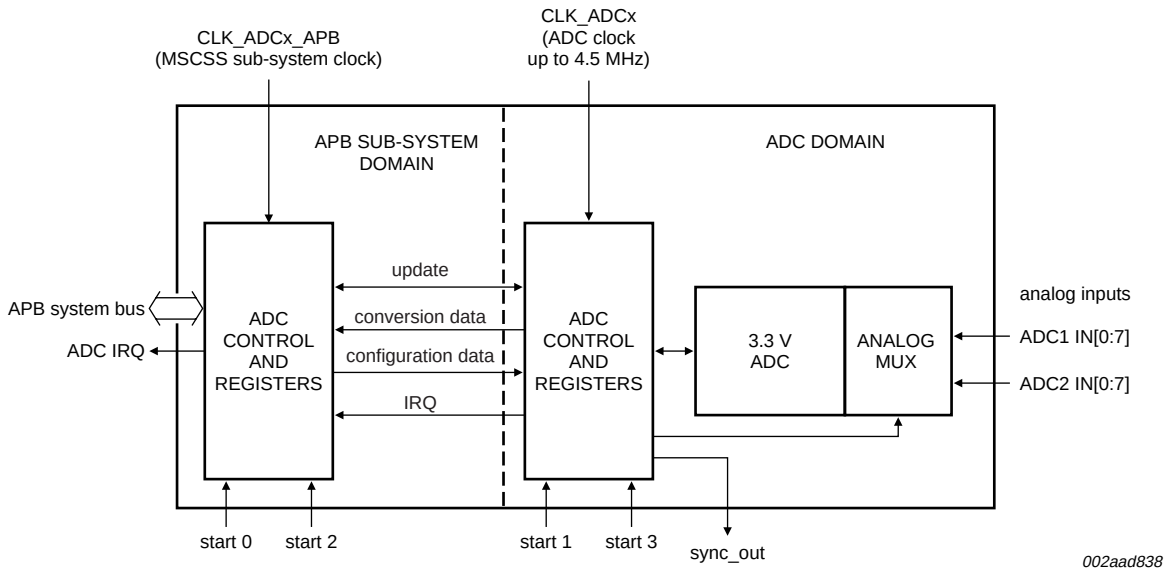


Fig 9. ADC block diagram

8.7.5.3 ADC pin description

The two ADC modules in the MSCSS have the pins described below. The ADCx input pins are combined with other functions on the port pins of the LPC2917/19. The VREFN and VREFP pins are common for both ADCs. Table 20 shows the ADC pins.

Table 20. Analog to digital converter pins

Symbol	Direction	Description
ADCn IN[7:0]	IN	analog input for ADCn, channel 7 to channel 0 (n is 1 or 2)
ADCn_EXT_START	IN	ADC external start-trigger input (n is 1 or 2)
VREFN	IN	ADC LOW reference level
VREFP	IN	ADC HIGH reference level

8.7.5.4 ADC clock description

The ADC modules are clocked from two different sources; CLK_MSCSS_ADCx_APB and CLK_ADCx (x = 1 or 2), see Section 7.2.2. Note that each ADC has its own CLK_ADCx and CLK_MSCSS_ADCx_APB branch clocks for power management. If an ADC is unused both its CLK_MSCSS_ADCx_APB and CLK_ADCx can be switched off.

The frequency of all the CLK_MSCSS_ADCx_APB clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK. Likewise the frequency of all the CLK_ADCx clocks is identical since they are derived from the same base clock BASE_ADC_CLK.

The register interface towards the system bus is clocked by CLK_MSCSS_ADCx_APB. Control logic for the analog section of the ADC is clocked by CLK_ADCx, see also Figure 9.

8.7.6 PWM

8.7.6.1 Overview

The MSCSS in the LPC2917/19 includes four PWM modules with the following features.

- Six pulse-width modulated output signals
- Double edge features (rising and falling edges programmed individually)
- Optional interrupt generation on match (each edge)
- Different operation modes: continuous or run-once
- 16-bit PWM counter and 16-bit prescale counter allow a large range of PWM periods
- A protective mode (TRAP) holding the output in a software-controllable state and with optional interrupt generation on a trap event
- Three capture registers and capture trigger pins with optional interrupt generation on a capture event
- Interrupt generation on match event, capture event, PWM counter overflow or trap event
- A burst mode mixing the external carrier signal with internally generated PWM
- Programmable sync-delay output to trigger other PWM modules (master/slave behavior)

8.7.6.2 Description

The ability to provide flexible waveforms allows PWM blocks to be used in multiple applications; e.g. automotive dimmer/lamp control and fan control. Pulse-width modulation is the preferred method for regulating power since no additional heat is generated and it is energy-efficient when compared with linear-regulating voltage control networks.

The PWM delivers the waveforms/pulses of the desired duty cycles and cycle periods. A very basic application of these pulses can be in controlling the amount of power transferred to a load. Since the duty cycle of the pulses can be controlled, the desired amount of power can be transferred for a controlled duration. Two examples of such applications are:

- Automotive dimmer controller: The flexibility of providing waves of a desired duty cycle and cycle period allows the PWM to control the amount of power to be transferred to the load. The PWM functions as a dimmer controller in this application
- Motor controller: The PWM provides multi-phase outputs, and these outputs can be controlled to have a certain pattern sequence. In this way the force/torque of the motor can be adjusted as desired. This makes the PWM function as a motor drive.

8.7.7.2 Description

See section Section 8.4.3.2 for a description of the timers.

8.7.7.3 MSCSS timer-pin description

MSCSS timer 0 has no external pins.

MSCSS timer 1 has a PAUSE pin available as external pin. The PAUSE pin is combined with other functions on the port pins of the LPC2917/19. Table 22 shows the MSCSS timer 1 external pin.

Table 22. MSCSS timer 1 pin

Symbol	Direction	Description
MSCSS PAUSE	IN	pause pin for MSCSS timer 1

8.7.7.4 MSCSS timer-clock description

The Timer modules in the MSCSS are clocked by CLK_MSCSS_MTMRx (x = 0-1), see Section 7.2.2. Note that each timer has its own CLK_MSCSS_MTMRx branch clock for power management. The frequency of all these clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

Note that, unlike the timer modules in the Peripheral SubSystem, the actual timer counter registers run at the same clock as the APB system interface CLK_MSCSS_APB. This clock is independent of the AHB system clock.

If a timer module is not used its CLK_MSCSS_MTMRx branch clock can be switched off.

8.8 Power, clock and reset control subsystem

8.8.1 Overview

The Power, Clock and Reset Control Subsystem (PCRSS) in the LPC2917/19 includes a Clock Generation Unit (CGU), a Reset Generation Unit (RGU) and a Power Management Unit (PMU).

8.8.2 Description

Figure 11 provides an overview of the PCRSS. An AHB-to-DTL bridge takes care of communication with the AHB system bus.

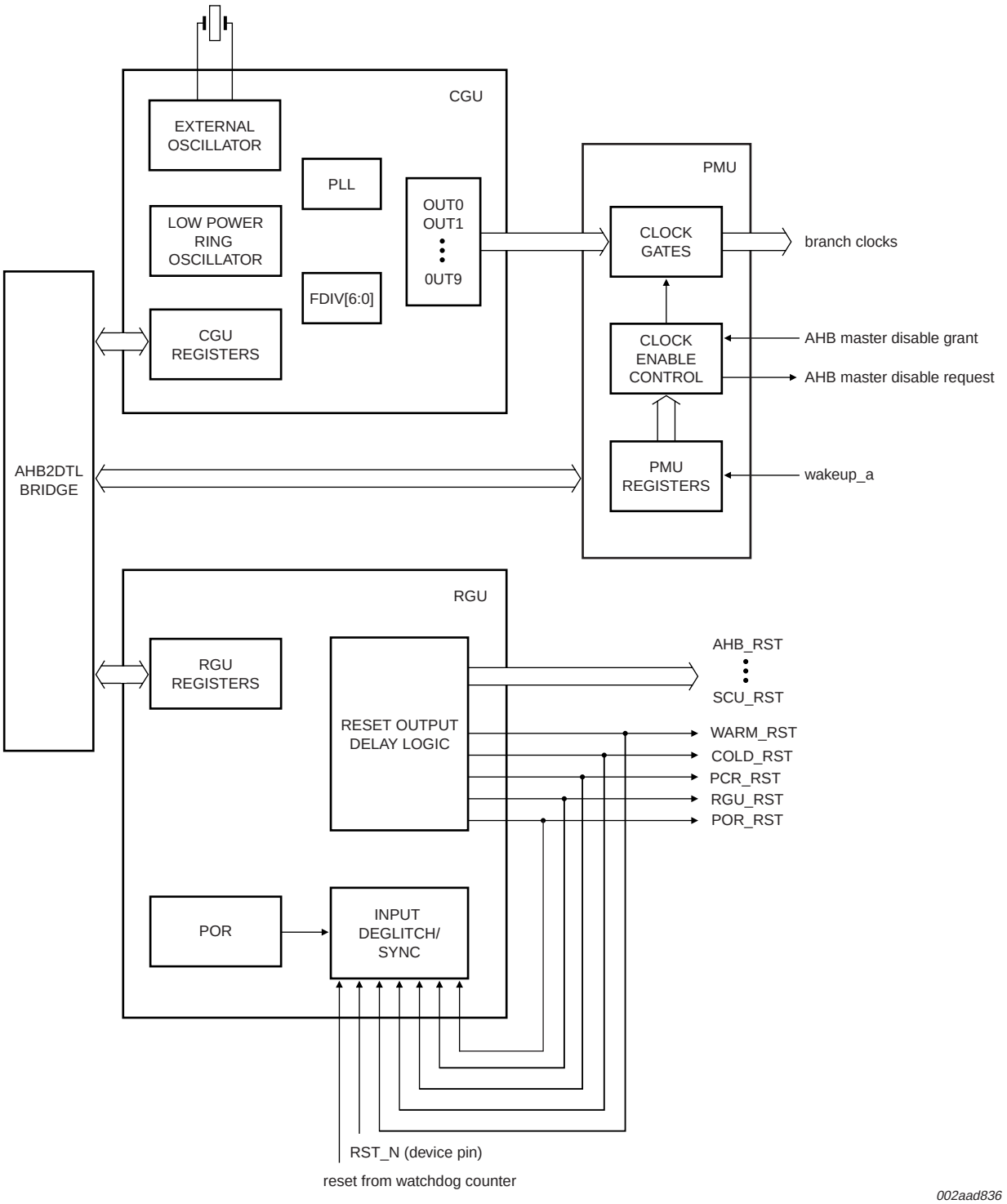


Fig 11. PCRSS block diagram

8.8.3 PCR subsystem clock description

The PCRSS is clocked by a number of different clocks. CLK_SYS_PCRSS clocks the AHB side of the AHB to DTL bus bridge and CLK_PCR_SLOW clocks the CGU, RGU and PMU internal logic, see Section 7.2.2. CLK_SYS_PCRSS is derived from BASE_SYS_CLK, which can be switched off in low-power modes. CLK_PCR_SLOW is derived from BASE_PCR_CLK and is always on in order to be able to wake up from low-power modes.

8.8.4 Clock Generation Unit (CGU)

8.8.4.1 Overview

The key features are:

- Generation of 10 and 2 test-base clocks, selectable from several embedded clock sources
- Crystal oscillator with power-down
- Control PLL with power-down
- Very low-power ring oscillator, always on to provide a ‘safe clock’
- Seven fractional clock dividers with L/D division
- Individual source selector for each base clock, with glitch-free switching
- Autonomous clock-activity detection on every clock source
- Protection against switching to invalid or inactive clock sources
- Embedded frequency counter
- Register write-protection mechanism to prevent unintentional alteration of clocks

Remark: Any clock-frequency adjustment has a direct impact on the timing of on-board peripherals such as the UARTs, SPI, watchdog, timers, CAN controller, LIN master controller, ADCs or flash memory interface.

8.8.4.2 Description

The clock generation unit provides 10 internal clock sources as described in Table 23.

Table 23. CGU base clocks

Number	Name	Frequency (MHz) [1]	Description
0	BASE_SAFE_CLK	0.4	base safe clock (always on)
1	BASE_SYS_CLK	80	base system clock
2	BASE_PCR_CLK	0.4 [2]	base PCR subsystem clock
3	BASE_IVNSS_CLK	80	base IVNSS subsystem clock
4	BASE_MSCSS_CLK	80	base MSCSS subsystem clock
5	BASE_UART_CLK	80	base UART clock
6	BASE_SPI_CLK	40	base SPI clock
7	BASE_TMR_CLK	80	base timers clock
8	BASE_ADC_CLK	4.5	base ADCs clock

[1] Maximum frequency that guarantees stable operation of the LPC2917/19.

[2] Fixed to low-power oscillator.

Table 25. Reset output configuration

Reset output	Reset source	Parts of the device reset when activated
POR_RST	power-on reset module	LP_OSC; is source for RGU_RST
RGU_RST	POR_RST, RST_N pin	RGU internal; is source for PCR_RST
PCR_RST	RGU_RST, WATCHDOG	PCR internal; is source for COLD_RST
COLD_RST	PCR_RST	parts with COLD_RST as reset source below
WARM_RST	COLD_RST	parts with WARM_RST as reset source below
SCU_RST	COLD_RST	SCU
CFID_RST	COLD_RST	CFID
FMC_RST	COLD_RST	embedded Flash Memory Controller (FMC)
EMC_RST	COLD_RST	embedded SRAM Memory Controller
SMC_RST	COLD_RST	external Static Memory Controller (SMC)
GESS_A2V_RST	WARM_RST	GeSS AHB-to-APB bridge
PESS_A2V_RST	WARM_RST	PeSS AHB-to-APB bridge
GPIO_RST	WARM_RST	all GPIO modules
UART_RST	WARM_RST	all UART modules
TMR_RST	WARM_RST	all Timer modules in PeSS
SPI_RST	WARM_RST	all SPI modules
IVNSS_A2V_RST	WARM_RST	IVNSS AHB-to-APB bridge
IVNSS_CAN_RST	WARM_RST	all CAN modules including Acceptance filter
IVNSS_LIN_RST	WARM_RST	all LIN modules
MSCSS_A2V_RST	WARM_RST	MSCSS AHB to APB bridge
MSCSS_PWM_RST	WARM_RST	all PWM modules
MSCSS_ADC_RST	WARM_RST	all ADC modules
MSCSS_TMR_RST	WARM_RST	all Timer modules in MSCSS
VIC_RST	WARM_RST	Vectored Interrupt Controller (VIC)
AHB_RST	WARM_RST	CPU and AHB Bus infrastructure

8.8.5.3 RGU pin description

The RGU module in the LPC2917/19 has the following pins. Table 26 shows the RGU pins.

Table 26. RGU pins

Symbol	Direction	Description
RST_N	IN	external reset input, active LOW; pulled up internally

8.8.6 Power Management Unit (PMU)

8.8.6.1 Overview

This module enables software to actively control the system's power consumption by disabling clocks not required in a particular operating mode.

Using the base clocks from the CGU as input, the PMU generates branch clocks to the rest of the LPC2917/19. Output clocks branched from the same base clock are phase- and frequency-related. These branch clocks can be individually controlled by software programming.

- Priority 15 corresponds to the highest priority

Software interrupt support is provided and can be supplied for:

- Testing Real-Time Operating System (RTOS) interrupt handling without using device-specific interrupt service routines
- Software emulation of an interrupt-requesting device, including interrupts

8.9.3 VIC pin description

The VIC module in the LPC2917/19 has no external pins.

8.9.4 VIC clock description

The VIC is clocked by CLK_SYS_VIC, see Section 7.2.2.

11. Static characteristics

Table 30. Static characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = -40 °C to +125 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
Core supply							
$V_{DD(CORE)}$	core supply voltage			1.71	1.80	1.89	V
$I_{DD(CORE)}$	core supply current	ARM9 and all peripherals active at max clock speeds		-	1.1	2.5	mA/ MHz
		all clocks off	[2]	-	30	450	µA
I/O supply							
$V_{DD(IO)}$	I/O supply voltage			2.7	-	3.6	V
Oscillator supply							
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			1.71	1.80	1.89	V
$I_{DD(OSC\_PLL)}$	oscillator and PLL supply current	start-up		3	-	4.5	mA
		normal mode		-	-	1	mA
		Power-down mode		-	-	2	µA
Analog-to-digital converter supply							
$V_{DDA(ADC3V3)}$	3.3 V ADC analog supply voltage			3.0	3.3	3.6	V
$I_{DDA(ADC3V3)}$	3.3 V ADC analog supply current	normal mode		-	-	1.9	mA
		Power-down mode		-	-	4	µA
Input pins and I/O pins configured as input							
V_I	input voltage	all port pins and $V_{DD(IO)}$ applied except port 0 pins 16 to 31 see Section 9	[7][8]	–0.5	-	+ 5.5	V
		port 0 pins 16 to 31	[8]			V_{VREFP}	
		all port pins and $V_{DD(IO)}$ not applied		–0.5	-	+3.6	V
		all other I/O pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		–0.5	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		2.0	-	-	V
V_{IL}	LOW-level input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-level input leakage current			-	-	1	µA

Table 31. Dynamic characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External static memory controller						
$t_{a(R)int}$	internal read access time		-	-	20.5	ns
$t_{a(W)int}$	internal write access time		-	-	24.9	ns
UART						
f_{UART}	UART frequency		$1/65024 f_{clk(uart)}$	-	$1/2 f_{clk(uart)}$	MHz
SPI						
f_{SPI}	SPI operating frequency	master operation	$1/65024 f_{clk(spi)}$	-	$1/2 f_{clk(spi)}$	MHz
		slave operation	$1/65024 f_{clk(spi)}$	-	$1/4 f_{clk(spi)}$	MHz
Jitter specification						
$t_{jit(cc)(p-p)}$	cycle to cycle jitter (peak-to-peak value)	on CAN TXDC pin [3]	-	0.4	1	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 125 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Table 23.

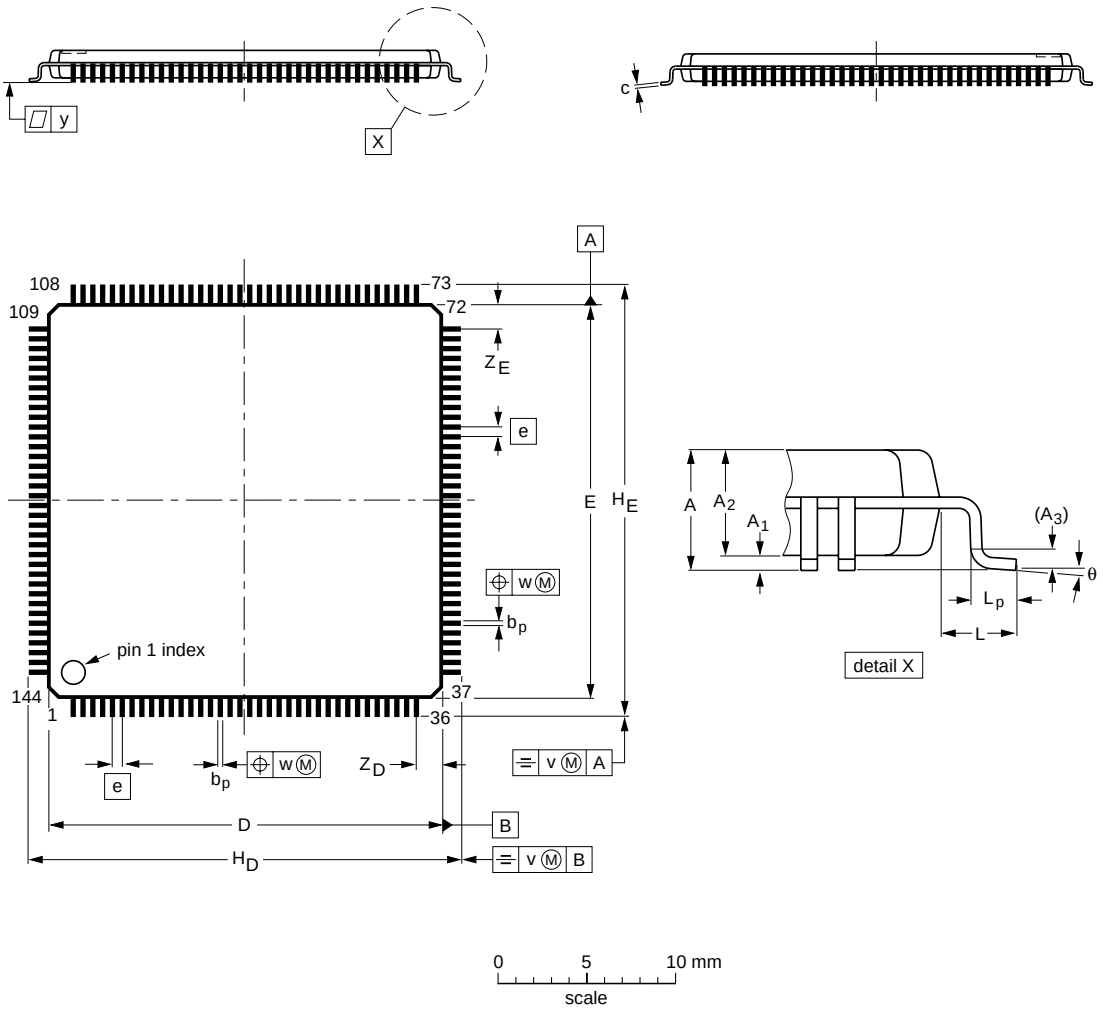
[3] This parameter is not part of production testing or final testing, hence only a typical value is stated.

[4] Oscillator start-up time depends on the quality of the crystal. For most crystals it takes about 1000 clock pulses until the clock is fully stable.

[5] Duty cycle clock should be as close as possible to 50 %.

13. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 15. Package outline SOT486-1 (LQFP144)

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 32 and 33

Table 32. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 33. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.