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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	108
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2919fbd144-551

2.4 On-chip static RAM

In addition to the two 16 kB TCMs the LPC2917/19 includes two static RAM memories: one of 32 kB and one of 16 kB. Both may be used for code and/or data storage.

3. Features

3.1 General

- ARM968E-S processor at 80 MHz maximum.
- AHB system bus at 80 MHz.
- On-chip memory:
  - Two Tightly Coupled Memories (TCM), 16 kB Instruction TCM (ITCM), 16 kB Data TCM (DTCM).
  - Two separate internal SRAM instances; 32 kB and 16 kB.
  - Up to 768 kB flash program memory.
- Two-channel CAN controller supporting Full-CAN and extensive message filtering.
- Two LIN master controllers with full hardware support for LIN communication.
- Two 550 UARTs with 16-byte TX and RX FIFO depths.
- Three full-duplex queued SPIs with four slave-select lines; 16 bits wide; 8 locations deep; TX FIFO and RX FIFO.
- Four 32-bit timers each containing four capture-and-compare registers linked to I/Os.
- Four 6-channel PWMs with capture and trap functionality.
- 32-bit watchdog with timer change protection, running on safe clock.
- Up to 108 general-purpose I/O pins with programmable pull-up, pull-down or bus keeper.
- Vectored Interrupt Controller (VIC) with 16 priority levels.
- Two 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 µs per channel. Each channel provides a compare function to minimize interrupts.
- Up to 24 level-sensitive external interrupt pins, including CAN and LIN wake-up features.
- External Static Memory Controller (SMC) with eight memory banks; up to 32-bit data bus; up to 24-bit address bus.
- Processor wake-up from power-down via external interrupt pins; CAN or LIN activity.
- Flexible Reset Generation Unit (RGU) able to control resets of individual modules.
- Flexible Clock Generation Unit (CGU) able to control clock frequency of individual modules:
  - On-chip very low-power ring oscillator; fixed frequency of 0.4 MHz; always on to provide a Safe_Clock source for system monitoring.
  - On-chip crystal oscillator with a recommended operating range from 10 MHz to 25 MHz - maximum PLL input 15 MHz.
  - On-chip PLL allows CPU operation up to a maximum CPU rate of 80 MHz.
  - Generation of up to 10 base clocks.
  - Seven fractional dividers.
- Highly configurable system Power Management Unit (PMU):
  - Clock control of individual modules.

Table 3. LQFP144 pin assignment *...continued*

Pin name	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P2[24]/PCAP3[1]/D22	16	GPIO 2, pin 24	-	PWM3 CAP1	EXTBUS D22
P2[25]/PCAP3[2]/D23	17	GPIO 2, pin 25	-	PWM3 CAP2	EXTBUS D23
$V_{DD(CORE)}$	18	1.8 V power supply for digital core			
$V_{SS(CORE)}$	19	ground for digital core			
P1[31]/CAP0[1]/MAT0[1]/EI5	20	GPIO 1, pin 31	TIMER0 CAP1	TIMER0 MAT1	EXTINT5
$V_{SS(IO)}$	21	ground for I/O			
P1[30]/CAP0[0]/MAT0[0]/EI4	22	GPIO 1, pin 30	TIMER0 CAP0	TIMER0 MAT0	EXTINT4
P3[8]/SCS2[0]/PMAT1[2]	23	GPIO 3, pin 8	SPI2 SCS0	PWM1 MAT2	-
P3[9]/SDO2/PMAT1[3]	24	GPIO 3, pin 9	SPI2 SDO	PWM1 MAT3	-
P1[29]/CAP1[0]/TRAP0/ PMAT3[5]	25	GPIO 1, pin 29	TIMER1 CAP0, EXT START	PWM TRAP0	PWM3 MAT5
P1[28]/CAP1[1]/TRAP1/ PMAT3[4]	26	GPIO 1, pin 28	TIMER1 CAP1, ADC1 EXT START	PWM TRAP1	PWM3 MAT4
P2[26]/CAP0[2]/MAT0[2]/EI6	27	GPIO 2, pin 26	TIMER0 CAP2	TIMER0 MAT2	EXTINT6
P2[27]/CAP0[3]/MAT0[3]/EI7	28	GPIO 2, pin 27	TIMER0 CAP3	TIMER0 MAT3	EXTINT7
P1[27]/CAP1[2]/TRAP2/ PMAT3[3]	29	GPIO 1, pin 27	TIMER1 CAP2, ADC2 EXT START	PWM TRAP2	PWM3 MAT3
P1[26]/PMAT2[0]/TRAP3/ PMAT3[2]	30	GPIO 1, pin 26	PWM2 MAT0	PWM TRAP3	PWM3 MAT2
$V_{DD(IO)}$	31	3.3 V power supply for I/O			
P1[25]/PMAT1[0]/PMAT3[1]	32	GPIO 1, pin 25	PWM1 MAT0	-	PWM3 MAT1
P1[24]/PMAT0[0]/PMAT3[0]	33	GPIO 1, pin 24	PWM0 MAT0	-	PWM3 MAT0
P1[23]/RXD0/CS5	34	GPIO 1, pin 23	UART0 RXD	-	EXTBUS CS5
P1[22]/TXD0/CS4	35	GPIO 1, pin 22	UART0 TXD	-	EXTBUS CS4
TMS	36	IEEE 1149.1 test mode select, pulled up internally			
TCK	37	IEEE 1149.1 test clock			
P1[21]/CAP3[3]/CAP1[3]/D7	38	GPIO 1, pin 21	TIMER3 CAP3	TIMER1 CAP3, MSCSS PAUSE	EXTBUS D7
P1[20]/CAP3[2]/SCS0[1]/D6	39	GPIO 1, pin 20	TIMER3 CAP2	SPI0 SCS1	EXTBUS D6
P1[19]/CAP3[1]/SCS0[2]/D5	40	GPIO 1, pin 19	TIMER3 CAP1	SPI0 SCS2	EXTBUS D5
P1[18]/CAP3[0]/SDO0/D4	41	GPIO 1, pin 18	TIMER3 CAP0	SPI0 SDO	EXTBUS D4
P1[17]/CAP2[3]/SDI0/D3	42	GPIO 1, pin 17	TIMER2 CAP3	SPI0 SDI	EXTBUS D3
$V_{SS(IO)}$	43	ground for I/O			
P1[16]/CAP2[2]/SCK0/D2	44	GPIO 1, pin 16	TIMER2 CAP2	SPI0 SCK	EXTBUS D2
P2[0]/MAT2[0]/TRAP3/D8	45	GPIO 2, pin 0	TIMER2 MAT0	PWM TRAP3	EXTBUS D8
P2[1]/MAT2[1]/TRAP2/D9	46	GPIO 2, pin 1	TIMER2 MAT1	PWM TRAP2	EXTBUS D9
P3[10]/SDI2/PMAT1[4]	47	GPIO 3, pin 10	SPI2 SDI	PWM1 MAT4	-
P3[11]/SCK2/PMAT1[5]	48	GPIO 3, pin 11	SPI2 SCK	PWM1 MAT5	-
P1[15]/CAP2[1]/SCS0[0]/D1	49	GPIO 1, pin 15	TIMER2 CAP1	SPI0 SCS0	EXTBUS D1
P1[14]/CAP2[0]/SCS0[3]/D0	50	GPIO 1, pin 14	TIMER2 CAP0	SPI0 SCS3	EXTBUS D0

Table 3. LQFP144 pin assignment *...continued*

Pin name	Pin	Description			
		Default function	Function 1	Function 2	Function 3
P2[10]/PMAT0[2]/SCS0[0]	91	GPIO 2, pin 10	-	PWM0 MAT2	SPI0 SCS0
P2[11]/PMAT0[3]/SCK0	92	GPIO 2, pin 11	-	PWM0 MAT3	SPI0 SCK
P0[0]/TXDC0/D24	93	GPIO 0, pin 0	-	CAN0 TXDC	EXTBUS D24
$V_{SS(IO)}$	94	ground for I/O			
P0[1]/RXDC0/D25	95	GPIO 0, pin 1	-	CAN0 RXDC	EXTBUS D25
P0[2]/PMAT0[0]/D26	96	GPIO 0, pin 2	-	PWM0 MAT0	EXTBUS D26
P0[3]/PMAT0[1]/D27	97	GPIO 0, pin 3	-	PWM0 MAT1	EXTBUS D27
P3[0]/PMAT2[0]/CS6	98	GPIO 3, pin 0	-	PWM2 MAT0	EXTBUS CS6
P3[1]/PMAT2[1]/CS7	99	GPIO 3, pin 1	-	PWM2 MAT1	EXTBUS CS7
P2[12]/PMAT0[4]/SDI0	100	GPIO 2, pin 12	-	PWM0 MAT4	SPI0 SDI
P2[13]/PMAT0[5]/SDO0	101	GPIO 2, pin 13	-	PWM0 MAT5	SPI0 SDO
P0[4]/PMAT0[2]/D28	102	GPIO 0, pin 4	-	PWM0 MAT2	EXTBUS D28
P0[5]/PMAT0[3]/D29	103	GPIO 0, pin 5	-	PWM0 MAT3	EXTBUS D29
$V_{DD(IO)}$	104	3.3 V power supply for I/O			
P0[6]/PMAT0[4]/D30	105	GPIO 0, pin 6	-	PWM0 MAT4	EXTBUS D30
P0[7]/PMAT0[5]/D31	106	GPIO 0, pin 7	-	PWM0 MAT5	EXTBUS D31
$V_{DDA(ADC3V3)}$	107	3.3 V power supply for ADC			
JTAGSEL	108	TAP controller select input; LOW-level selects the ARM debug mode; HIGH-level selects boundary scan and flash programming; pulled up internally			
n.c.	109	not connected			
VREFP	110	HIGH reference for ADC			
VREFN	111	LOW reference for ADC			
P0[8]/IN1[0]/TXDL0/A20	112	GPIO 0, pin 8	ADC1 IN0	LIN0 TXDL	EXTBUS A20
P0[9]/IN1[1]/RXDL0/A21	113	GPIO 0, pin 9	ADC1 IN1	LIN0 RXDL	EXTBUS A21
P0[10]/IN1[2]/PMAT1[0]/A8	114	GPIO 0, pin 10	ADC1 IN2	PWM1 MAT0	EXTBUS A8
P0[11]/IN1[3]/PMAT1[1]/A9	115	GPIO 0, pin 11	ADC1 IN3	PWM1 MAT1	EXTBUS A9
P2[14]/PCAP0[0]/BLS0	116	GPIO 2, pin 14	-	PWM0 CAP0	EXTBUS BLS0
P2[15]/PCAP0[1]/BLS1	117	GPIO 2, pin 15	-	PWM0 CAP1	EXTBUS BLS1
P3[2]/MAT3[0]/PMAT2[2]	118	GPIO 3, pin 2	TIMER3 MAT0	PWM2 MAT2	-
$V_{SS(IO)}$	119	ground for I/O			
P3[3]/MAT3[1]/PMAT2[3]	120	GPIO 3, pin 3	TIMER3 MAT1	PWM2 MAT3	-
P0[12]/IN1[4]/PMAT1[2]/A10	121	GPIO 0, pin 12	ADC1 IN4	PWM1 MAT2	EXTBUS A10
P0[13]/IN1[5]/PMAT1[3]/A11	122	GPIO 0, pin 13	ADC1 IN5	PWM1 MAT3	EXTBUS A11
P0[14]/IN1[6]/PMAT1[4]/A12	123	GPIO 0, pin 14	ADC1 IN6	PWM1 MAT4	EXTBUS A12
P0[15]/IN1[7]/PMAT1[5]/A13	124	GPIO 0, pin 15	ADC1 IN7	PWM1 MAT5	EXTBUS A13
P0[16]IN2[0]/TXD0/A22	125	GPIO 0, pin 16	ADC2 IN0	UART0 TXD	EXTBUS A22
P0[17]/IN2[1]/RXD0/A23	126	GPIO 0, pin 17	ADC2 IN1	UART0 RXD	EXTBUS A23
$V_{DD(CORE)}$	127	1.8 V power supply for digital core			
$V_{SS(CORE)}$	128	ground for digital core			
P2[16]/TXD1/PCAP0[2]/BLS2	129	GPIO 2, pin 16	UART1 TXD	PWM0 CAP2	EXTBUS BLS2

7.1.3 IEEE 1149.1 interface pins (JTAG boundary-scan test)

The LPC2917/19 contains boundary-scan test logic according to IEEE 1149.1, also referred to in this document as JTAG. The boundary-scan test pins can be used to connect a debugger probe for the embedded ARM processor. Pin JTAGSEL selects between boundary-scan mode and debug mode. Table 5 shows the boundary- scan test pins.

Table 5. IEEE 1149.1 boundary-scan test and debug interface

Symbol	Description
JTAGSEL	TAP controller select input. LOW-level selects ARM debug mode and HIGH-level selects boundary scan and flash programming; pulled up internally
TRST_N	test reset input; pulled up internally (active LOW)
TMS	test mode select input; pulled up internally
TDI	test data input, pulled up internally
TDO	test data output
TCK	test clock input

7.1.4 Power supply pins description

Table 6 shows the power supply pins.

Table 6. Power supplies

Symbol	Description
$V_{DD(CORE)}$	digital core supply 1.8 V
$V_{SS(CORE)}$	digital core ground (digital core, ADC1/2)
$V_{DD(IO)}$	I/O pins supply 3.3 V
$V_{SS(IO)}$	I/O pins ground
$V_{DD(OSC)}$	oscillator and PLL supply
$V_{SS(OSC)}$	oscillator ground
$V_{DDA(ADC3V3)}$	ADC1/2 3.3 V supply
$V_{SS(PLL)}$	PLL ground

7.2 Clocking strategy

7.2.1 Clock architecture

The LPC2917/19 contains several different internal clock areas. Peripherals like Timers, SPI, UART, CAN and LIN have their own individual clock sources called Base Clocks. All base clocks are generated by the Clock Generation Unit (CGU). They may be unrelated in frequency and phase and can have different clock sources within the CGU.

The system clock for the CPU and AHB Bus infrastructure has its own base clock. This means most peripherals are clocked independently from the system clock. See Figure 3 for an overview of the clock areas within the device.

Within each clock area there may be multiple branch clocks, which offers very flexible control for power-management purposes. All branch clocks are outputs of the Power Management Unit (PMU) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase. See Section 8.8 for more details of clock and power control within the device.

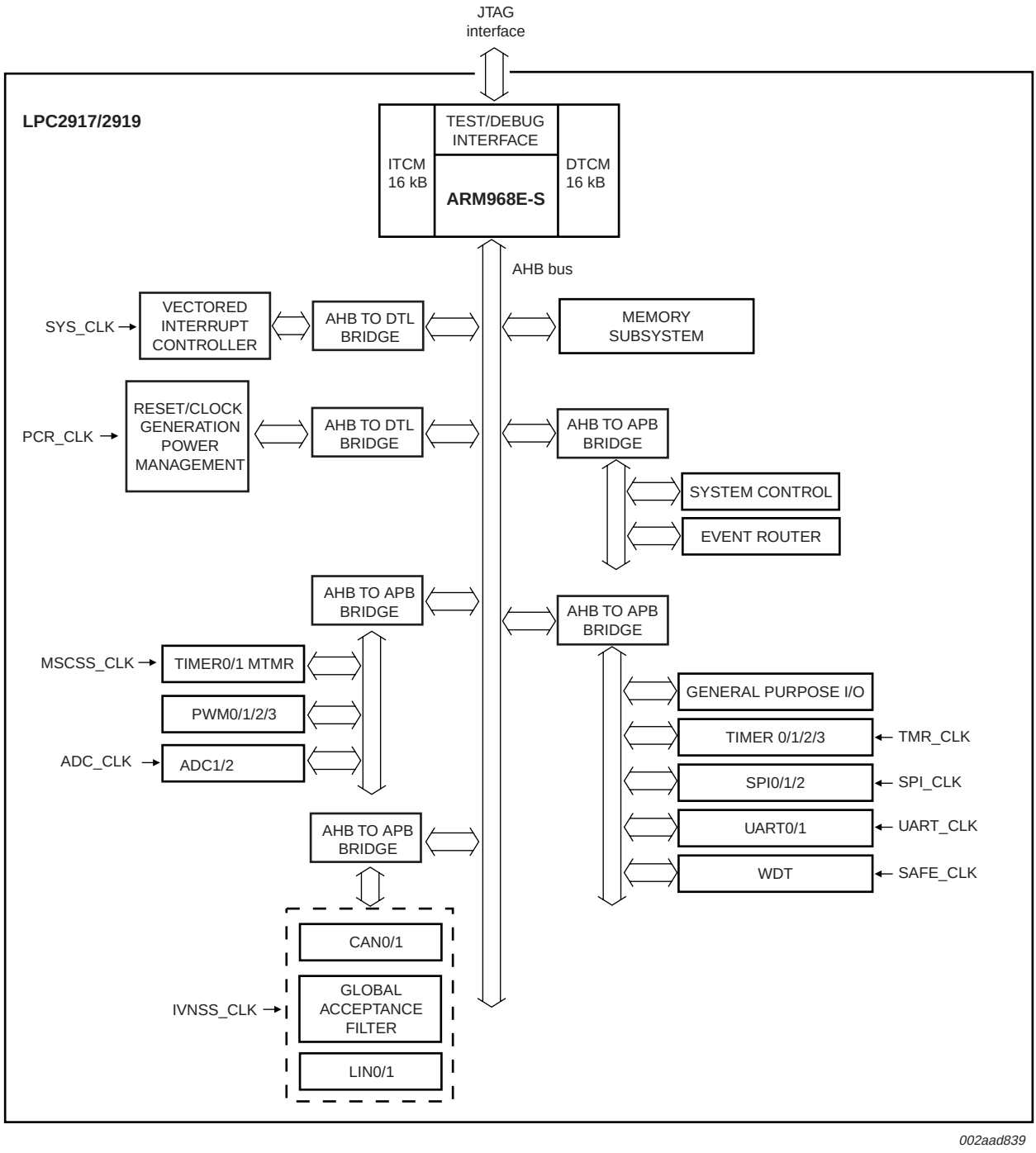


Fig 3. LPC2917/19 block diagram, overview of clock areas

7.2.2 Base clock and branch clock relationship

The next table contains an overview of all the base blocks in the LPC2917/19 and their derived branch clocks. A short description is given of the hardware parts that are clocked with the individual branch clocks. In relevant cases more detailed information can be

found in the specific subsystem description. Some branch clocks have special protection since they clock vital system parts of the device and should (for example) not be switched off. See Section 8.8.6 for more details of how to control the individual branch clocks.

Table 7. Base clock and branch clock overview

Base clock	Branch clock name	Parts of the device clocked by this branch clock	Remark
BASE_SAFE_CLK	CLK_SAFE	watchdog timer	[1]
BASE_SYS_CLK	CLK_SYS_CPU	ARM968E-S and TCMs	
	CLK_SYS_SYS	AHB bus infrastructure	
	CLK_SYS_PCRSS	AHB side of bridge in PCRSS	
	CLK_SYS_FMC	Flash Memory Controller	
	CLK_SYS_RAM0	Embedded SRAM Controller 0 (32 kB)	
	CLK_SYS_RAM1	Embedded SRAM Controller 1 (16 kB)	
	CLK_SYS_SMC	External Static Memory Controller	
	CLK_SYS_GESS	General Subsystem	
	CLK_SYS_VIC	Vectored Interrupt Controller	
	CLK_SYS_PESS	Peripheral Subsystem	[2] [4]
	CLK_SYS_GPIO0	GPIO bank 0	
	CLK_SYS_GPIO1	GPIO bank 1	
	CLK_SYS_GPIO2	GPIO bank 2	
	CLK_SYS_GPIO3	GPIO bank 3	
	CLK_SYS_IVNSS_A	AHB side of bridge of IVNSS	
BASE_PCR_CLK	CLK_PCR_SLOW	PCRSS, CGU, RGU and PMU logic clock	[1], [3]
BASE_IVNSS_CLK	CLK_IVNSS_APB	APB side of the IVNSS	
	CLK_IVNSS_CANCA	CAN controller Acceptance Filter	
	CLK_IVNSS_CANC0	CAN channel 0	
	CLK_IVNSS_CANC1	CAN channel 1	
	CLK_IVNSS_LIN0	LIN channel 0	
	CLK_IVNSS_LIN1	LIN channel 1	
BASE_MSCSS_CLK	CLK_MSCSS_APB	APB side of the MSCSS	
	CLK_MSCSS_MTMR0	Timer 0 in the MSCSS	
	CLK_MSCSS_MTMR1	Timer 1 in the MSCSS	
	CLK_MSCSS_PWM0	PWM 0	
	CLK_MSCSS_PWM1	PWM 0	
	CLK_MSCSS_PWM2	PWM 0	
	CLK_MSCSS_PWM3	PWM 0	
	CLK_MSCSS_ADC1_APB	APB side of ADC 1	
	CLK_MSCSS_ADC2_APB	APB side of ADC 2	

Depending on the operating mode selected, the SPI_CS_OUT outputs operate as an active-HIGH frame synchronization output for Texas Instruments synchronous serial frame format or an active-LOW chip select for SPI.

Each data frame is between four and 16 bits long, depending on the size of words programmed, and is transmitted starting with the MSB.

There are two basic frame types that can be selected:

- Texas Instruments synchronous serial
- Motorola Serial Peripheral Interface

8.4.5.3 Modes of operation

The SPI module can operate in:

- Master mode:
  - Normal transmission mode
  - Sequential slave mode
- Slave mode

8.4.5.4 SPI pin description

The three SPI modules in the LPC2917/19 have the pins listed below. The pins are combined with other functions on the port pins of the LPC2917/19, see Section 8.3.3. Table 16 shows the SPI pins (x runs from 0 to 2; y runs from 0 to 3).

Table 16. SPI pins

Symbol	Direction	Description
SPIx SCSy	IN/OUT	SPIx chip select[1][2]
SPIx SCK	IN/OUT	SPIx clock[1]
SPIx SDI	IN	SPIx data input
SPIx SDO	OUT	SPIx data output

[1] Direction of SPIx SCS and SPIx SCK pins depends on master or slave mode. These pins are output in master mode, input in slave mode.

[2] In slave mode there is only one chip select input pin, SPIx SCS0. The other chip selects have no function in slave mode.

8.4.5.5 SPI clock description

The SPI modules are clocked by two different clocks; CLK_SYS_PESS and CLK_SPIx (x = 0-2), see Section 7.2.2. Note that each SPI has its own CLK_SPIx branch clock for power management. The frequency of all clocks CLK_SPIx is identical as they are derived from the same base clock BASE_CLK_SPI. The register interface towards the system bus is clocked by CLK_SYS_PESS. The serial-clock rate divisor is clocked by CLK_SPIx.

The SPI clock frequency can be controlled by the CGU. In master mode the SPI clock frequency (CLK_SPIx) must be set to at least twice the SPI serial clock rate on the interface. In slave mode CLK_SPIx must be set to four times the SPI serial clock rate on the interface.

control. Several other trigger possibilities are provided for the ADCs (external, cascaded or following a PWM). The capture inputs of both timers can also be used to capture the start pulse of the ADCs.

The PWMs can be used to generate waveforms in which the frequency, duty cycle and rising and falling edges can be controlled very precisely. Capture inputs are provided to measure event phases compared to the main counter. Depending on the applications, these inputs can be connected to digital sensor motor outputs or digital external signals. Interrupt signals are generated on several events to closely interact with the CPU.

The ADCs can be used for any application needing accurate digitized data from analog sources. To support applications like motor control, a mechanism to synchronize several PWMs and ADCs is available (sync_in and sync_out).

Note that the PWMs run on the PWM clock and the ADCs on the ADC clock, see Section 8.8.4.

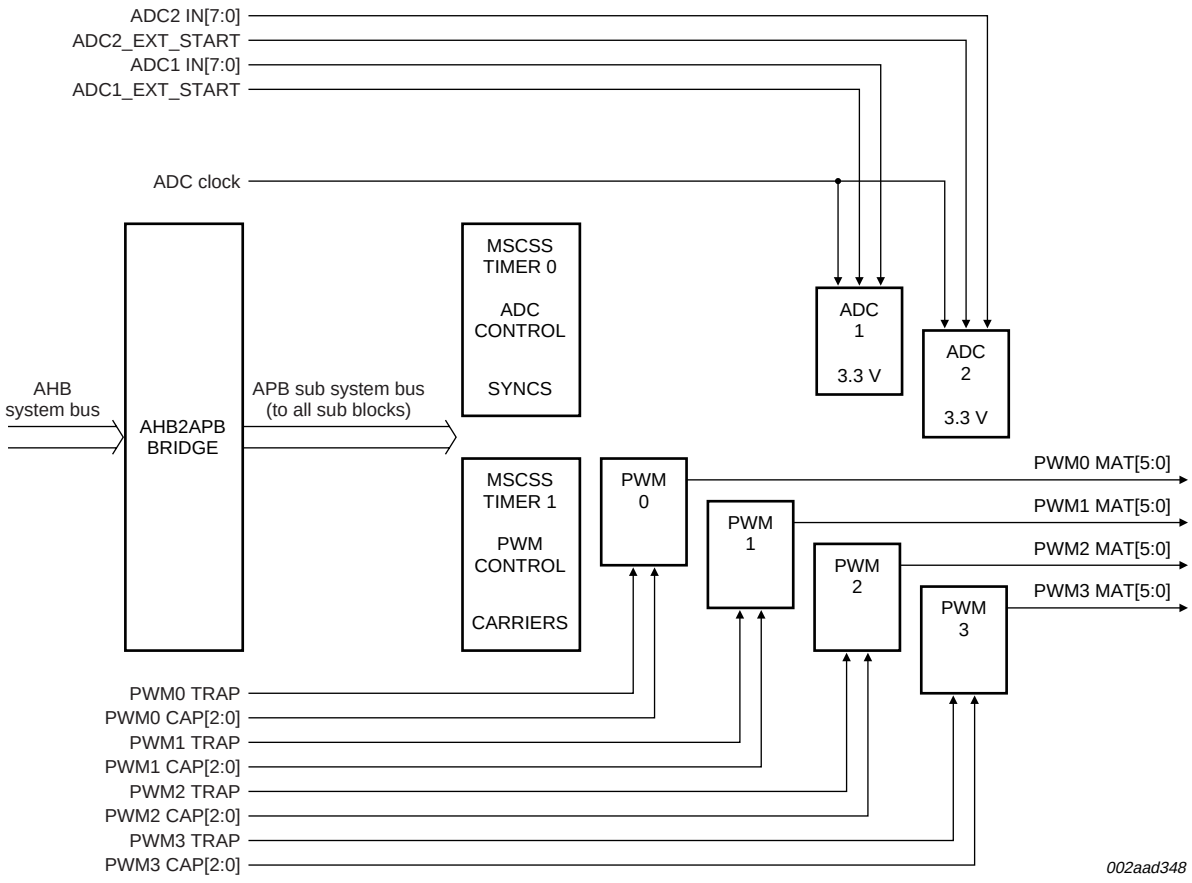


Fig 7. Modulation and sampling control subsystem block diagram

8.7.2.1 Synchronization and trigger features of the MSCSS

The MSCSS contains two internal timers to generate synchronization and carrier pulses for the ADCs and PWMs. Figure 8 shows how the timers are connected to the ADC and PWM modules.

Each ADC module has four start inputs. An ADC conversion is started when one of the start ADC conditions is valid:

- Start 0: ADC external start input pin; can be triggered at a positive or negative edge. Note that this signal is captured in the ADC clock domain
- Start 1: If the 'preceding' ADC conversion is ended, the sync_out signal starts an ADC conversion. This signal is captured in the MSCSS subsystem clock domain, see Section 8.7.5.2. As can be seen in Figure 8, the sync_out of ADC1 is connected to the start 1 input of ADC2 and the sync_out of ADC2 is connected to the start 1 input of ADC1.
- Start 2: The PWM sync_out can start an ADC conversion. The sync_out signal is synchronized to the ADC clock in the ADC module. This signal is captured in the MSCSS subsystem clock domain.
- Start 3: The match outputs from MSCSS timer 0 are connected to the start 3 inputs of the ADCs. This signal is captured in the ADC clock domain.

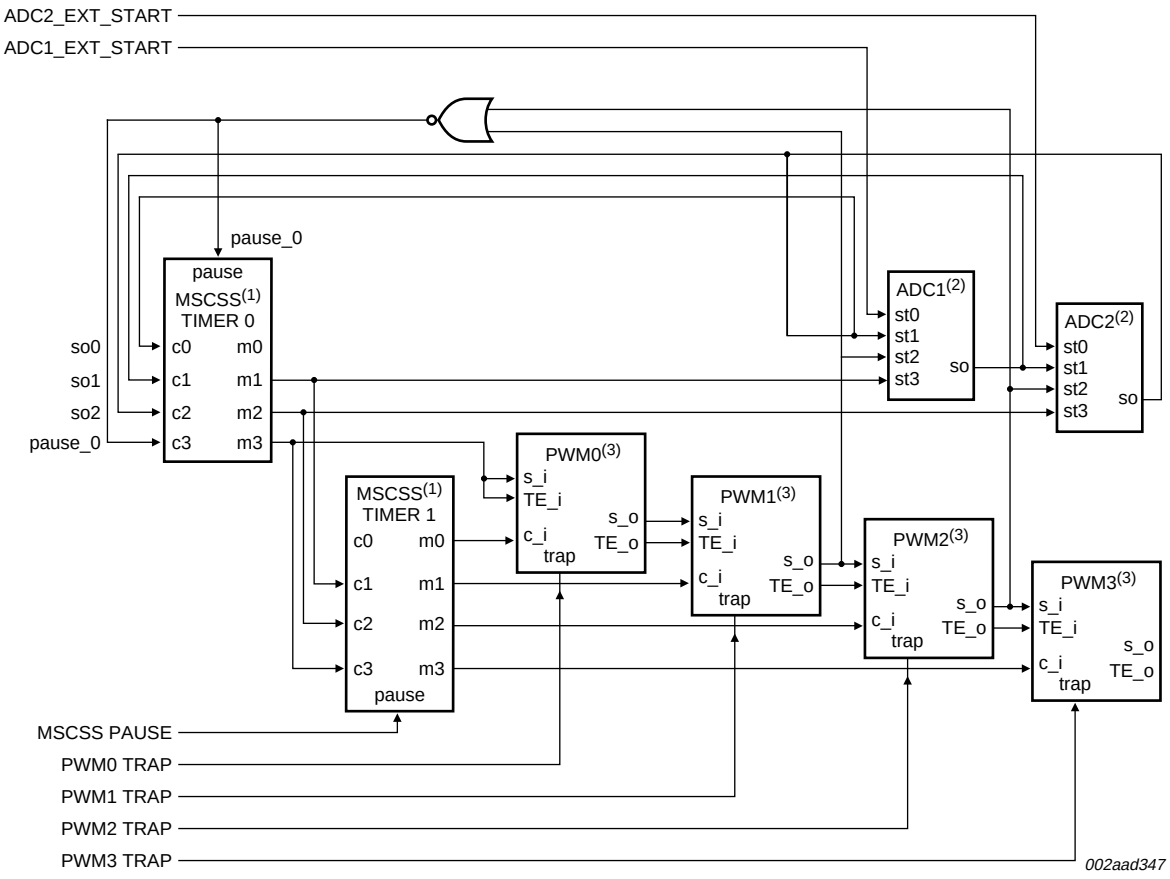
The PWM_sync and trans_enable_in of PWM 0 are connected to the 4th match output of MSCSS timer 0 to start the PWM after a pre-programmed delay. This sync signal is cascaded through all PWMs, allowing a programmable delay offset between subsequent PWMs. The sync delay of each PWM can be programmed synchronously or with a different phase for spreading the power load.

The match outputs of MSCSS timer 1 (PWM control) are connected to the corresponding carrier inputs of the PWM modules. The carrier signal is modulated with the PWM-generated waveforms.

The pause input of MSCSS timer 1 (PWM Control) is connected to an external input pin. Generation of the carrier signal is stopped by asserting the pause of this timer.

The pause input of MSCSS timer 0 (ADC Control) is connected to a 'NOR' of the PWM_sync outputs (start 2 input on the ADCs). If the pause feature of this timer is enabled the timer only counts when one of the PWM_sync outputs is active HIGH. This feature can be used to start the ADC once every x PWM cycles, where x corresponds to the value in the match register of the timer. In this case the start 3 input of the ADC should be enabled (start on match output of MSCSS timer 0).

The signals connected to the capture inputs of the timers (both MSCSS timer 0 and MSCSS timer 1) are intended for debugging.



(1) Timers:

c0 to c3 = capture in 0 to capture in 3

m0 to m3 = match out 0 to match out 3

(2) ADCs:

st0 to st3 = start 0 to start 3 inputs

s0 to s3 = sync_out 0 to sync_out 3

(3) PWMs:

c_i = carrier in

s_i = sync_in

s_o = sync_out

TE_i = trans_enable_in

TE_o = trans_enable_out

Fig 8. Modulation and sampling-control subsystem synchronization and triggering

8.7.3 MSCSS pin description

The pins of the LPC2917/19 MSCSS associated with the two ADC modules are described in Section 8.7.5.3. Pins directly connected to the four PWM modules are described in Section 8.7.6.5: pins directly connected to the MSCSS timer 1 module are described in Section 8.7.7.3.

8.7.4 MSCSS clock description

The MSCSS is clocked from a number of different sources:

8.7.7.2 Description

See section Section 8.4.3.2 for a description of the timers.

8.7.7.3 MSCSS timer-pin description

MSCSS timer 0 has no external pins.

MSCSS timer 1 has a PAUSE pin available as external pin. The PAUSE pin is combined with other functions on the port pins of the LPC2917/19. Table 22 shows the MSCSS timer 1 external pin.

Table 22. MSCSS timer 1 pin

Symbol	Direction	Description
MSCSS PAUSE	IN	pause pin for MSCSS timer 1

8.7.7.4 MSCSS timer-clock description

The Timer modules in the MSCSS are clocked by CLK_MSCSS_MTMRx (x = 0-1), see Section 7.2.2. Note that each timer has its own CLK_MSCSS_MTMRx branch clock for power management. The frequency of all these clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

Note that, unlike the timer modules in the Peripheral SubSystem, the actual timer counter registers run at the same clock as the APB system interface CLK_MSCSS_APB. This clock is independent of the AHB system clock.

If a timer module is not used its CLK_MSCSS_MTMRx branch clock can be switched off.

8.8 Power, clock and reset control subsystem

8.8.1 Overview

The Power, Clock and Reset Control Subsystem (PCRSS) in the LPC2917/19 includes a Clock Generation Unit (CGU), a Reset Generation Unit (RGU) and a Power Management Unit (PMU).

8.8.2 Description

Figure 11 provides an overview of the PCRSS. An AHB-to-DTL bridge takes care of communication with the AHB system bus.

Table 27. Branch clock overview *…continued*

Legend:
'1' Indicates that the related register bit is tied off to logic HIGH, all writes are ignored
'0' Indicates that the related register bit is tied off to logic LOW, all writes are ignored
'+' Indicates that the related register bit is readable and writable

Branch clock name	Base clock	Implemented switch on/off mechanism		
		WAKE-UP	AUTO	RUN
CLK_SYS_VIC	BASE_SYS_CLK	+	+	+
CLK_SYS_PESS	BASE_SYS_CLK	+	+	+
CLK_SYS_GPIO0	BASE_SYS_CLK	+	+	+
CLK_SYS_GPIO1	BASE_SYS_CLK	+	+	+
CLK_SYS_GPIO2	BASE_SYS_CLK	+	+	+
CLK_SYS_GPIO3	BASE_SYS_CLK	+	+	+
CLK_SYS_IVNSS_A	BASE_SYS_CLK	+	+	+
CLK_SYS_MSCSS_A	BASE_SYS_CLK	+	+	+
CLK_SYS_CHCA	BASE_SYS_CLK	+	+	+
CLK_SYS_CHCB	BASE_SYS_CLK	+	+	+
CLK_PCR_SLOW	BASE_PCR_CLK	+	+	1
CLK_IVNSS_APB	BASE_IVNSS_CLK	+	+	+
CLK_IVNSS_CANC0	BASE_IVNSS_CLK	+	+	+
CLK_IVNSS_CANC1	BASE_IVNSS_CLK	+	+	+
CLK_IVNSS_LIN0	BASE_IVNSS_CLK	+	+	+
CLK_IVNSS_LIN1	BASE_IVNSS_CLK	+	+	+
CLK_MSCSS_APB	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_MTMR0	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_MTMR1	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_PWM0	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_PWM1	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_PWM2	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_PWM3	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_ADC1_APB	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_ADC2_APB	BASE_MSCSS_CLK	+	+	+
CLK_UART0	BASE_UART_CLK	+	+	+
CLK_UART1	BASE_UART_CLK	+	+	+
CLK_SPI0	BASE_SPI_CLK	+	+	+
CLK_SPI1	BASE_SPI_CLK	+	+	+
CLK_SPI2	BASE_SPI_CLK	+	+	+
CLK_TMR0	BASE_TMR_CLK	+	+	+
CLK_TMR1	BASE_TMR_CLK	+	+	+
CLK_TMR2	BASE_TMR_CLK	+	+	+
CLK_TMR3	BASE_TMR_CLK	+	+	+

9. Limiting values

Table 28. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Supply pins						
P_{tot}	total power dissipation		[1]	-	1	W
$V_{DD(CORE)}$	core supply voltage			–0.5	+2.0	V
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			–0.5	+2.0	V
$V_{DDA(ADC3V3)}$	3.3 V ADC analog supply voltage			–0.5	+4.6	V
$V_{DD(IO)}$	I/O supply voltage			–0.5	+4.6	V
I_{DD}	supply current	average value per supply pin	[2]	-	98	mA
I_{SS}	ground current	average value per ground pin	[2]	-	98	mA
Input pins and I/O pins						
V_{XIN_OSC}	voltage on pin XIN_OSC			–0.5	+2.0	V
$V_{I(IO)}$	I/O input voltage		[3][4][5]	–0.5	$V_{DD(IO)}$ + 3.0	V
$V_{I(ADC)}$	ADC input voltage	I/O port 0.	[4][5]	–0.5	$V_{DDA(ADC3V3)}$ + 0.5	V
V_{VREFP}	voltage on pin VREFP			–0.5	+3.6	V
V_{VREFN}	voltage on pin VREFN			–0.5	+3.6	V
$I_{I(ADC)}$	ADC input current	average value per input pin	[2]	-	35	mA
Output pins and I/O pins configured as output						
I_{OHS}	HIGH-level short-circuit output current	drive HIGH, output shorted to $V_{SS(IO)}$	[9]	-	–33	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW, output shorted to $V_{DD(IO)}$	[9]	-	+38	mA
General						
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_{vj}	virtual junction temperature		[6]	–40	+125	°C
Memory						
$n_{endu(fl)}$	endurance of flash memory			-	100 000	cycle
$t_{ret(fl)}$	flash memory retention time			-	20	year

11. Static characteristics

Table 30. Static characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = -40 °C to +125 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
Core supply							
$V_{DD(CORE)}$	core supply voltage			1.71	1.80	1.89	V
$I_{DD(CORE)}$	core supply current	ARM9 and all peripherals active at max clock speeds		-	1.1	2.5	mA/ MHz
		all clocks off	[2]	-	30	450	µA
I/O supply							
$V_{DD(IO)}$	I/O supply voltage			2.7	-	3.6	V
Oscillator supply							
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			1.71	1.80	1.89	V
$I_{DD(OSC\_PLL)}$	oscillator and PLL supply current	start-up		3	-	4.5	mA
		normal mode		-	-	1	mA
		Power-down mode		-	-	2	µA
Analog-to-digital converter supply							
$V_{DDA(ADC3V3)}$	3.3 V ADC analog supply voltage			3.0	3.3	3.6	V
$I_{DDA(ADC3V3)}$	3.3 V ADC analog supply current	normal mode		-	-	1.9	mA
		Power-down mode		-	-	4	µA
Input pins and I/O pins configured as input							
V_I	input voltage	all port pins and $V_{DD(IO)}$ applied except port 0 pins 16 to 31 see Section 9	[7][8]	–0.5	-	+ 5.5	V
		port 0 pins 16 to 31	[8]			V_{VREFP}	
		all port pins and $V_{DD(IO)}$ not applied		–0.5	-	+3.6	V
		all other I/O pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		–0.5	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		2.0	-	-	V
V_{IL}	LOW-level input voltage	all port pins, RESET_N, TRST_N, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-level input leakage current			-	-	1	µA

Table 31. Dynamic characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{vj} = −40 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External static memory controller						
$t_{a(R)int}$	internal read access time		-	-	20.5	ns
$t_{a(W)int}$	internal write access time		-	-	24.9	ns
UART						
f_{UART}	UART frequency		$1/65024 f_{clk(uart)}$	-	$1/2 f_{clk(uart)}$	MHz
SPI						
f_{SPI}	SPI operating frequency	master operation	$1/65024 f_{clk(spi)}$	-	$1/2 f_{clk(spi)}$	MHz
		slave operation	$1/65024 f_{clk(spi)}$	-	$1/4 f_{clk(spi)}$	MHz
Jitter specification						
$t_{jit(cc)(p-p)}$	cycle to cycle jitter (peak-to-peak value)	on CAN TXDC pin [3]	-	0.4	1	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 125 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Table 23.

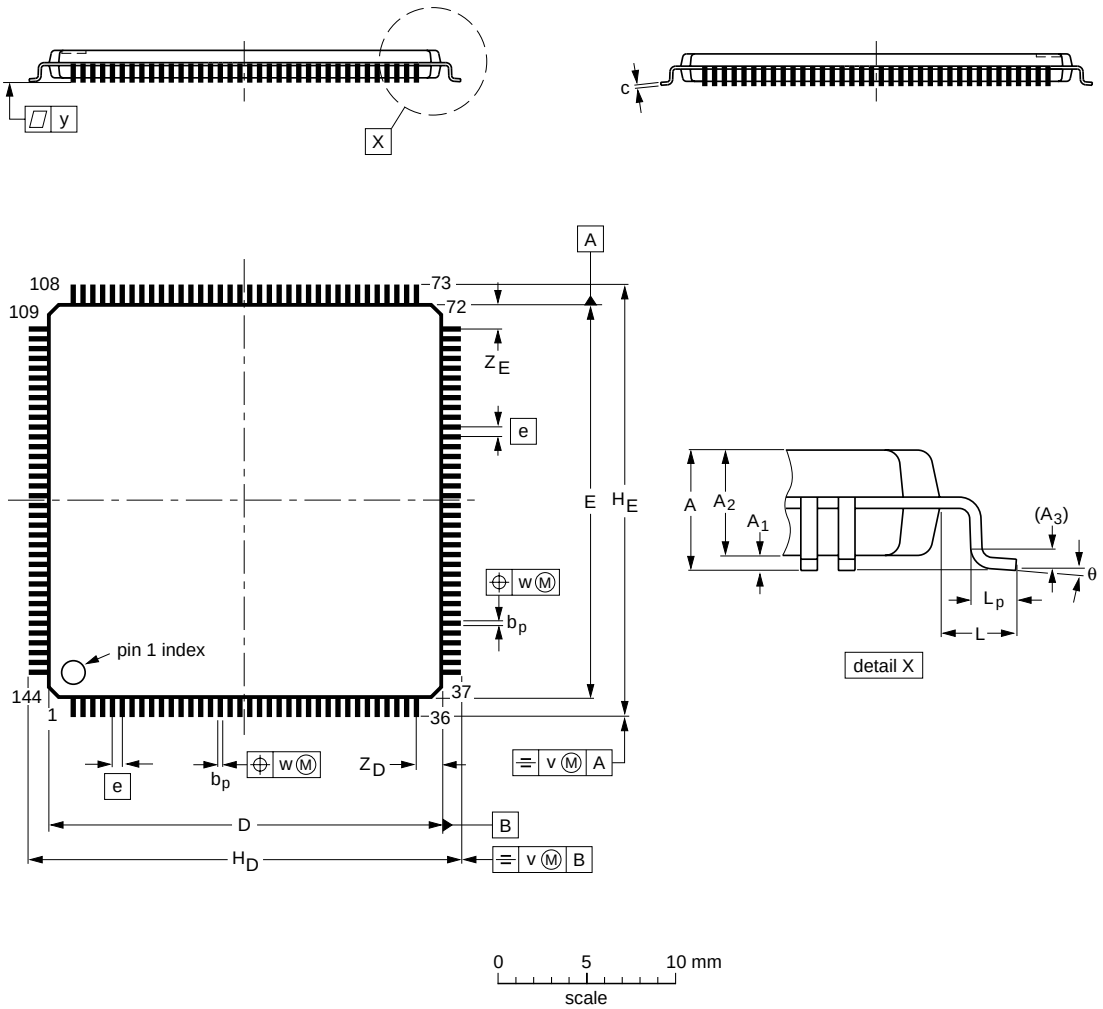
[3] This parameter is not part of production testing or final testing, hence only a typical value is stated.

[4] Oscillator start-up time depends on the quality of the crystal. For most crystals it takes about 1000 clock pulses until the clock is fully stable.

[5] Duty cycle clock should be as close as possible to 50 %.

13. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 15. Package outline SOT486-1 (LQFP144)

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 32 and 33

Table 32. SnPb eutectic process (from J-STD-020C)

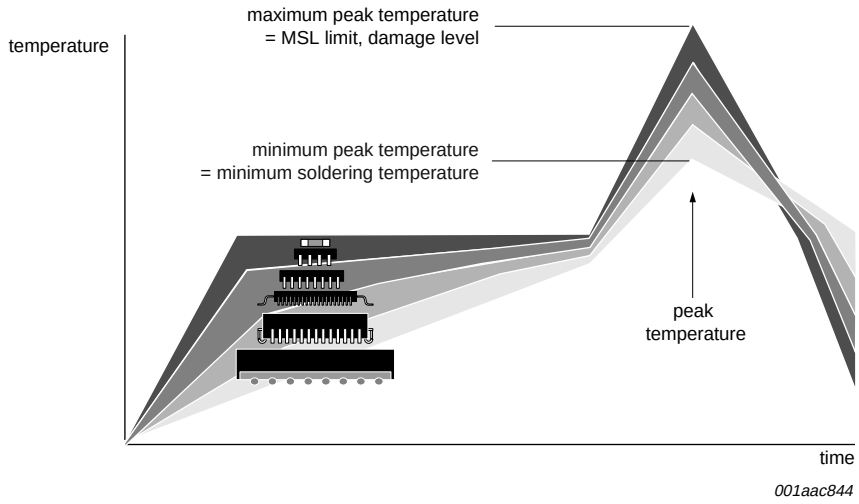
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 33. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2917_19_1	20080731	Product data sheet	-	-

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