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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	25MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32hg310f64g-b-qfn32r

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32HG310 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32HG310F32G-B-QFN32	32	8	25	1.98 - 3.8	-40 - 85	QFN32
EFM32HG310F64G-B-QFN32	64	8	25	1.98 - 3.8	-40 - 85	QFN32

Adding the suffix 'R' to the part number (e.g. EFM32HG310F32G-B-QFN32R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

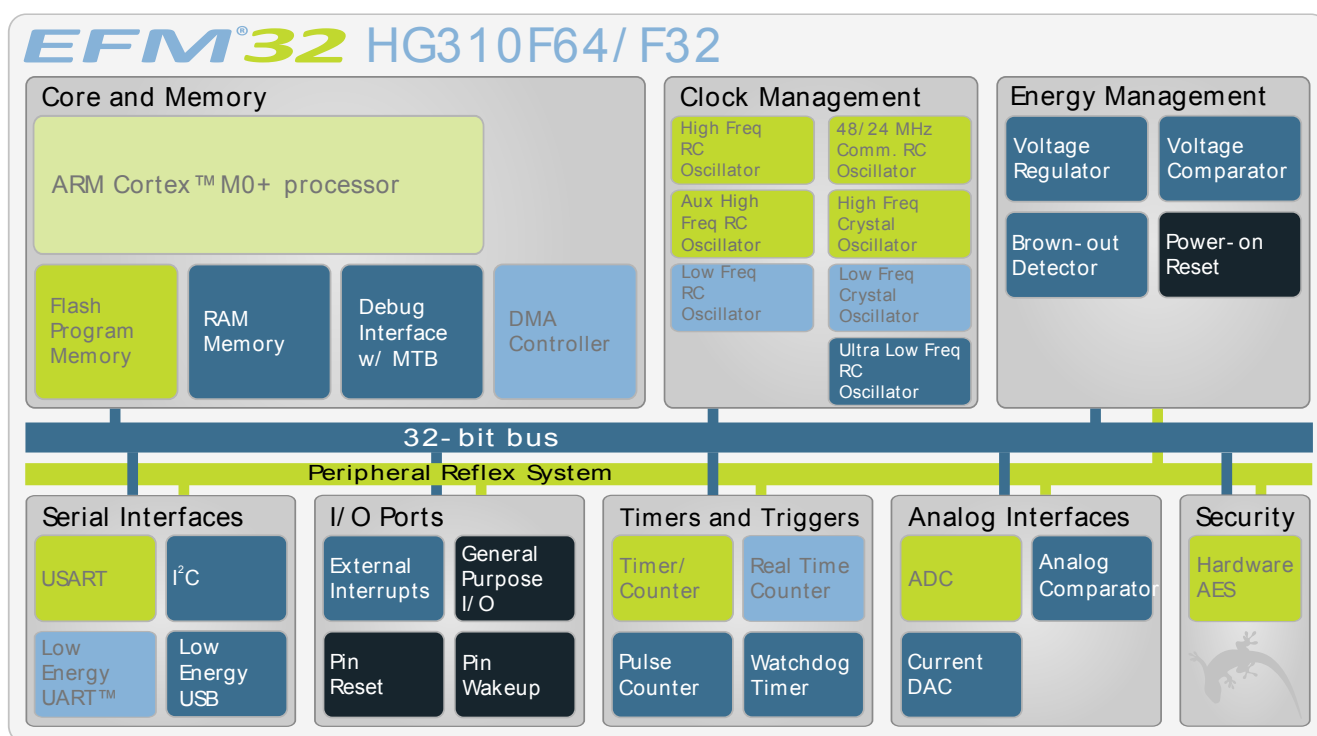
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32HG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32HG310 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32HG Reference Manual*.

A block diagram of the EFM32HG310 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and a Micro Trace Buffer (MTB) for data/instruction tracing.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		24 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		85	91	μA/ MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		86	92	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		51	55	μA/ MHz
		24 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		52	56	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		53	57	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		54	58	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		56	59	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		57	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		58	61	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		59	63	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		64	68	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		67	71	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		106	114	μA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		114	126	μA/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		0.9	1.35	μA

Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz

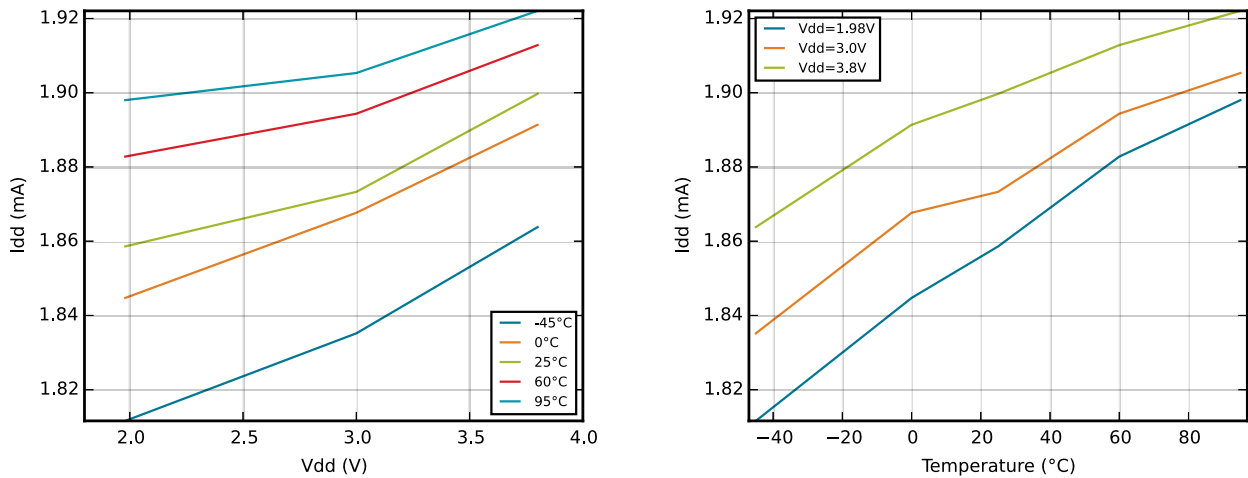


Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz

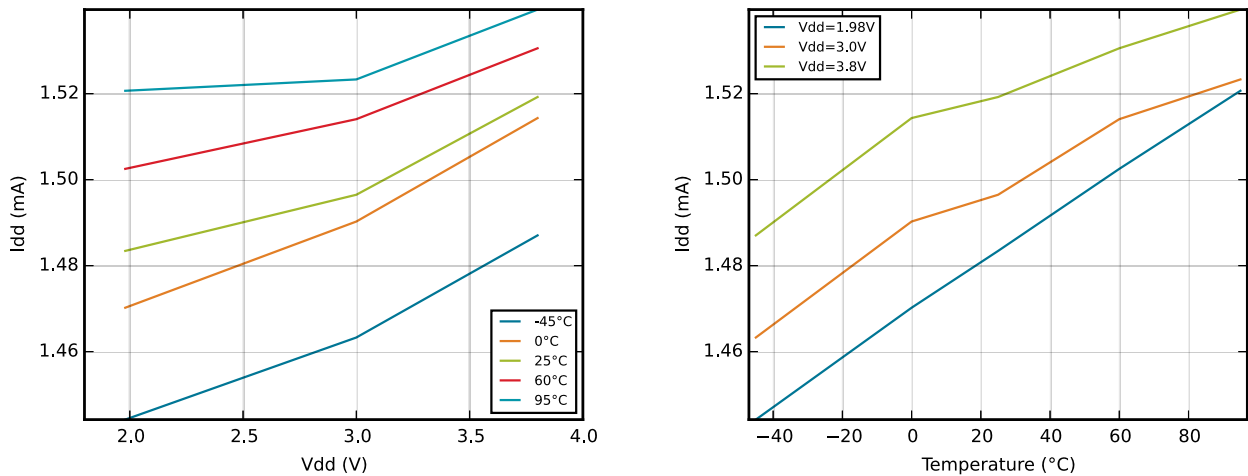


Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz

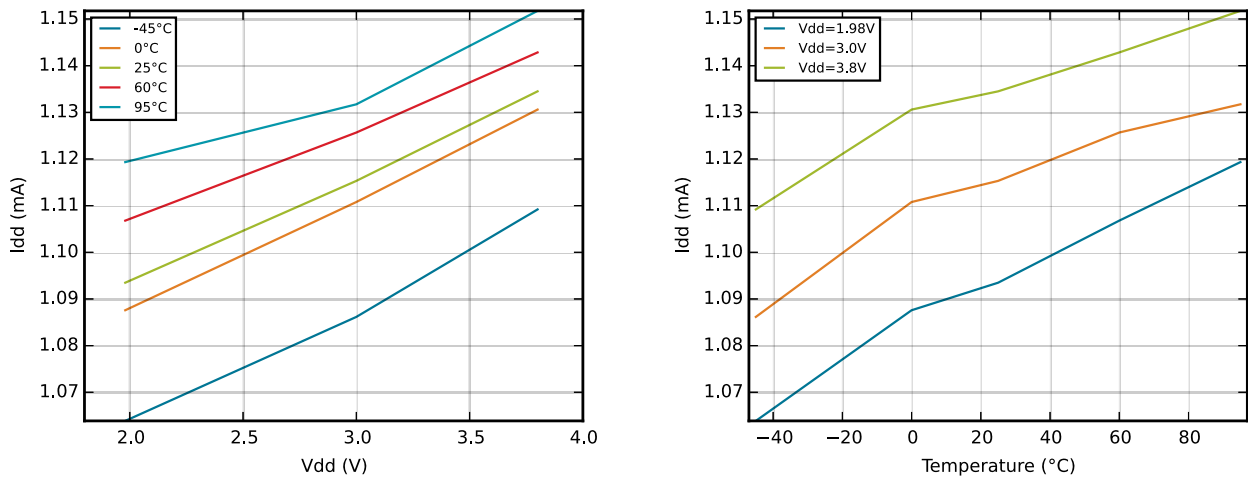
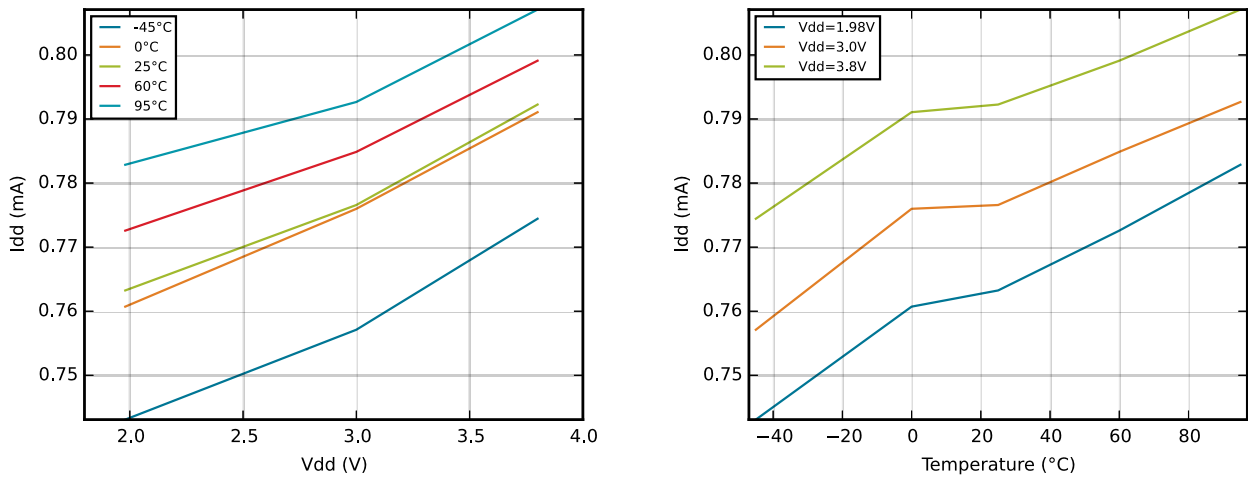
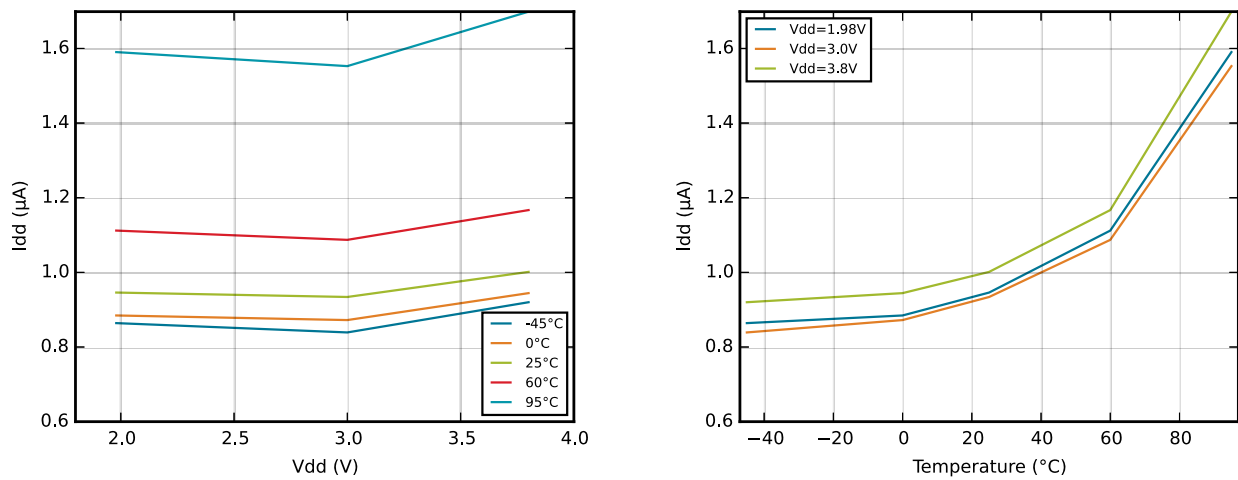


Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz



3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.

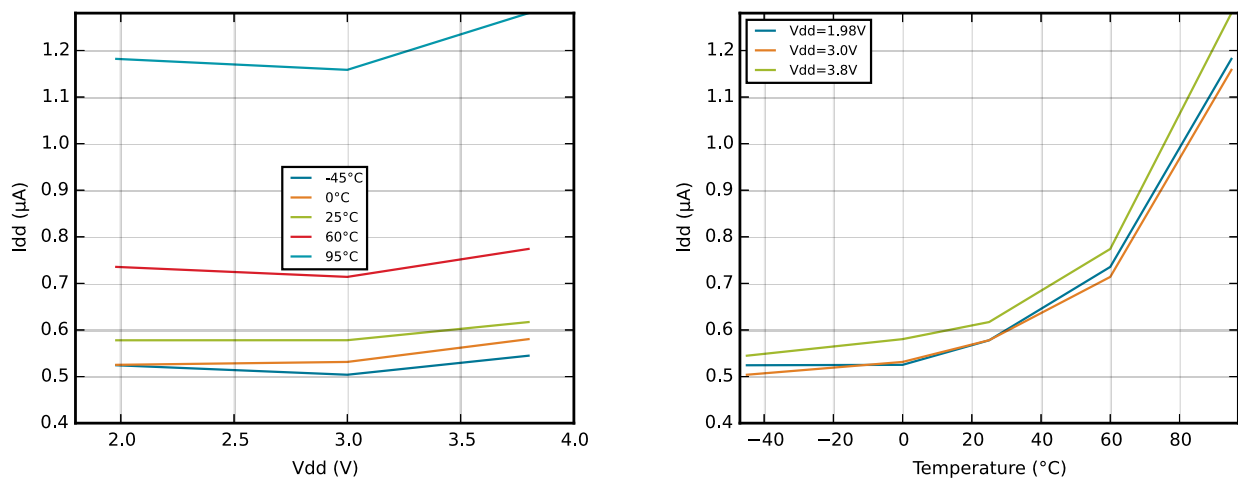
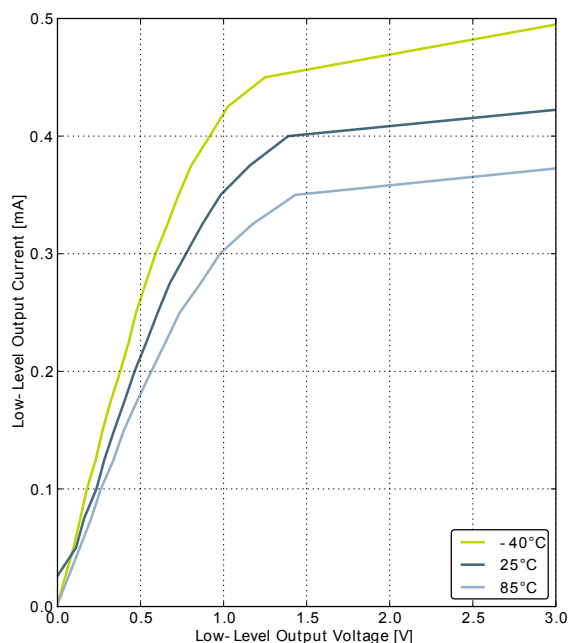
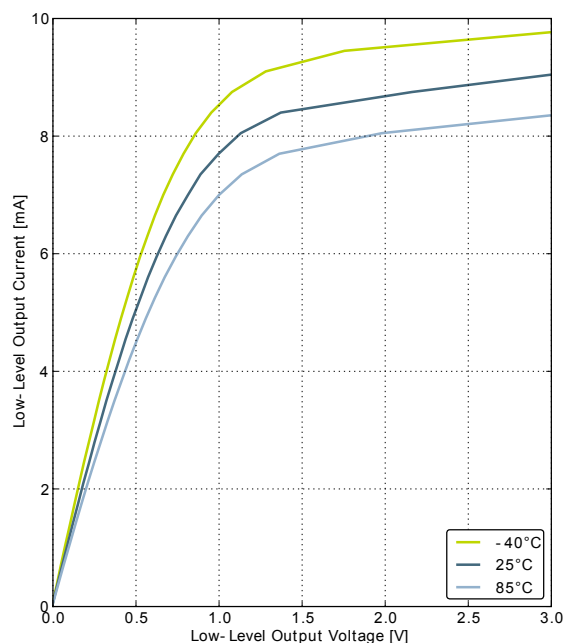
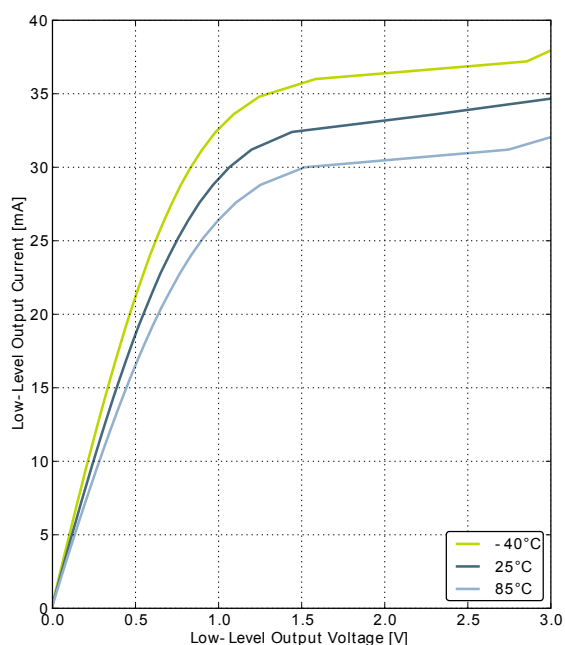


Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage

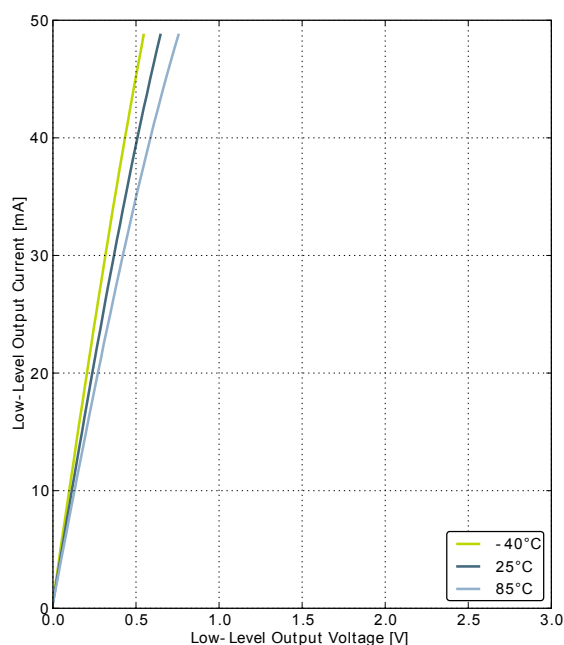
GPIO_Px_CTRL DRIVEMODE = LOWEST



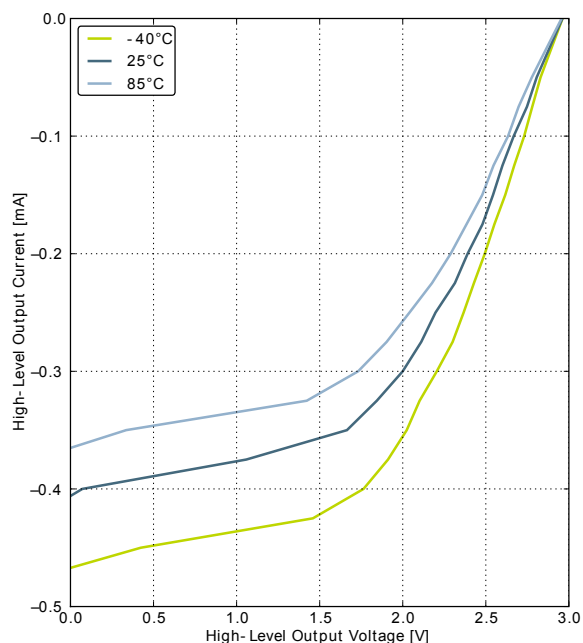
GPIO_Px_CTRL DRIVEMODE = LOW



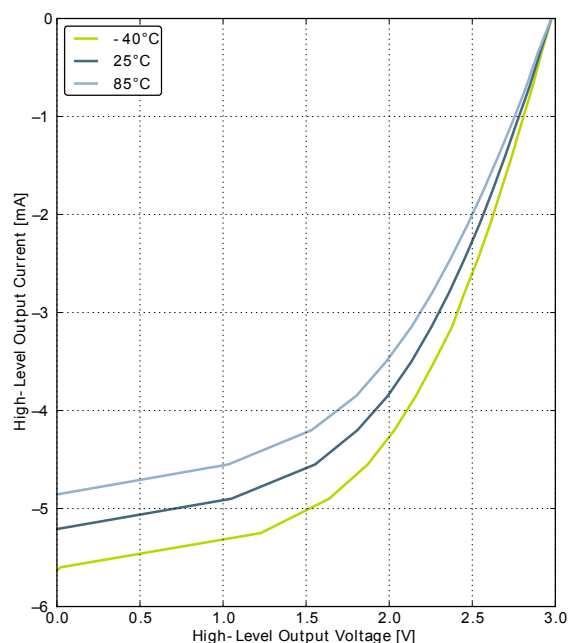
GPIO_Px_CTRL DRIVEMODE = STANDARD



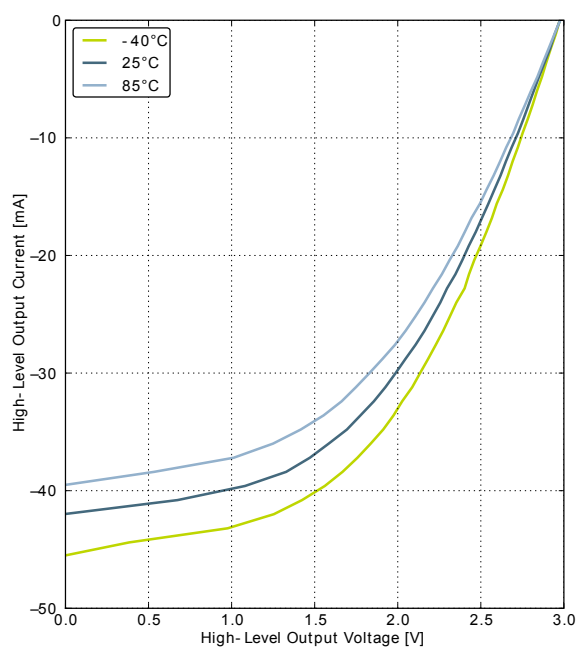
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage

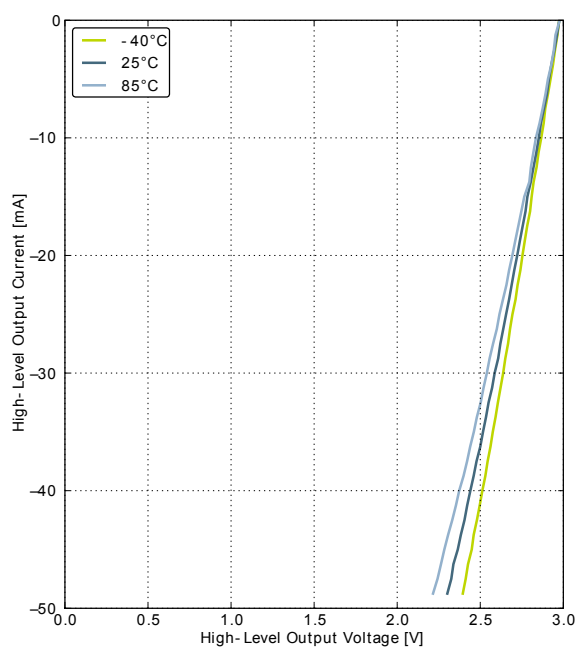
GPIO_Px_CTRL DRIVEMODE = LOWEST



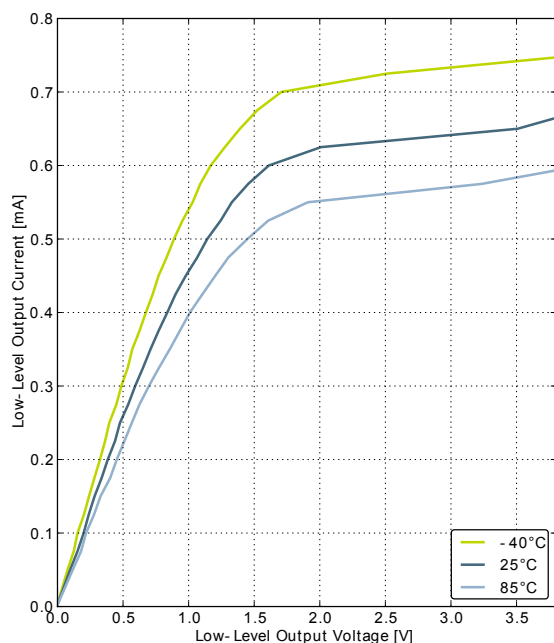
GPIO_Px_CTRL DRIVEMODE = LOW



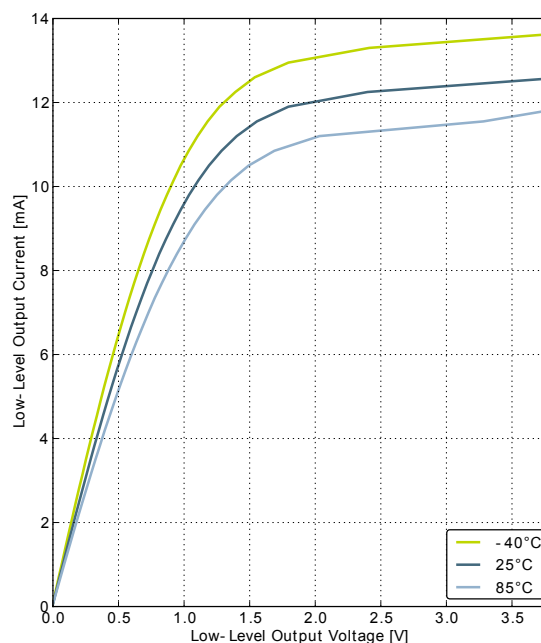
GPIO_Px_CTRL DRIVEMODE = STANDARD



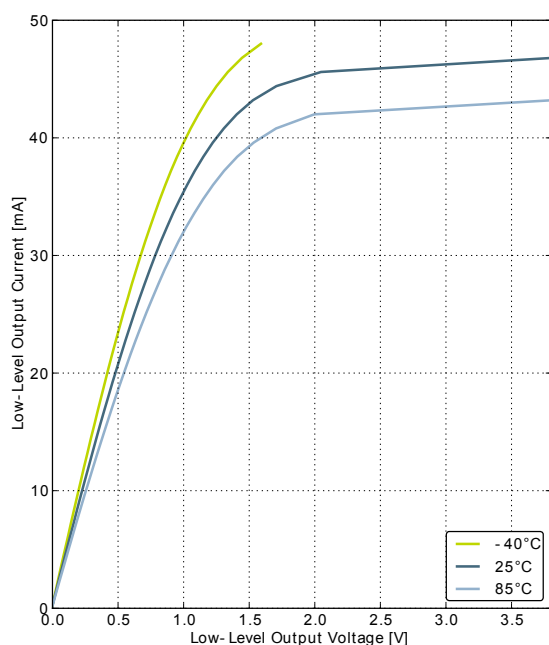
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage

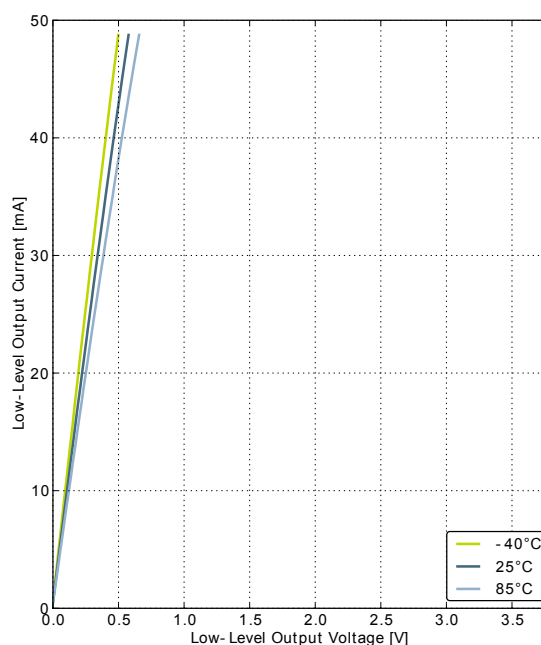
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.6 USHFRCO

Table 3.13. USHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{USHFRCO}	Oscillation frequency	No Clock Recovery, Full Temperature and Supply Range, 48 MHz band	47.10	48.00	48.90	MHz
		No Clock Recovery, Full Temperature and Supply Range, 24 MHz band	23.73	24.00	24.32	MHz
		No Clock Recovery, 25°C, 3.3V, 48 MHz band	47.50	48.00	48.50	MHz
		No Clock Recovery, 25°C, 3.3V, 24 MHz band	23.86	24.00	24.16	MHz
		USB Active with Clock Recovery, Full Temperature and Supply Range	47.88	48.00	48.12	MHz
TC_{USHFRCO}	Temperature coefficient	3.3V		0.0175		%/°C
VC_{USHFRCO}	Supply voltage coefficient	25°C		0.0045		%/V
I_{USHFRCO}	Current consumption	$f_{\text{USHFRCO}} = 48 \text{ MHz}$	1.21	1.36	1.48	mA
		$f_{\text{USHFRCO}} = 24 \text{ MHz}$	0.81	0.92	1.02	mA

3.9.7 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{\text{REF}}/2$		$V_{\text{REF}}/2$	V
V_{ADCREFIN}	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{\text{ADCREFIN_CH7}}$	Input range of external negative reference voltage on channel 7	See V_{ADCREFIN}	0		$V_{\text{DD}} - 1.1$	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCREFIN_CH6}	Input range of external positive reference voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
V _{ADCCMIN}	Common mode input range		0		V _{DD}	V
I _{ADCIN}	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input common mode rejection ratio			65		dB
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		392	510	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		μA
I _{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MΩ
R _{ADCFLT}	Input RC filter resistance			10		kΩ
C _{ADCFLT}	Input RC filter/de-coupling capacitance			250		fF
f _{ADCCLK}	ADC Clock Frequency				13	MHz
t _{ADCCONV}	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc

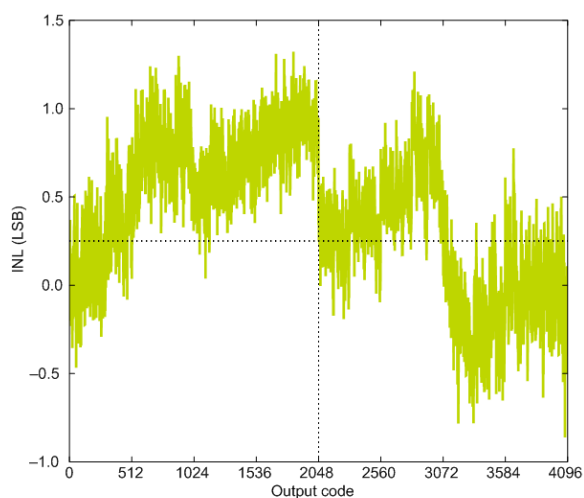
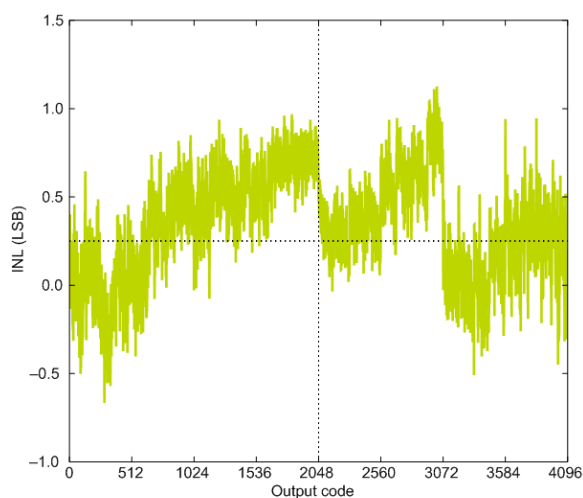
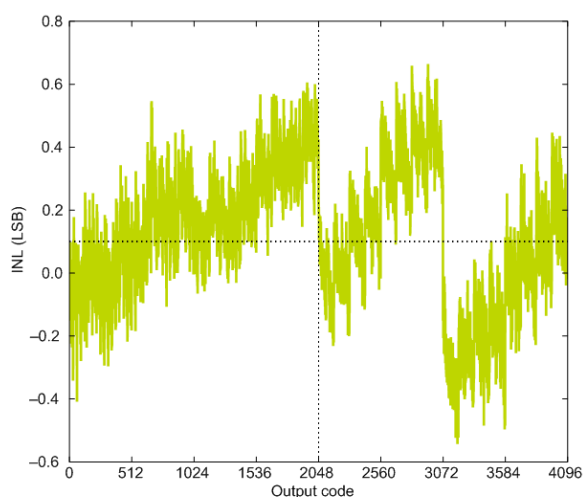
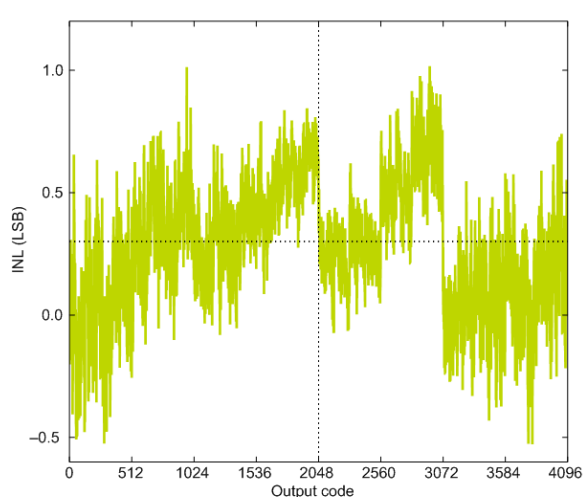
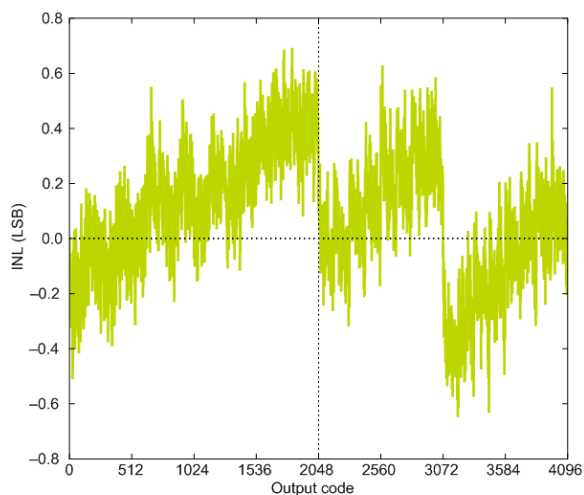
Figure 3.29. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

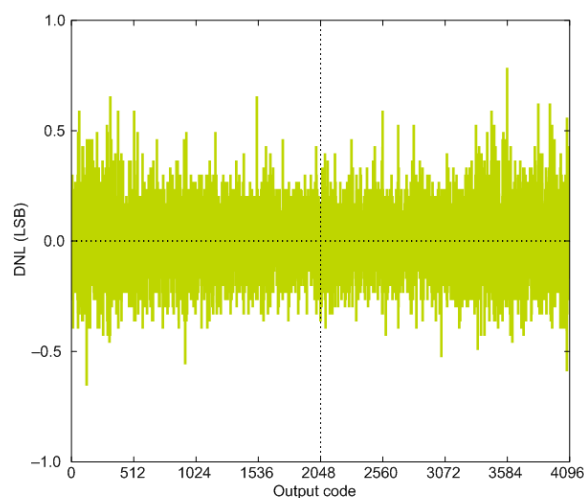
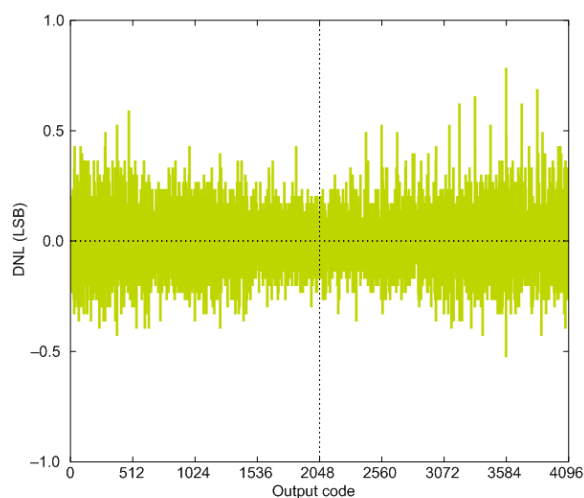
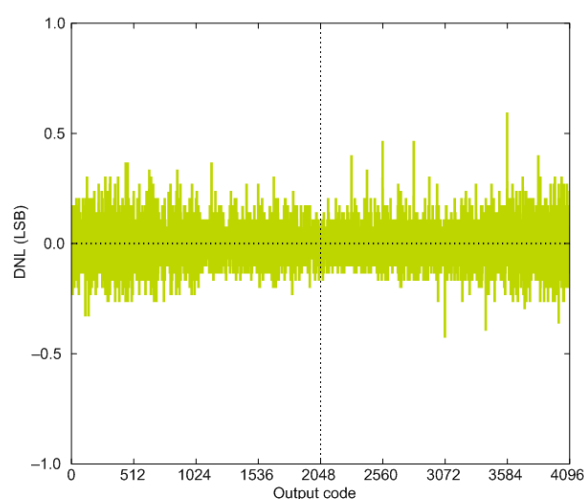
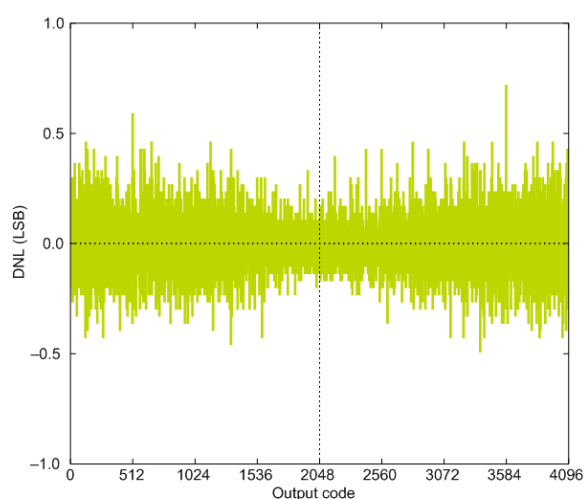
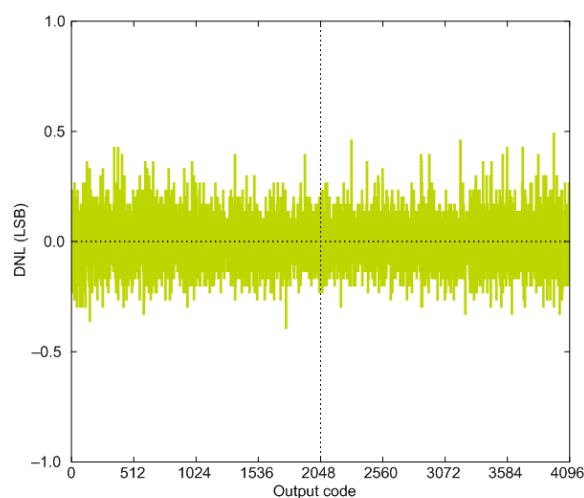
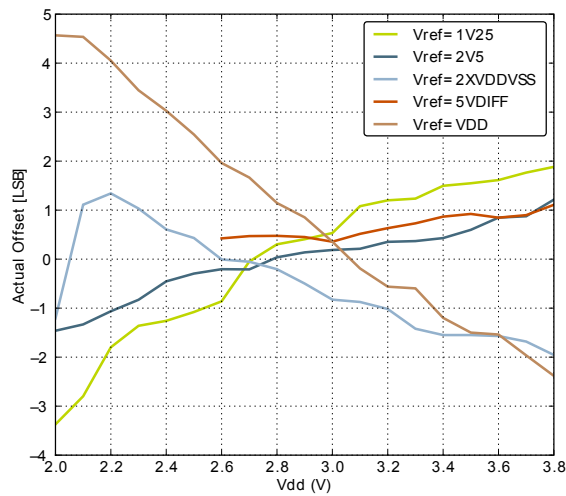
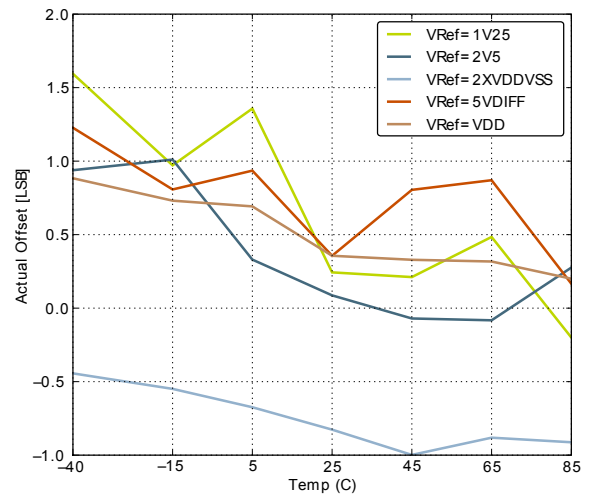
Figure 3.30. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.31. ADC Absolute Offset, Common Mode = $V_{dd} / 2$

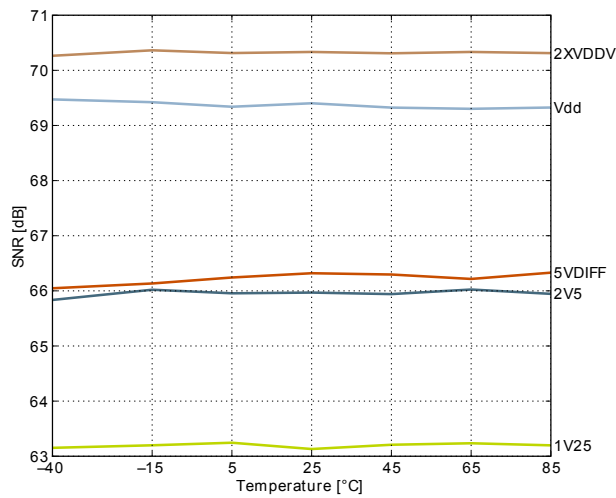


Offset vs Supply Voltage, Temp = 25°C

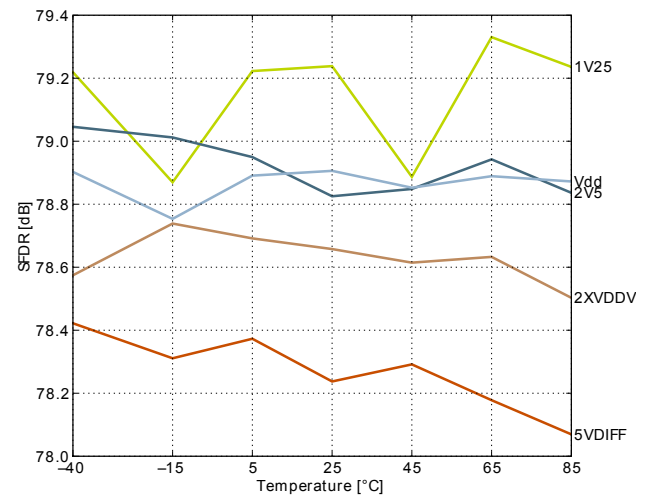


Offset vs Temperature, $V_{dd} = 3V$

Figure 3.32. ADC Dynamic Performance vs Temperature for all ADC References, $V_{dd} = 3V$



Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			8.5		μA
I_{STEP}	Step size			0.5		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = 200 \text{ mV}$		0.62		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		2.8		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		94.4		nA/V

Table 3.22. IDAC Range 3 Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		18.7		μA
		Duty-cycled		10		nA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			33.9		μA
I_{STEP}	Step size			2.0		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = V_{\text{DD}} - 100 \text{ mV}$		3.54		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		10.9		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		159.5		nA/V

Table 3.23. IDAC Range 3 Sink

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IDAC}	Active current with STEPSEL=0x10	EM0, default settings		62.5		μA
I_{0x10}	Nominal IDAC output current with STEPSEL=0x10			34.1		μA
I_{STEP}	Step size			2.0		μA
I_{D}	Current drop at high impedance load	$V_{\text{IDAC_OUT}} = 200 \text{ mV}$		1.75		%
TC_{IDAC}	Temperature coefficient	$V_{\text{DD}} = 3.0 \text{ V}$, STEPSEL=0x10		10.9		$\text{nA}/^\circ\text{C}$
VC_{IDAC}	Voltage coefficient	$T = 25^\circ\text{C}$, STEPSEL=0x10		148.6		nA/V

Table 3.24. IDAC

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{IDACSTART}}$	Start-up time, from enabled to output settled		40		μs

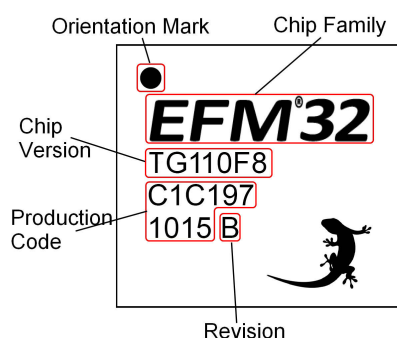
QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
2	PA1		TIM0_CC0 #6 TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0
4	IOVDD_0	Digital IO power supply 0.			
5	PC0	ACMP0_CH0	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5/6 US1_TX #0 US1_CS #5 I2C0_SDA #4	PRS_CH2 #0
6	PC1	ACMP0_CH1	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5/6 US1_TX #5 US1_RX #0 I2C0_SCL #4	PRS_CH3 #0
7	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
8	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
9	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PB11	IDAC0_OUT	TIM1_CC2 #3 PCNT0_S1IN #4	US1_CLK #4	CMU_CLK1 #3 ACMP0_O #3
11	AVDD_2	Analog power supply 2.			
12	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
13	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
14	IOVDD_3	Digital IO power supply 3.			
15	AVDD_0	Analog power supply 0.			
16	PD5	ADC0_CH5		LEU0_RX #0	
17	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	US1_RX #2/3 I2C0_SDA #1	ACMP0_O #2
18	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2/3 I2C0_SCL #1	CMU_CLK0 #2
19	VDD_DREG	Power supply for on-chip voltage regulator.			
20	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
21	USB_VREGI				
22	USB_VREGO				
23	PC14		TIM0_CDTI1 #1/6 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 US1_CS #3/4 LEU0_TX #5 USB_DM	PRS_CH0 #2
24	PC15		TIM0_CDTI2 #1/6 TIM1_CC2 #0	US0_CLK #3 US1_CLK #3 LEU0_RX #5 USB_DP	PRS_CH1 #2
25	PF0		TIM0_CC0 #5	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0 BOOT_TX
26	PF1		TIM0_CC1 #5	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3 BOOT_RX
27	PF2		TIM0_CC2 #5/6 TIM2_CC0 #3	US1_TX #4 LEU0_TX #4	CMU_CLK0 #3 PRS_CH0 #3

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 61) .

6.3 Errata

Please see the errata document for EFM32HG310 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

B Contact Information

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Please visit the Silicon Labs Technical Support web page:

<http://www.silabs.com/support/pages/contacttechnicalsupport.aspx>

and register to submit a technical support request.

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